

reset
 clk
 enable
 rd1
 rd2
 wr
 call
 ret
 busy
 mmu_en
 mmu_w_r
 add_wr[5:0]
 add_rd1[5:0]
 add_rd2[5:0]
 datain[7:0]
 out1[7:0]
 out2[7:0]
 mmu_d_in[7:0]
 mmu_d_out[7:0]
 mmu_add[5:0]
 RF
 add_wrs[32:0]
 add_rd1s[32:0]
 add_rd2s[32:0]
 mmu_adds[43:0]
 datains[7:0]
 out1s[7:0]
 out2s[7:0]
 rd1s
 rd2s
 wrs









