COMP2611 Spring 2019 Homework #1

Note:

- **The deadline is at 5pm on Friday, Mar 8.**
- **Work out your solution either by typing or handwriting.**
- **Take photos of the solution before submission.**
- **Submit a hard copy to COMP2611 assignment collection box. The box is in a big blue metal cabinet located in the CSE lab area, in the corridor of lift 21 opposing the male-toilet close to life 21. There are assignment collection boxes for other courses nearby, make sure you submit to the COMP2611 box. Collection box 16 for Comp2611 L1; collection box 17 for Comp2611 L1 and L3.**

Question 1: Data representation (16 points)

a) Given the following **signed integer values**, write their corresponding 16-bit 2's complement representations and decimal values. (4 points)

1) $DC72_{(16)}$:

2's complement =

Decimal =

2) $213_{(10)}$:

2's complement =

Hexadecimal =

b) Given the following **signed integer values**, write their corresponding 32-bit 2's complement representations and decimal values. (4 points)

1) $BF5D_{(16)}$:

2's complement =

Decimal =

2) $-4823_{(10)}$:

2's complement =

Hexadecimal =

c) Give the IEEE754 single-precision representation of the following decimal number. Can the decimal number be represented exactly? If not, please find the nearest approximation of the number. Show your steps briefly. (4 points)

1) -1526.625

2) 0.1025

d) What decimal values are represented by the following IEEE754 single-precision floating-point representations? Show your steps briefly. (4 points)

1) 1 1000 0001 11111000000000000000000

2) 0 0000 0000 10110010000000000000000

Question 2: Boolean algebra (8 points)

Simplify the following logic equations using the laws of Boolean algebra only. Briefly show your steps.

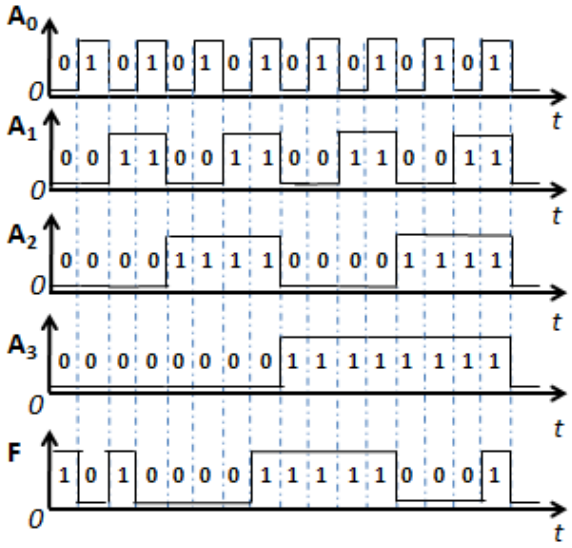
a) $ABC + ABC\overline{D} + AB\overline{DE} + AC\overline{E} + A\overline{C}\,\overline{E}$

b) $AB + \overline{A}C + BC$

c) $\overline{A}\,\overline{B}\,C + \overline{A}BC + A\overline{B}C + AB\overline{D} + ABD$

Question 3: Combinational Logic (14 points)

We are given a black-box circuit and wish to reverse engineer the circuit and implement the circuit according to its input/output behavior by probing the circuit using an oscilloscope. The following oscilloscope diagram shows the changes of the inputs A_0, A_1, A_2, and A_3, and the corresponding output F of the black-box circuit. The X-axis of the diagram denotes the time and the Y-axis denotes the voltage levels of the inputs and the output (assume high voltage corresponds to 1, and low voltage corresponds to 0). By referring to the diagram, and by assuming there is no delay for the circuit to produce the output, answer questions below.



a) Complete the truth table for the output of this black-box circuit. (3 points)

Input				Output
A_3	A_2	A_1	A_0	F
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

b) Derive the logic expression $F(A_0, A_1, A_2, A_3)$ for this black-box circuit, in both the **Sum-of-Product** format and the **Product-of-Sum** format. There is no need to simplify the expression for the part of the question. (2 points)

1) The **SoP** expression :

2) The **PoS** expression:

c) Use K-map below to simplify the SoP expression. Write the logic function in simplest form. (5 points)

A_1A_0 \ A_3A_2	00	01	11	10
00				
01				
11				
10				

The simplest logic form is:_____

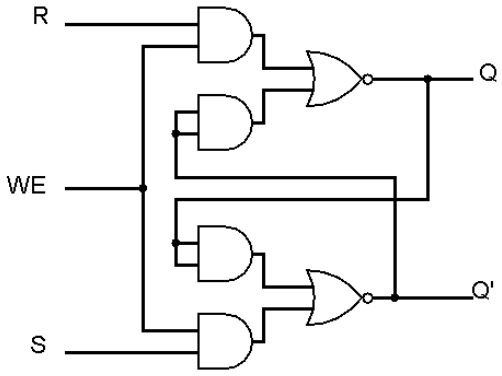
_____

d) Implement the simplified logic equation using **NOT**, **AND**, **OR** gates ***only***.

Note: You can use at most 6 gates for the circuit. If you use more than 6 gates and your logic is correct, you will get 2 points. If you use any gate (other than **NOT**, **AND**, **OR**) or if your logic is incorrect, you will get zero point. (4 points)

Question 4: Sequential Logic (12 points)

a) Fill the truth table of the given sequential logic circuit. Assume **Q** to be the value of the output after the corresponding logic gates have been given enough time to produce the output according to the inputs. If you feel the older **Q** value will be preserved by the input combination, put "**Latch**" in the table for the output Q. (6 points)



Input			Output
WE	S	R	Q
1	0	0	
1	0	1	
1	1	0	
1	1	1	Forbidden

b) A pair of positive edge-triggered (i.e. rising edge triggered) D-flip-flops are connected as shown below. Complete the timing diagram below for this circuit. Ignore propagation delays. Assume $Q_1=Q_2=0$, initially. (6 points)