FPGA Code Instructions:

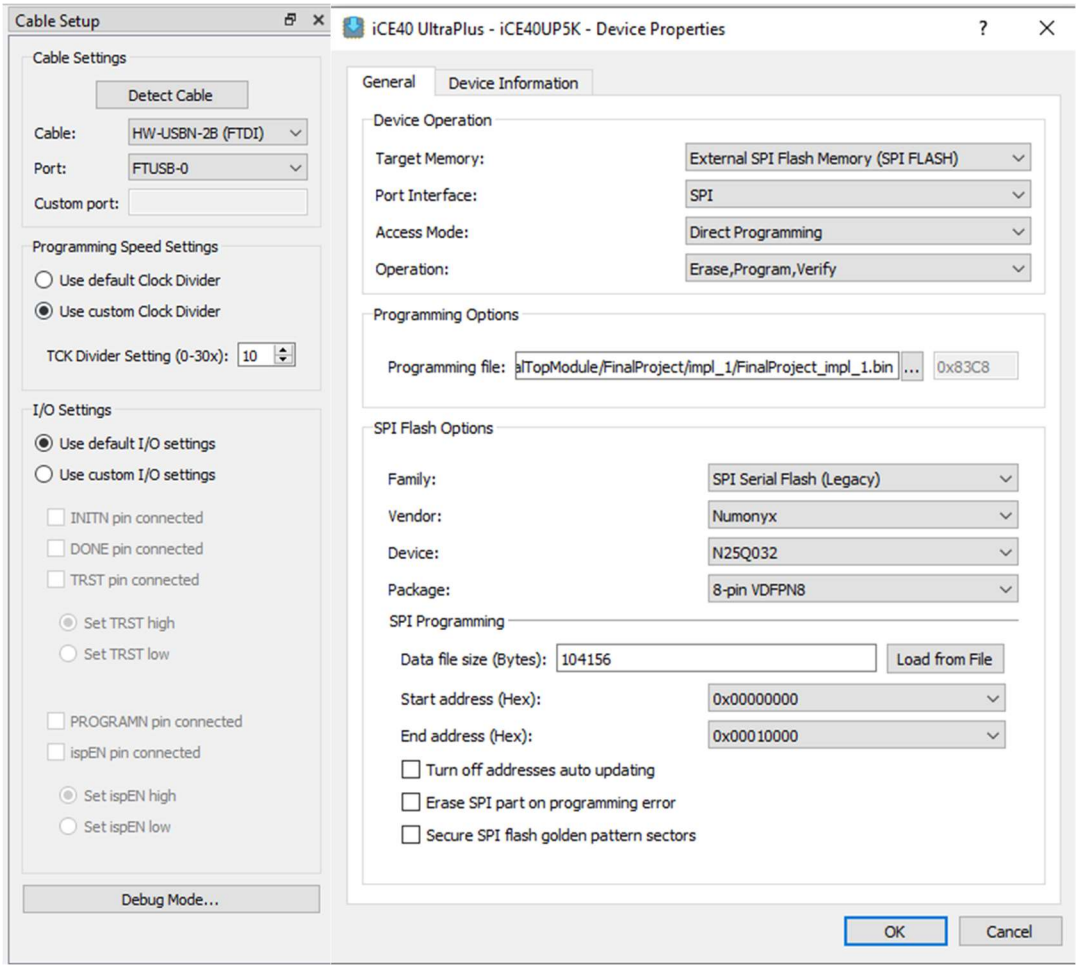
Open Lattice Radiant 3.1 -> Open Project-> (navigate to RDF file in FPGA Code Folder and open) Double Check Project Implementation that file topwclks.v is Top Module

To synthesize into bitstream and download

- Note: The LED pins and Module are commented out for simulation purposes as the libraries don't compile in ModelSIM, however they function on hardware. If hardware testing, uncomment the led outputs and the "LED u_LED" module in topwclks.v

Run Synthesis process and double check existing input and output pins match Schematic (Included Excel Sheet) sometimes Radiant will reset these selections upon synthetization.

Open Radiant Programmer-> Select iCE40 Ultra Plus family, iCE40UP5K, correct File Name. Make sure cable set up and device properties matches below:

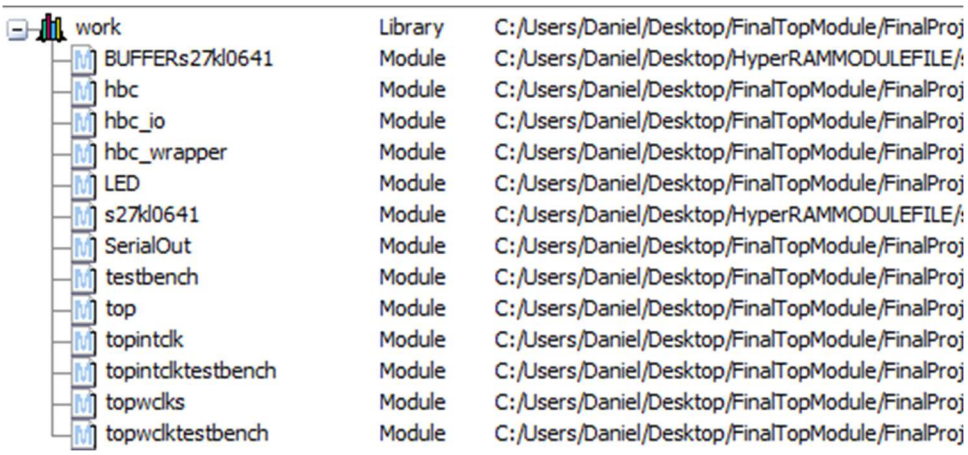


Program Device and Wait for Process to Finish. 

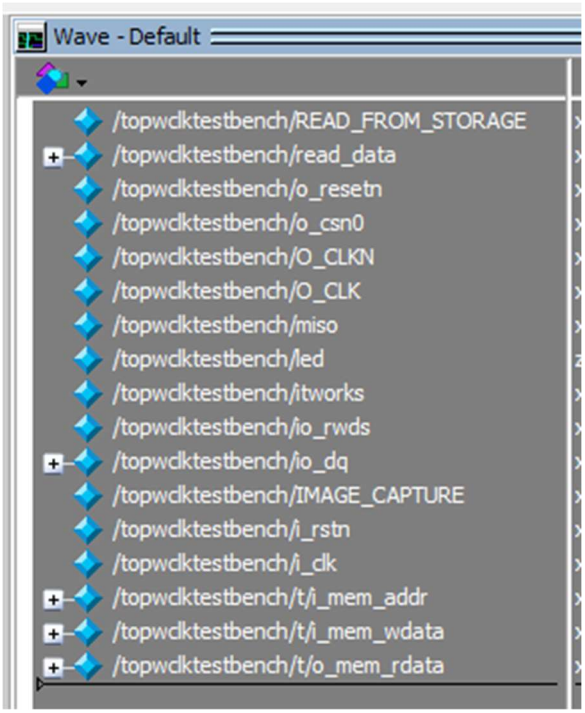
To simulate in ModelSIM:

Open ModelSIM from Radiant 

->Compile all project files that aren't grayed out in the Input Files folder from Lattice Radiant-> They should appear in the work library in Model Sim like below:



In the console type "vsim -L iCE40UP topwclktestbench" to simulate the correct testbench using iCE40UP libraries. Select the Objects you want to view and drag to the wave section to watch their behaviors. I recommend this setup:



Run simulation for a step of 160ms (takes 45 seconds or so) then I recommend intervals of 100ns until testbench reaches $stop.