Table

Description automatically generated

Lab Report (Diodes) By: Danilo Zelenovic

Date of Preparation: Feb 1, 2022

**Table of Contents**

1. Objectives………………………………………………………………… page 3
2. Schematics/Simulation Results………………………………… page 3
3. Conclusions and Remarks………………………………………… page 5
4. References……………………………………………………………… page 8
5. Appendix (Prelab)…………………………………………………… page 8
6. **Objectives**

The objective of this lab was to understand the behaviour of a diode under different signal values, as well as to calculate the difference made when an additional resistance was added in parallel to the diode, which was done at multiple different current values. The obtained values were checked for correctness for the analysis.

1. **Schematics/Simulation Results**

**Figure 1** below shows the circuit that was to be designed in the lab. 2 circuits are shown below, but the two circuits were made into one with the use of a switch, which allowed us to quickly switch between the two different circuits. Both circuits contain a resistor R, a voltage input Vcc, and a diode.

**Figure 2** shows the circuit created in the Multisim virtual environment that was used to gather the data. The circuit was checked and approved.

Diagram, schematic

Description automatically generated

**Figure 1.** (a) Diode biased with DC power supply. (b) same circuit as (a) but with an additional Rsh resistor added in parallel to the diode.

A picture containing scatter chart

Description automatically generated

**Figure 2.** Multisim schematic created to test a diode, based on **figure 1**. A switch was implemented to rapidly switch between **Figure 1 (a) and (b).**

The circuit in  **Figure 2** was created in Multisim by connecting a variable DC power source to a resistor. The diode was then put in parallel to a switch in series with a resistor. The circuit is also grounded. The experiment was run for varying source voltages. Probes were set up to measure the voltage after the 1kΩ resistor, and the current was measured across the diode. At each current reading specified in the lab manual (or as close as possible to it), the values of our Vcc and the voltage probe was measured while the switch was open. Next, the switch was closed, and the value of the voltage probe was taken again. The Rsh vales were also changed according to the lab manual for **Figure 1(b).** The values are shown below in **Table E1.**

**Table E1**. Test results for the circuits of **Figure 1(a)** and **Figure 1(b).**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | Vcc [V] |  |  |  |  |  | ) 1000 |
| 10 | 10.668 | 0.671 | 1.5 | 0.669 | -0.002 | -0.446 | 4.43 |
| 7 | 7.656 | 0.657 | 2.2 | 0.655 | -0.002 | -0.298 | 6.71 |
| 5 | 5.64 | 0.645 | 2.7 | 0.644 | -0.001 | -0.239 | 4.13 |
| 2 | 2.616 | 0.617 | 6.8 | 0.615 | -0.002 | -0.0904 | 22.12 |
| 1 | 1.596 | 0.597 | 12 | 0.596 | -0.001 | -0.0497 | 20.12 |

1. **Conclusions and Remarks**

This section includes both the questions and the answers from this lab. The questions have been copied and pasted for easy reference and have been bolded and italicized.

***C1. Describe the waveforms of Graph P1(a) and explain what is happening. Also, comment on the v-i characteristic of Graph P1(b). Did you expect this characteristic curve? Explain.***

The Vs-t Graph P1(a) takes a triangular shape. It has a 12V voltage amplitude, which translates to 24V peak-to-peak. Each period is 1ms, as specified in the setting of the source voltage. The simulation settings were adjusted to allow for 3 cycles to be graphed.

The Vi-t Graph P1(a) is very similar to the Vs-t graph, as the Vi node is separated from the Vs by only 1 resistor which has a resistance value of 50Ω which is not very much. That is why the graph looks similar but is ever so vertically compressed.

The Vd-t Graph P1(a) shares a general structure with the previous graphs mentioned above. The main difference this time is that the Vd node is positioned after the Vi node and separated by a 1kΩ resistor. Because of this, the voltage reaching the node is capped to about 50% of the maximum source voltage. The source voltage amplitude was 12V, meaning the voltage flattened and capped at around 6V. All of the graphs were adjusted to -6V, which is why the graph signal goes from -6V to 0V instead of 0V to 6V.

The id-t **graph P1(a)** shows a straight line. This is because the circuit from **Prelab** **Figure 1** is entirely in series, meaning the current will be the same through the entire circuit and will remain constant, as the diode will allow the current to flow in a specific direction with no problem, and will restrict the current flow from the opposing direction.

I did expect the characteristic curve of the diode to look similar to what was produced in **graph P1(b)** because I noticed that the diode was forward-biased. From the lecture notes of this semester and the previous semester, I was able to predict the general shape of the diode v-I curve. We know that i increases as v increases for a forward biased diode and decreases and v decreases to be reverse biased.

**C2. Calculate Is and n for the diode. Write a program code to plot the v-I characteristic of the diode. (Paraphrased to shorten and simplify question).**

**A picture containing text, whiteboard

Description automatically generated**

Above: Calculations to find n and Is in the diode.

Graphical user interface, text, application

Description automatically generated

Above is a screenshot of my MATLAB code which was inspired by the code found at the following link:

<https://www.mathworks.com/matlabcentral/answers/657758-diode-i-v-curve-graph#answer_552533>

The graph was found to be:

Chart, line chart

Description automatically generated

**Graph C2.** Graph simulated in MATLAB, designed by code featured above.

1. **References**

Mohamad. (2020, November 22). *Diode I-V curve graph*. Diode i-v Curve Graph -. Retrieved February 2, 2022, from https://www.mathworks.com/matlabcentral/answers/657758-diode-i-v-curve-graph#answer\_552533

1. **Appendix**

The following are screenshots of the prelab report that has been submitted. They have not been signed as labs have been virtual.

**Chart

Description automatically generated** **Graphical user interface

Description automatically generated** Graphical user interface

Description automatically generated Histogram

Description automatically generated Graphical user interface

Description automatically generated