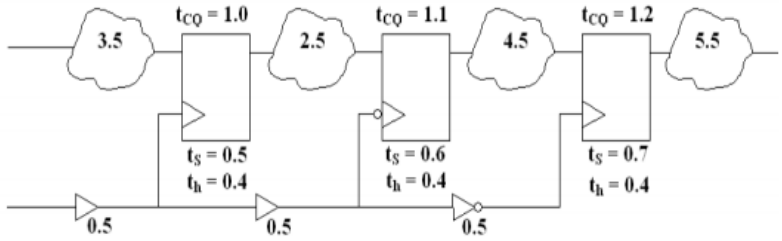
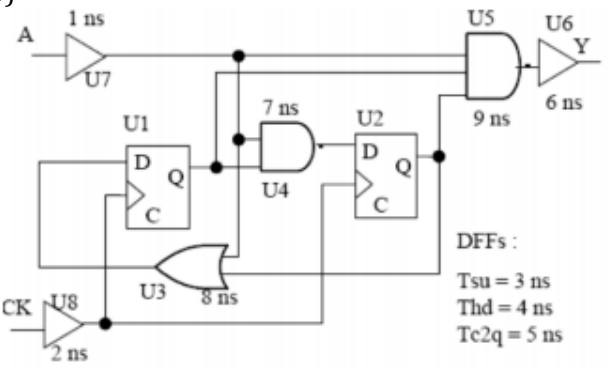
CSCE337: Digital Design II
HW 3

Q1) Find the maximum clock frequency for the following circuits: [3x25pts]

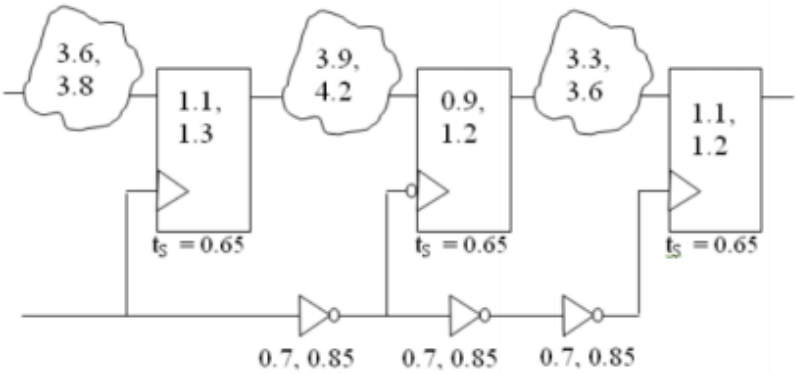
a)



b)

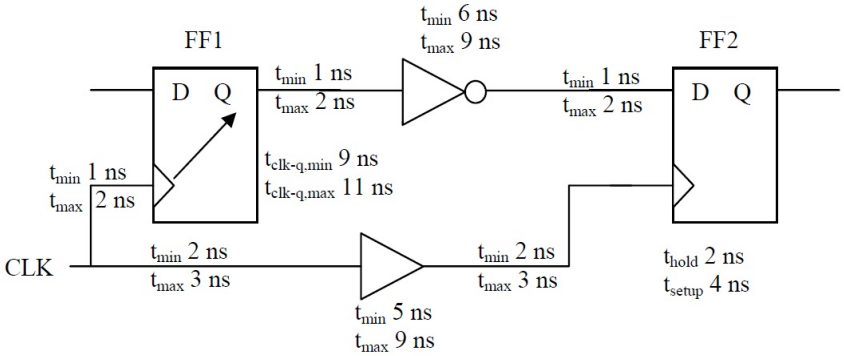


c)



For combinational Logic: The first number is the contamination Delay and the Second is the Propagation Delay. For Flip-Flops: The first number is the minimum Clock-to-Q and the second number is the maximum Clock-to-Q.

Q2) Calculate the hold slack and the setup stack of the following circuit. FF1 and FF2 are identical.



Due Date is Sunday May 2nd, 2015 11:59PM by email to the TA.