CMPE 374 | Digital Systems Engineering

Phase 1 Submission

Feb 25th, 2020

Daniyal Maniar | 20064993

Hermann Krohn |

## Register



## Register File



## Register Multiplexer

## ALU



## ALU Result Selector

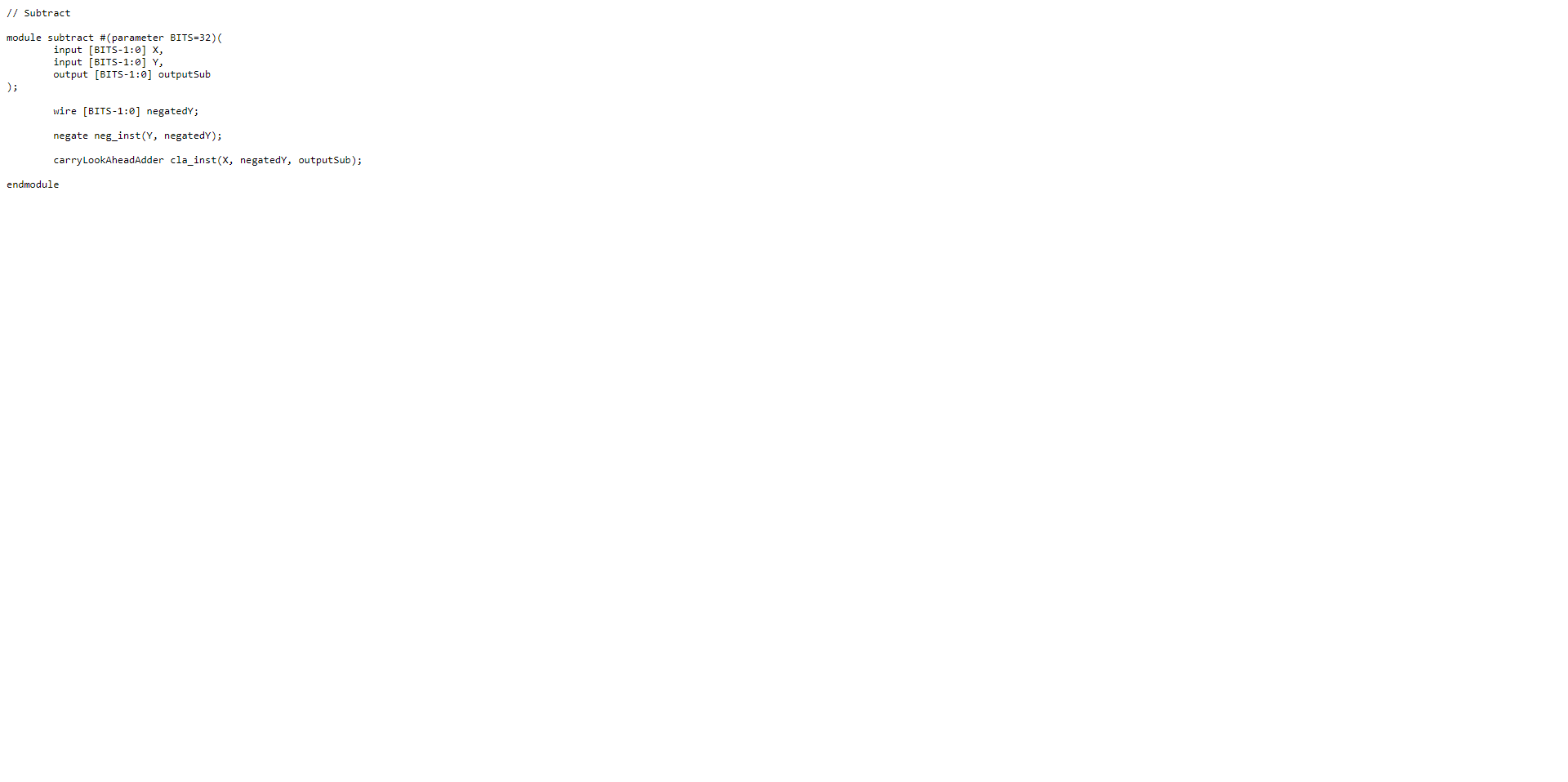
## CLA Adder



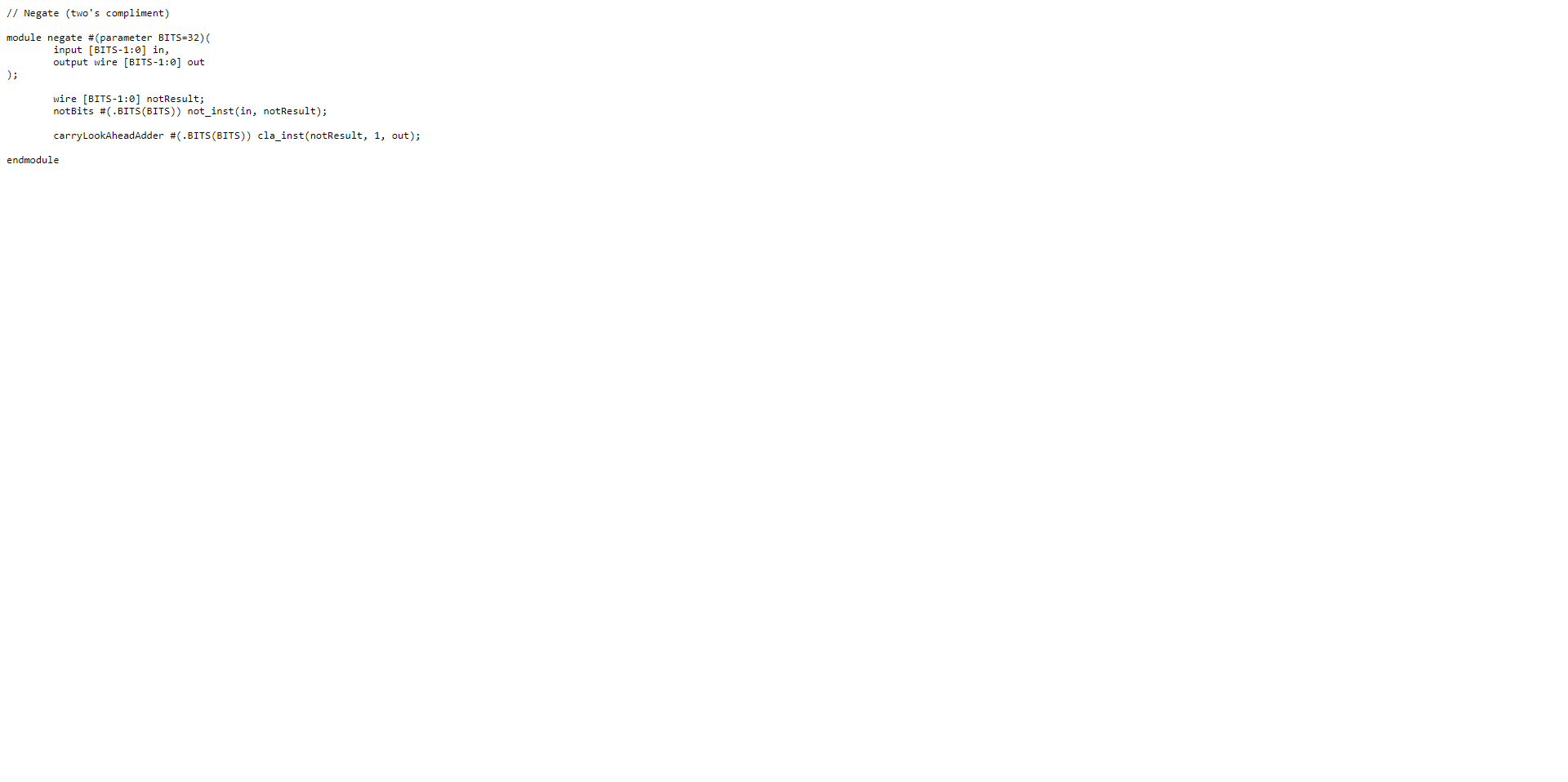
## CLA Full Adder



## Subtract



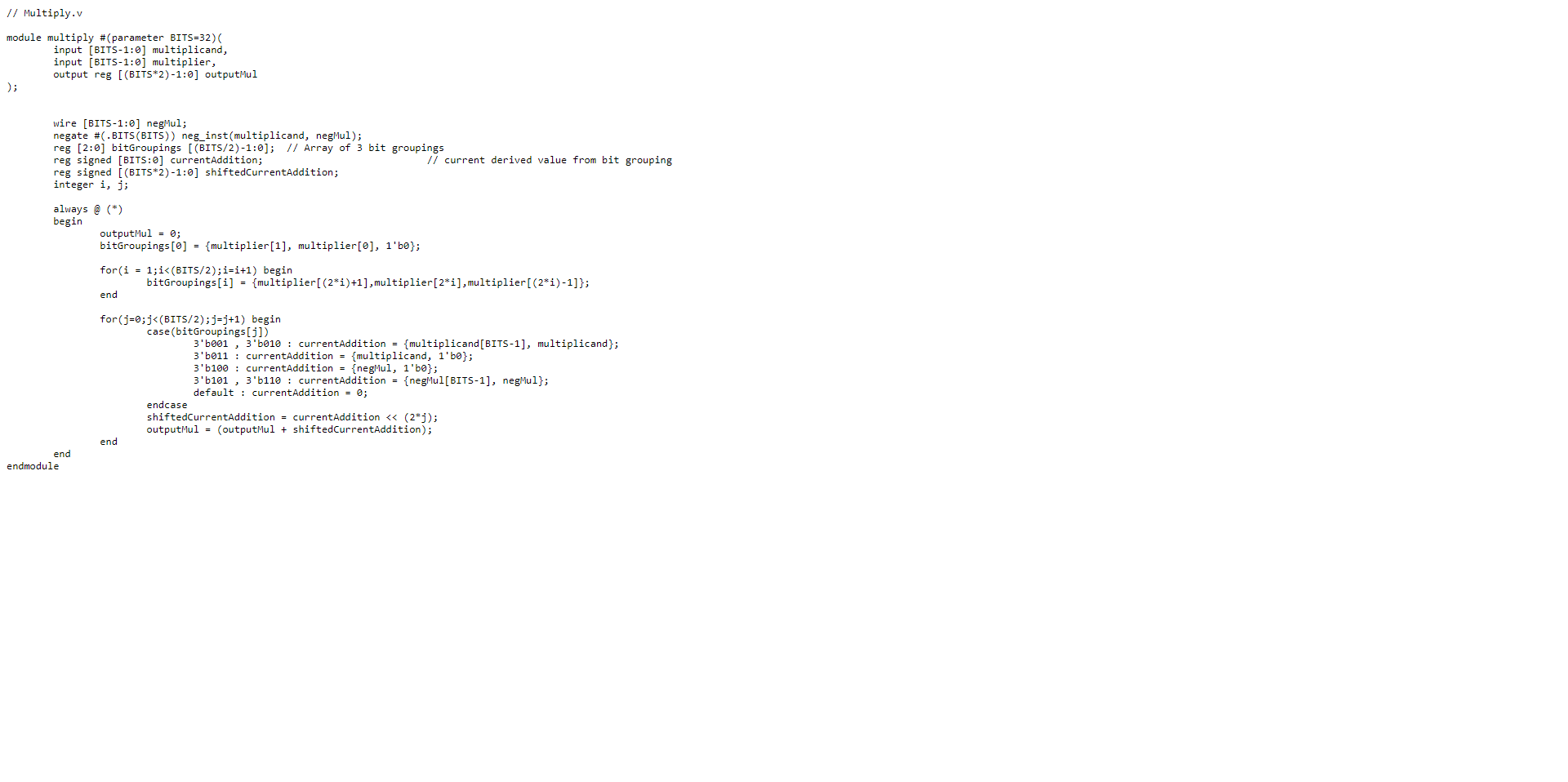
## Negate



## Not



## Multiply



## Division



## Shift Right



## Shift left



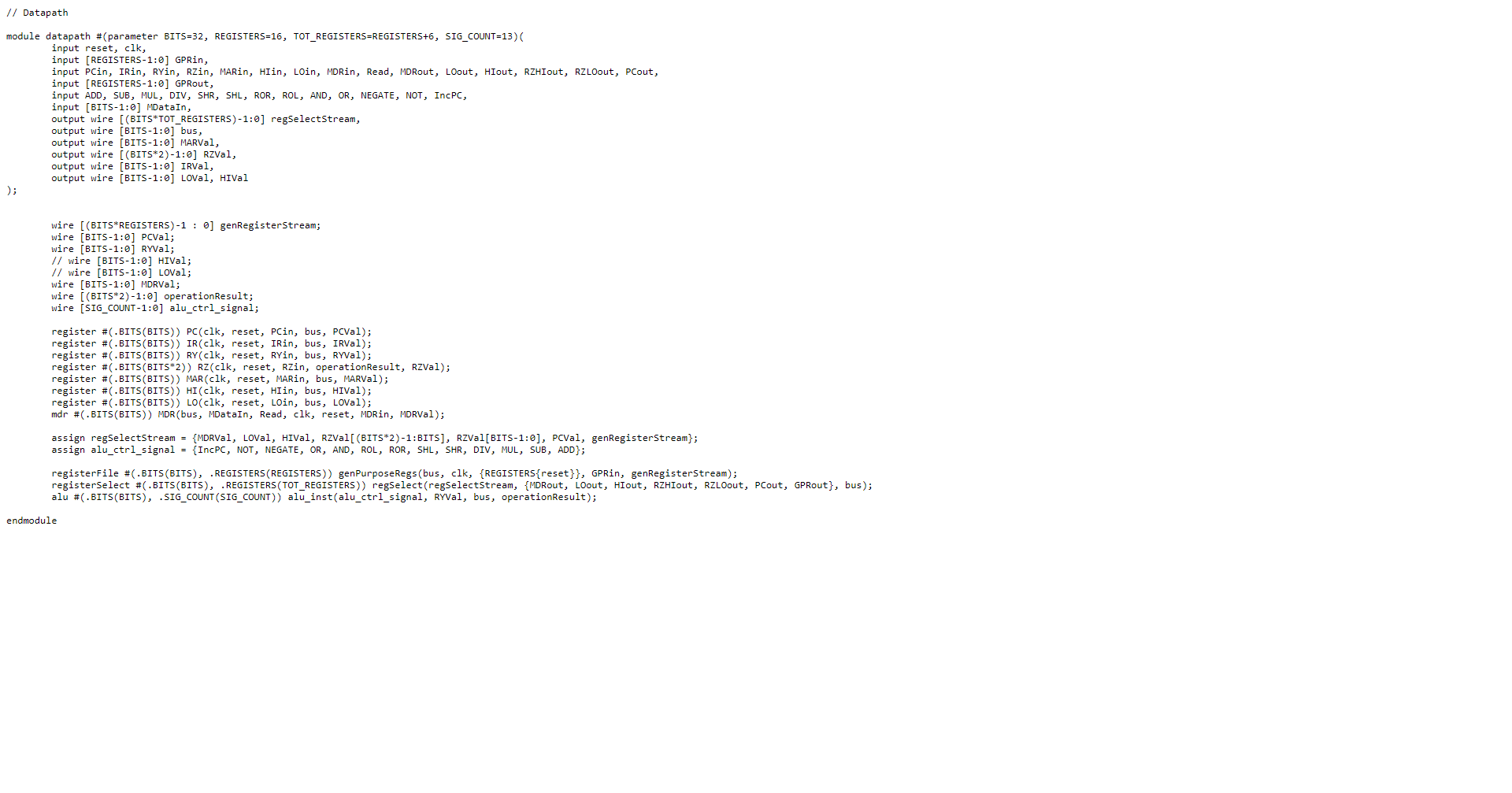
## Rotate Right



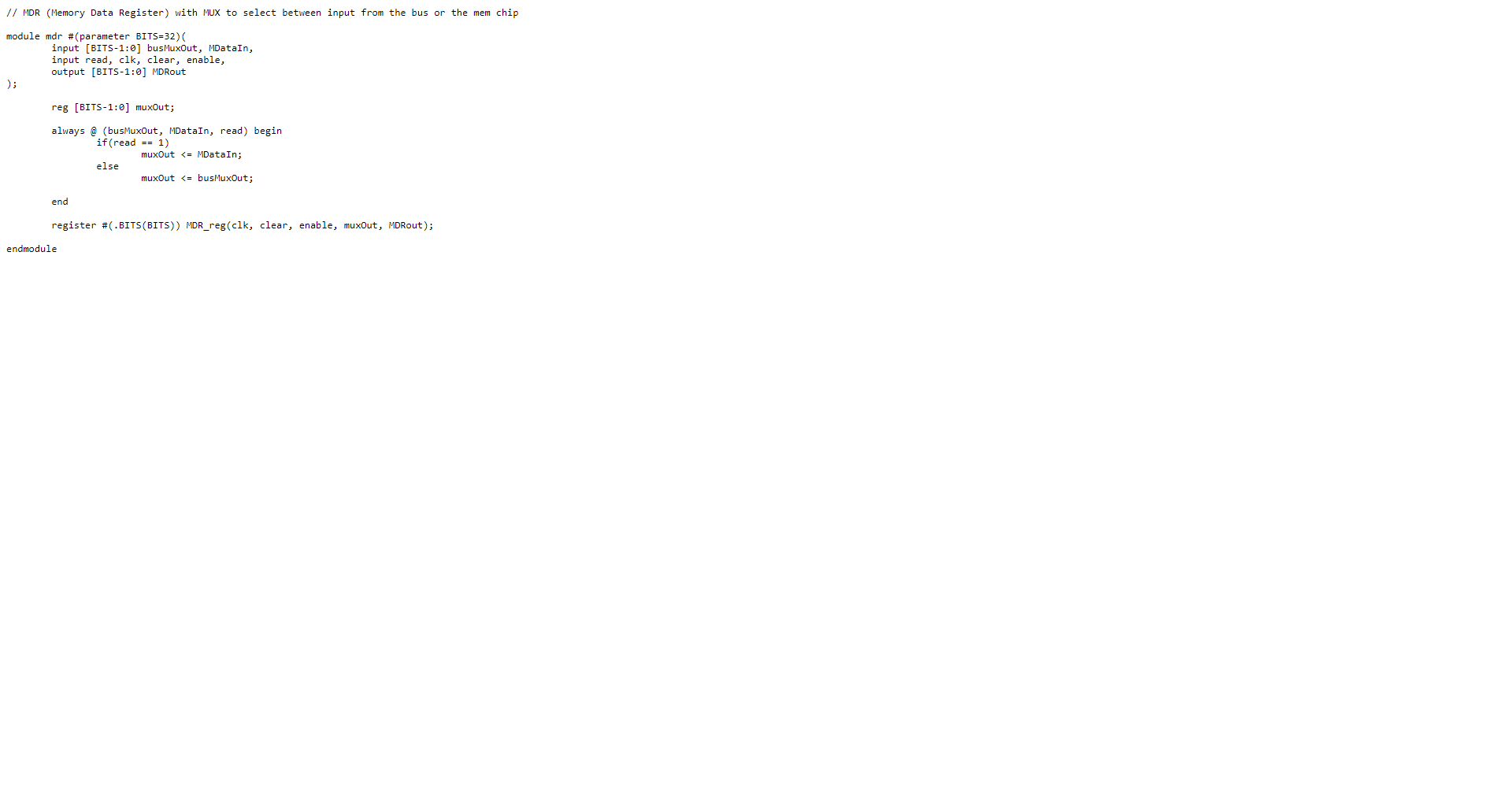
## Rotate Left



## Datapath



## MDR

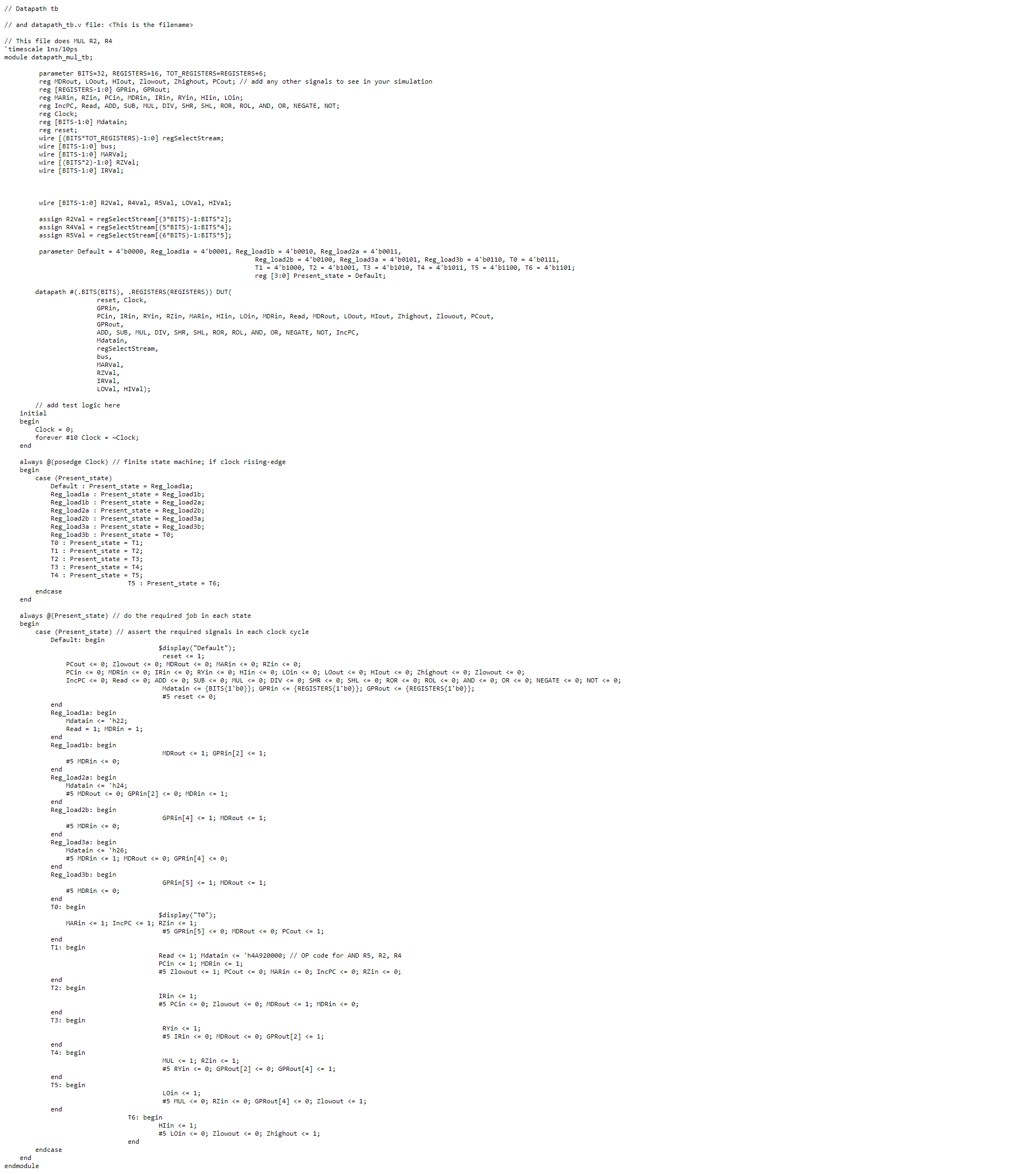


## Datapath Testbench (Tests ALU along with the bus and registers)

The datapath testbench shown is for the AND operation. However, the testbench for the different ALU operations are identical, with the difference being the control signal which chooses operation. The other difference is for multiply and divide as they require double sized registers for result and the HI and LO registers. This testbench is simulated for 32 bits, but the overall design is modular and can simulate 64, 128, and 256-bit sized systems. Additionally the testbench can simulate with N amounts of general purpose registers.



## Datapath Testbench Multiply (Tests 2xbits bit Multiplication and Division)



## ALU Testbench (Tests all ALU operations)



## A screenshot of a computer Description automatically generatedDatapath AND Waveform

## Datapath MUL Testbench

## ALU Testbench