Simple CPU design

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Refer to figure 3.2--computer components: top-level view
Data and instructions stored in single read-write memory
Contents of memory addressable by location (regardless of data contained)

CPU exchanges data with memory. Makes use of two registers: MAR and MBR

- Memory address register (MAR)
  - Specifies the address in memory for the next read or write
- Memory Buffer Register (MBR)
  - Contains the data to be written into memory or receives data read from memory
- Have similar registers for I/O that does the same thing

Bus- a communication pathway connecting two or more devices
- Shared transmission medium
  - Multiple devices all connected by same bus can share transmitted signal
  - Only one device at a time can transmit

<u>Types of Buses</u>
- System bus - connects major computer components like processor, memory, I/O
  - 3 functional groups: Data lines, Address lines, control lines
    - Data lines: provide a path for moving data among system modules
    - Address lines: used to designate the source or destination of the data on the bus
    - Control lines: used to control access to and use of the data and address lines
      - Memory write, memory read, Transfer ACL, interrupt request, etc

INSTRUCTION CYCLE
Basic instruction cycle broken down into two steps: fetch and execute

Interrupt - a mechanism by which other modules can disrupt the normal processing of the processor. Classes of interrupts include:
- Program: generate by a condition that occurs as a result of instruction execution
  - Overflow, division by zero, illegal machine instruction, etc
- Timer: generated by a timer within the processor
  - Perform certain functions on a regular basis
- I/O: generated by I/O controller
  - Completion of operation, variety of error conditions, etc
- Hardware failure: power failure or memory parity error

When interrupt occurs, the processor:
- Suspends operation
- Branches off to program service, known as **interrupt handler**
- Resumes original execution