ECE 341 (Required or Elective)
Digital System Design
Fall 2015

Course (catalog) description:

Tools and methodologies for top-down design of complex digital systems. Important topics include minimization, mixed logic, algorithmic state machines, microprogrammed controllers, creating & using a gold model, data & control path design, and data movement & routing via buses. Design methodologies covered include managing the design process from concept to implementation, gold model validation, and introduction to design flow. A hardware description language is used extensively to demonstrate models & methodologies, and is also used in design exercises & projects. (offered fall, spring)

Prerequisites: ECE 241 (C or better) or ECE 340.
Corequisites:

Texbook(s) and/or other required materials:

C. H. Roth, Jr., and L. K. John, *Digital Systems Design Using VHDL*, Second Edition, Toronto: Thompson Learning, 2008.

Course Learning Objectives:

1. Develop proficiency in modeling digital systems with VHDL
2. Understand mixed logic design, flip-flop design, POS forms, state minimization
3. Design using algorithmic state machine methods
4. Controller design using structured design approaches including one-hot and microcoded controllers
5. Modeling datapath components including registers, counters, ALUs
6. Create datapath to model complex digital systems
7. Control path design
8. Introduction to FPGA design flow
9. Introduction to CPU design

Topics Covered:

Topic	Periods	Text Sections
I. COURSE INTRODUCTION	1	---
A. Course Overview		
B. Curriculum Overview		
C. Course Format and Policies		
II. ECE 241 Recap	1	---
III. INTRODUCTION TO VHDL	6	2.1-2.16
A. Modeling digital systems with VHDL		
B. Concurrent signal assignments		
C. Processes, sequential statements, and delay models		
D. Introduction to design flow		
IV. TOPICS IN LOGIC DESIGN	6	---
A. POS Forms and Design		
B. Mixed-Logic Design		
C. SR, T, and JK Flip-Flop Design		
D. State Minimization		

V. STATE MACHINE & CONTROLLER DESIGN	6	5.1-5.5,6.9 3.2,3.4
A. State machine diagrams		
B. one hot finite state machine design		
C. microcoded controller design		
VI. SYSTEM MODELING WITH VHDL	6	6.11,6.12
A. Introduction to FPGA Design flow		
B. Modeling levels of abstraction		
C. Gold model regression testing		
VII. DATAPATH DESIGN	6	4.3,4.8,4.10
A. Components, registers, counters, etc		
B. Fast adders		
C. multipliers		
D. buses and data movement		
VIII. SELECTED TOPICS IN VHDL	3	8.1-8.12
A. Functions, procedures, and packages		
B. Attributes, IEEE STD_LOGIC		
C. Named associations and generate		
D. File I/O		
IX. INTRODUCTION TO CPU DESIGN	3	9.1-9.5
X. IN CLASS TESTS	2	
XI. SUMMARY AND WRAP-UP	1	

Class Schedule: MWF Three times a week. Ordering of above topics may vary.
Each class is 50 minutes duration.

Engineering Science Hours: 2 Engineering Design Hours: 1

Relationship of the course to Program Outcomes:

1. An ability to identify, formulate, and solve computer engineering problems (Outcome 5).
2. An ability to use the techniques, skills, and modern engineering tools necessary for computer engineering practice (Outcome 11).

Grading:

Homework	15%
VHDL Programming	20%*
Tests (2)	30%
Project	20%
Final exam	15%

*Satisfactory performance required to receive a passing grade in the class.

Prepared by: Lee A. Belfore II

Signature and Date: _____