Initialize signals
Op, OpSave in Sens list, RH:/RLO?

Wait State } Sync process

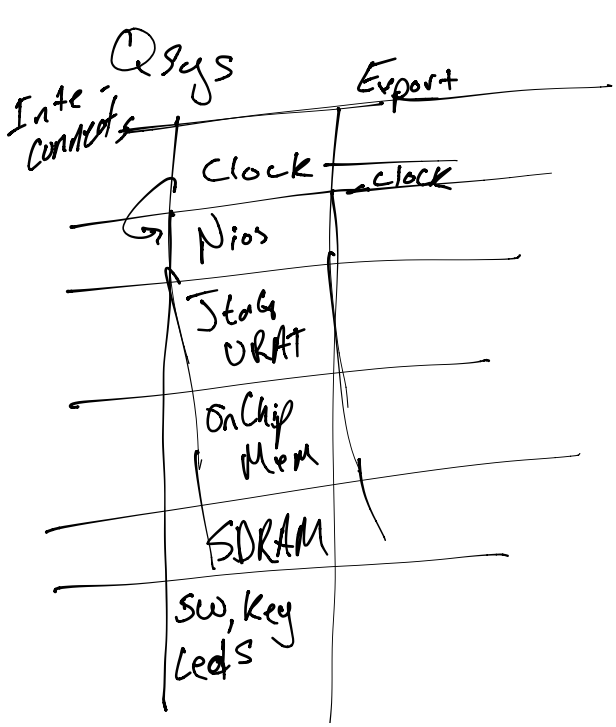
Save <= Op

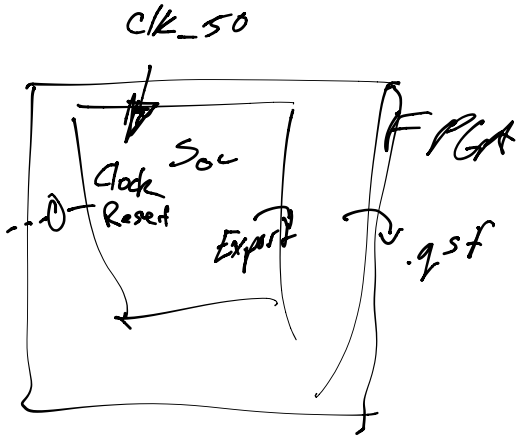
MF?

State

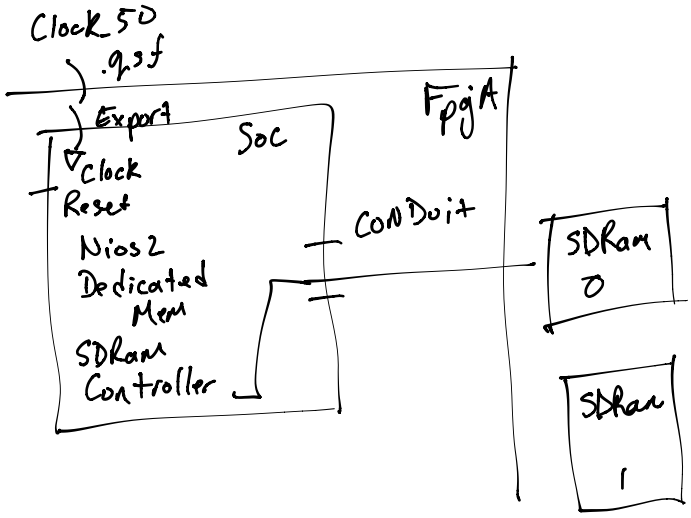
MFhi then ALU_Result MF(63..32)

Load MF of side of state 2 JTAG (SW Debug)





3 ns lead time for SDRam Memory



Embedded

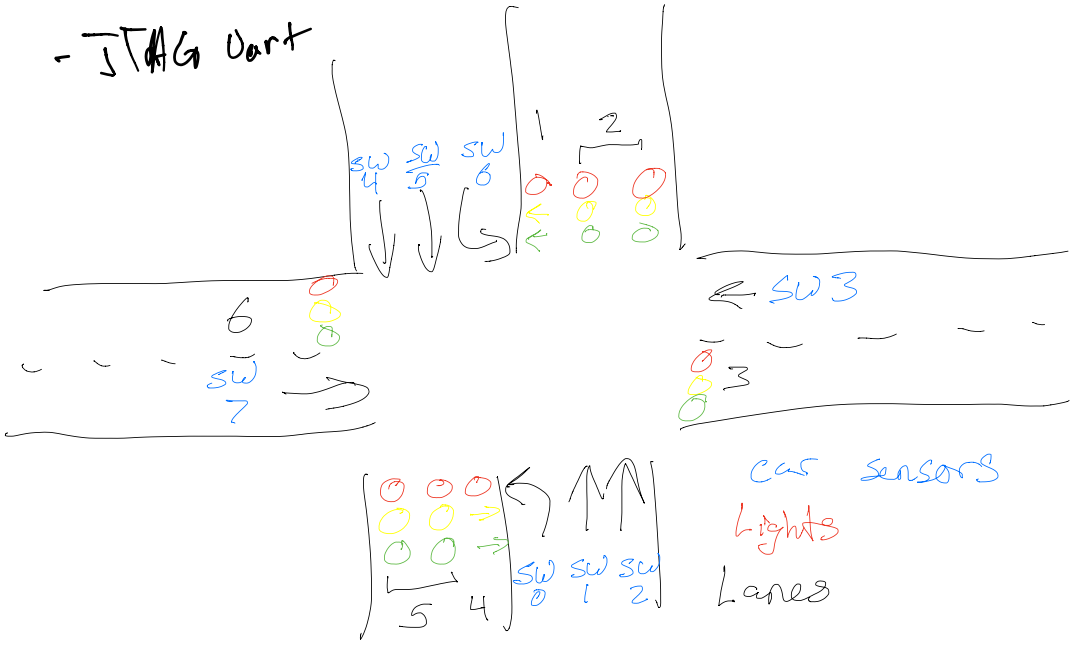
- Nios

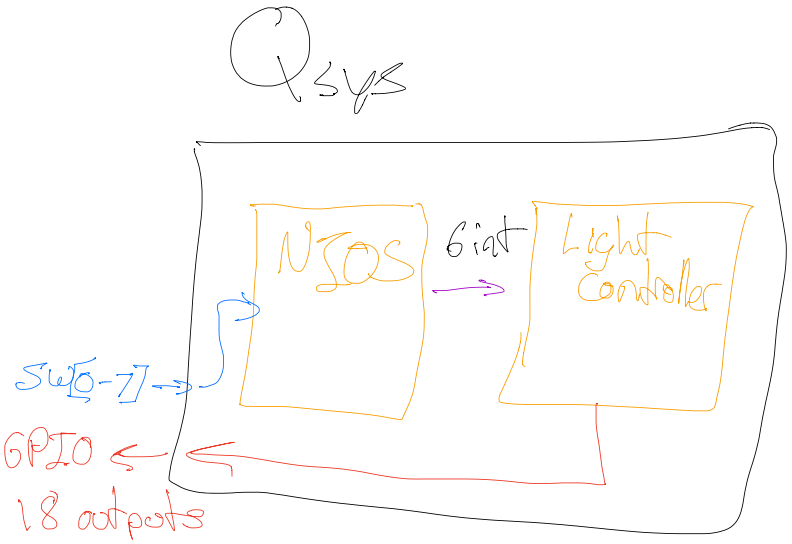
Periph

- PIO

Serial

- JTAG Uart





Light controller takes 6 integers 0, 1, 2 and turns them into logic bits for the lights

* The 2 lights will turn ~~off~~ some driver