4-Bit Multiplier Implementation in 0.35μm AMS CMOS Technology

EE30121 - Coursework

Name: Daniel Sipthorpe
Student ID: drs46
University of Bath
Department of Electrical and Electronic Engineering

September 16, 2025

Contents

1 Introduction

IC CMOS design is an essential skill in modern electronics. It integrates millions of components on a singular small chip reducing size , power consumption all while increasing speed and performance. It drives modern electronic advancement and is necessary for future innovation of electronics.

This report details the steps and procedures taken to implement a 4-bit binary multiplier in 0.35 μm AMS CMOS technology.

The design process of such building blocks is critical to a circuits functionality and can affect a systems performance in a wide manner such as accuracy , scalability and efficiency. Throughout the design process, a key emphasis is placed on the iterative process taken at each stage ensuring the full functionality and quality of every subsystem used in the wider design. This design technique also benefits in identifying and resolving potential design issues by ensuring schematic is fully operational with rigorous simulation and layout fully adheres to the tested schematic

2 Design Process

2.1 Full Adder

The first part of the full adder to be designed and the most fundamental building block of the four bit multiplier was the half adder (figure 1 and 2).

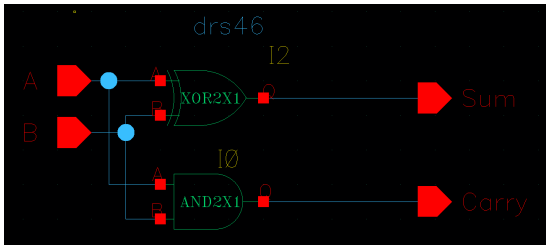

Figure 1: Half adder schematic

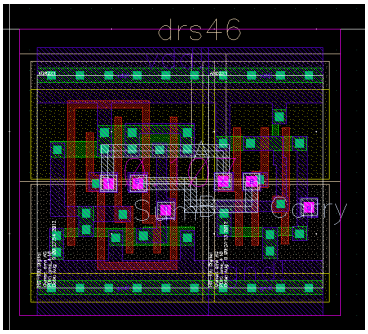

Figure 2: Half adder layout

The half adder has two inputs A and B and outputs the result (sum) of the two bits and the carry bit.

The cell layout has been done using internal routing to allow for vertical and horizontal bunting in larger designs with minimal bends in metal two to minimize delay and congestion

2.1.1 Schematic and Simulation

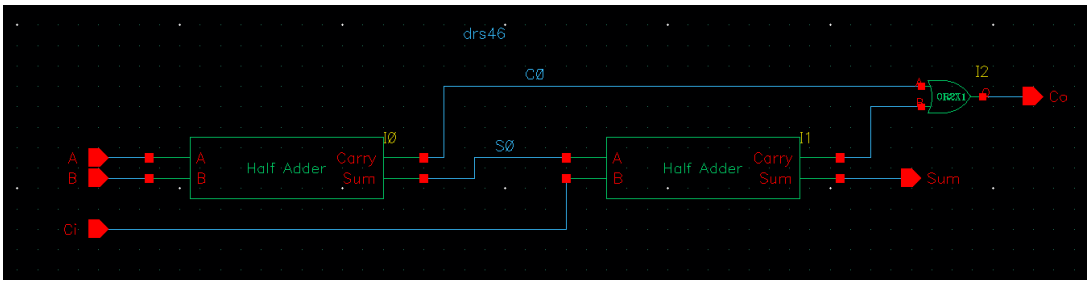

Figure 3: Full Adder Schematic

The full adder (figure 3) is an extension of the half adder made of two half adders and one OR gate. three binary bits can be inputted (two data bits and one carry input bit) and much like the half adder two bits are outputted (sum and carry). It is imperative in the design of a 4 bit multiplier and the layout of it will undoubtedly affect the performance of the final circuit

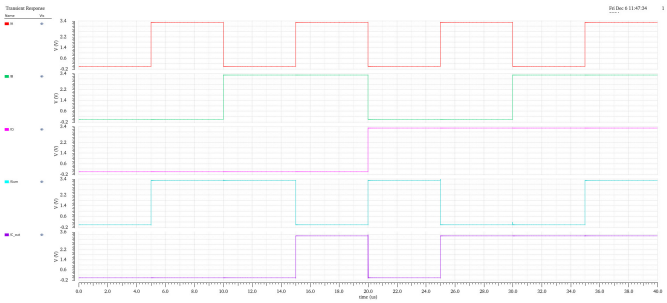

Figure 4: Full adder simulation

Inputs			Outputs	
A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Figure 5: Full Adder Truth Table

The circuit was then tested in a test bench by applying a series of signals on all inputs to simulate all possible conditions (figure 4) . It is imperative to implement rigorous testing throughout in order to ease fault finding in larger designs. It can be seen (figure 5) that the correct binary addition of the two inputs bit was performed with no errors.

2.1.2 Layout Design

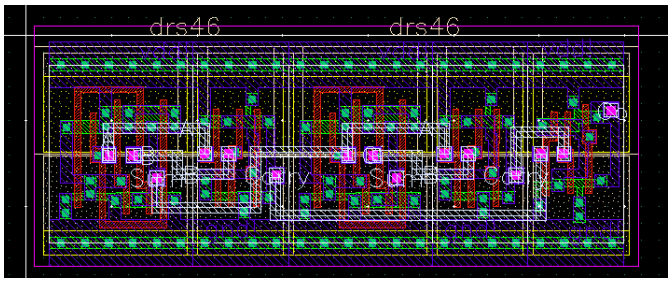

Figure 6: Full Adder Layout

the design (figure 6) has been implemented by bunting horizontally all cells. Doing this provides robust power delivery and a stable ground reference providing a better resistance to potential shifts in ground level due to current flow.

Internal routing has been chosen, reducing area of the design and allowing shorter traces to be used thus easing congestion and minimizing delay. It should also be noted due to the digital nature and architecture size the induced capacitance and inductance are negligible in the performance. Making all connections internal also makes the cell scalable to larger systems.

All connections have been made on metal two with a single via to metal one. Using just one layer adheres to standardization and allows all other metal layers to be used for wider vertical and horizontal global connections. Likewise, without these multiple layers, there will be very little to no crosstalk present between the layers leaning to clearer signal transfer. In addition to this, it reduces the material and processing costs making it more economical and manufacturable.

Figure 7: Full Adder DRC Pass

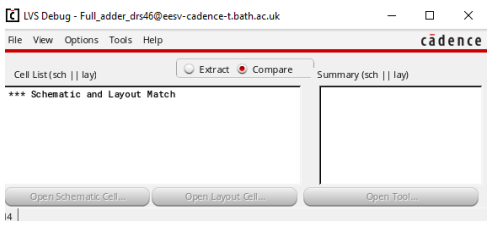

Figure 8: Full Adder LVS Pass

The functional validity of the layout was then assessed through the DRC and LVS tests (figure 7 and 8). The DRC (design rules check) ensures layout matches predefined set of rules depending on architecture such as minimum spacing , width , density etc and the LVS (layout vs schematic) compares the layout to the schematic ensuring if perfectly matches the known working schematic .

It can be seen in figure 7 that some DRC warnings are present these simply state that there isn't a high enough density of polymer one and metal two layers. These do not matter for the cell design but would need to be fixed in a larger design to be built by simply adding more of both to the design.

2.2 4 Bit Full Adder

2.2.1 Schematic And Simulation

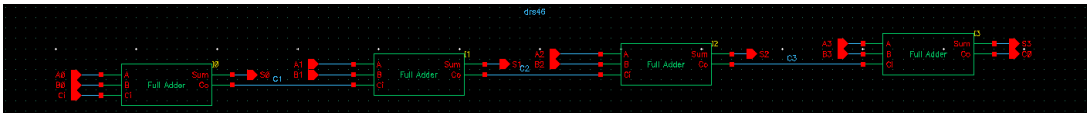

Figure 9: 4 bit Full Adder Schematic

The next building block created was the four bit full adder created by connecting four full adders (figure 9) which for any two four bit binary inputs it will output the binary addition including the carry bit.

The circuit was then tested in a test bench simulating every variation of input.

Figure 10: 4 bit Full Adder Simulation snapshot (adding by 1 and 2)

INPUT									OUTPUT					
Ci	A0	A1	A2	A3	B0	B1	B2	B3	S0	S1	S2	S3	Co	Decimal
1	0	0	0	0	1	0	0	0	0	1	0	0	0	0+1+1 = 2
1	1	0	0	0	1	0	0	0	1	1	0	0	0	1+1+1 = 3
1	0	1	0	0	1	0	0	0	0	0	1	0	0	1+2+1 = 4
1	1	1	0	0	1	0	0	0	1	0	1	0	0	1+3+1 = 5
1	1	1	1	1	1	0	0	0	1	0	0	0	1	1+15+1 = 1 with 1 carry
1	0	0	0	0	0	1	0	0	1	1	0	0	0	1+0+2 = 3
1	1	0	0	0	0	1	0	0	0	0	1	0	0	1+1+2 = 4
1	0	1	0	0	0	1	0	0	1	0	1	0	0	1+2+2 = 5
1	1	1	0	0	0	1	0	0	0	1	1	0	0	1+3+2 = 6

Table 1: Truth Table for specific cases in figure 10

It can be seen in the snapshot (figure 10) how the design operates when adding binary 0001 and 0010 (decimal 1 and 2) to any set of inputs with the carry input high. The outputs for a few specific cases can be seen in table 1, specifically noting the output where the carry output is correctly high for an overflow in the four bit addition. The design worked for every possible input combination thus the design was proven to be functional.

It can be seen that there it some transient spikes in the outputs where the circuit falsely changes state this is a result of a timing issue and the circuit not reaching steady state and cannot be avoided and can be ignored when investigating the functionality of the circuit.

2.2.2 Layout Design

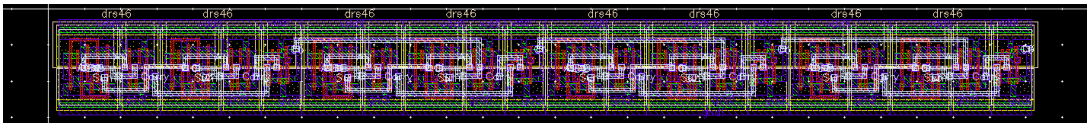

Figure 11: 4 bit Full Adder Layout

When designing the layout for the four bit full adder, several considerations were made including routing, modularity, area efficiency , noise and parasitics.

Forwarding from the previously designed standard in the full adder, internal routing has been used to complete the design all on the singular metal two layer minimizing crosstalk that would be present with extra metal layers (albeit minimal).

The circuit requires a lot more inputs and outputs than the singular full adder. However, since the four bit is such a relatively small cell they would still be easily accessible without any issue thus a simple via has been placed on all inputs/outputs which can be later connected to.

The four full adders have been bunted together horizontally, continuing the well establish ground connection. Even with the extra metal traces parasitics, digital congestion and bottle neck will be kept to a minimum and could arguably be negligible.

Doing the full adder design in this manner saves on the area of design whilst still allowing easy implementation and scalability into a wider design. Very useful for the four bit multiplier which introduces a large amount of logic gates.

Figure 12: 4 bit Full Adder DRC Pass

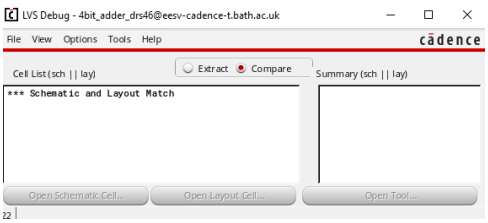

Figure 13: 4 Bit Full Adder LVS Pass

The layout was then tested using both identical DRC and LVS tests as previously defined (figure 12 and 13) where it can be seen that the design both perfectly matches the working schematic and adheres to all defined design rules.

2.3 4 Bit multiplier

2.3.1 Schematic And Simulation

Using the collection of all cells defined throughout , the four bit multiplier could be created. It consists of three four bit adders and sixteen logic AND gates in order to multiply two four bit binary inputs (figure 14)

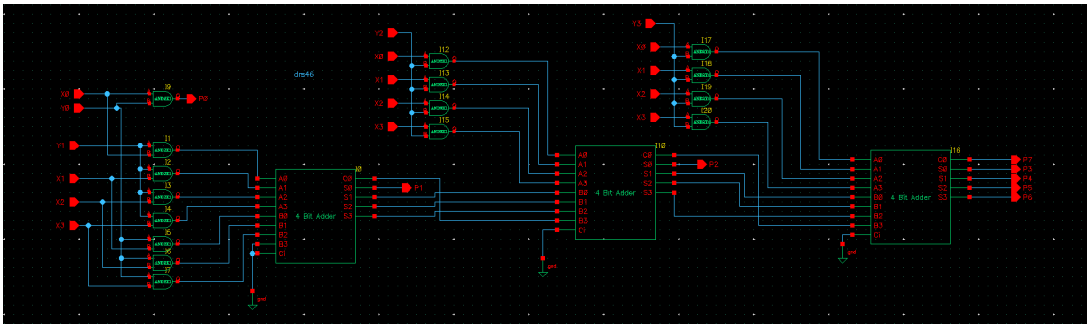

Figure 14: 4 bit Multiplier Circuit

It can be seen in the schematic why the design choices made in both the four bit and singular full adder were made and would allow for an easy implementation of a more complex design.

Metal layers greater than two have not been utilized at all and can be used as vertical and horizontal global connections while causing minimal crosstalk within the cells themselves.

It should be noted that both channel routing and internal routing would have to be used for the multiplier to make a valid, compact design.

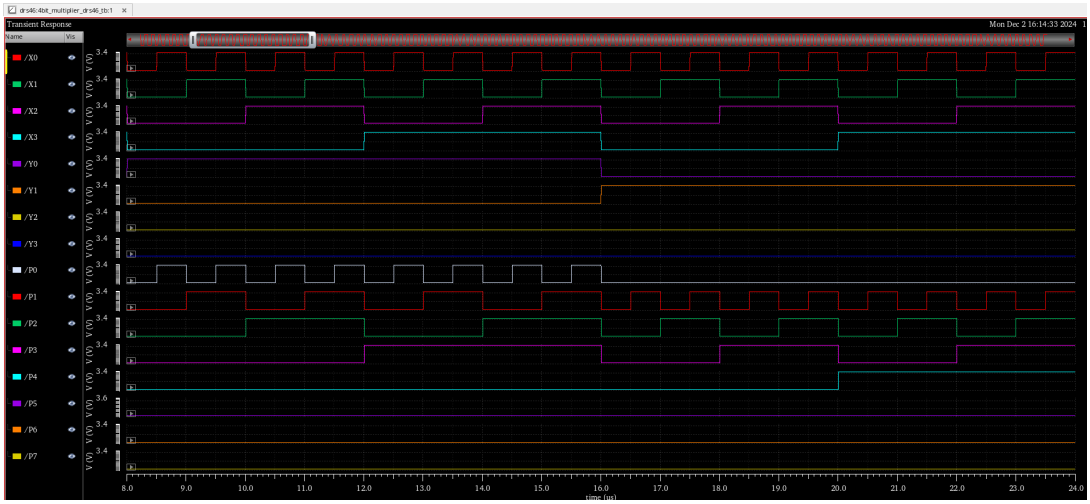

Figure 15: Multiplier Simulation (by 1 and 2)

INPUT								OUTPUT								
X0	X1	X2	X3	Y0	Y1	Y2	Y3	P0	P1	P2	P3	P4	P5	P6	P7	Decimal
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0x1 = 0
1	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1x1 = 1
0	1	0	0	1	0	0	0	0	1	0	0	0	0	0	0	2x1 = 2
1	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	1x2 = 2
0	1	0	0	0	1	0	0	0	0	1	0	0	0	0	0	2x2 = 4
1	1	0	0	0	1	0	0	0	1	1	0	0	0	0	0	3x2 = 6

Table 2: Truth Table for specific outputs in figure 15

.

The circuit was simulated to show functionality of the design and consequently all building designed up to this point . It can be seen in figure 15 how the multiplier operates for a series of inputs when being multiplied by 0001 (one) and 0010 (two). The truth table (table 2) details how the circuit performs the binary multiplication for a few specific examples in comparison to the decimal calculation.

The circuit did every calculation correctly for all variations of input.

3 Conclusion

In this project a four bit multiplier and a series of adder variations layouts were successfully created. The design process involved considerations of routing strategies, testing and ease of integration into larger systems.

In the design internal routing was chosen over external because it minimizes parasitics and improves signal integrity (thus timing performance). In addition, this routing technique allows the design to be compact which is very useful if the circuit was to be used in a wider high density design. However, channel routing could've been chosen and implemented with some benefits that are not present when done with internal routing.The inputs and outputs are more difficult to access in comparison to external routing which would make the cell harder to be integrated and distribute power. In a larger design such as an ALU the use of channel routing would be nearly impossible to avoid.

The importance of the mass of testing done throughout is crucial. The iterative testing done at each stage allowed faults to easily be found and ensure both schematic and layout is fully operational within specific design rules ensuring the designs are both functional and manufacturable.

This project showed how small modular designs can be integrated into larger systems and how carefully tailoring and changing layouts depending on specifications can create an easy to use and efficient design process.