جامعة بيرزيت

BIRZEIT UNIVERSITY

Faculty of Engineering and Technology

Electrical and Computer Engineering Department

DIGITAL INTEGRATED CIRCUITS– ENCS3330

Assignment No. 2 Report

Buffer and invertor using electric

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Section: 1

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Assignment parts:

Lambda" Design Rules– lambda, λ, = 1/2 minimum feature size

The program has scaling number we have to follow, which is 3µm.

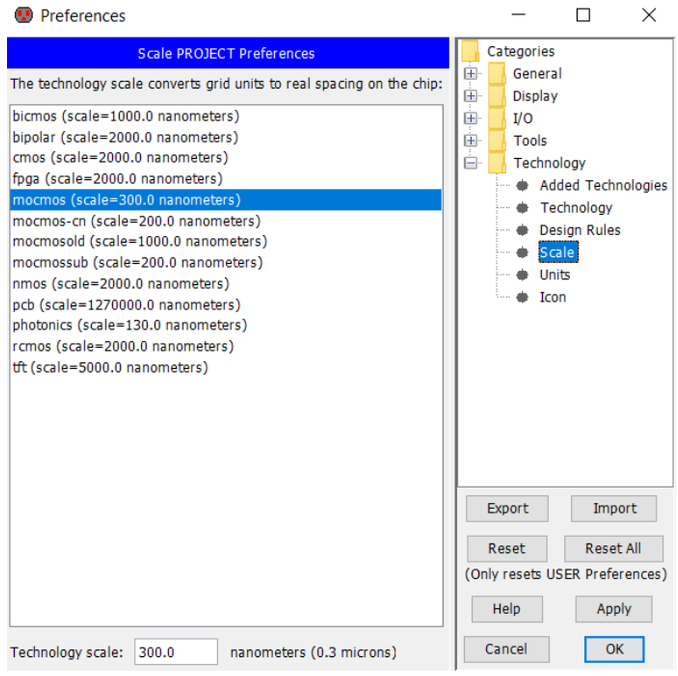


Figure 1 Scales

Part 1: invertor:

1.1 Schematic:

First part is to build an investor with width 10 and length 2. For both NMOS and PMOS as the following:

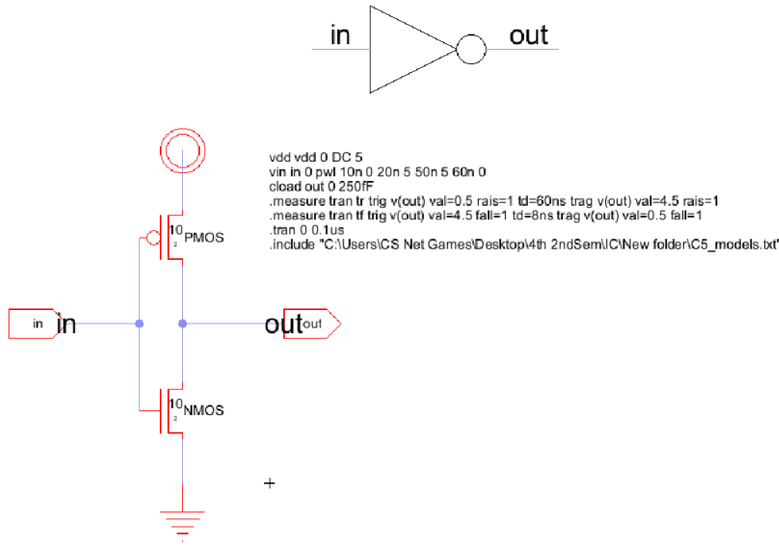


Figure 2 invertor schematic

Simulation:

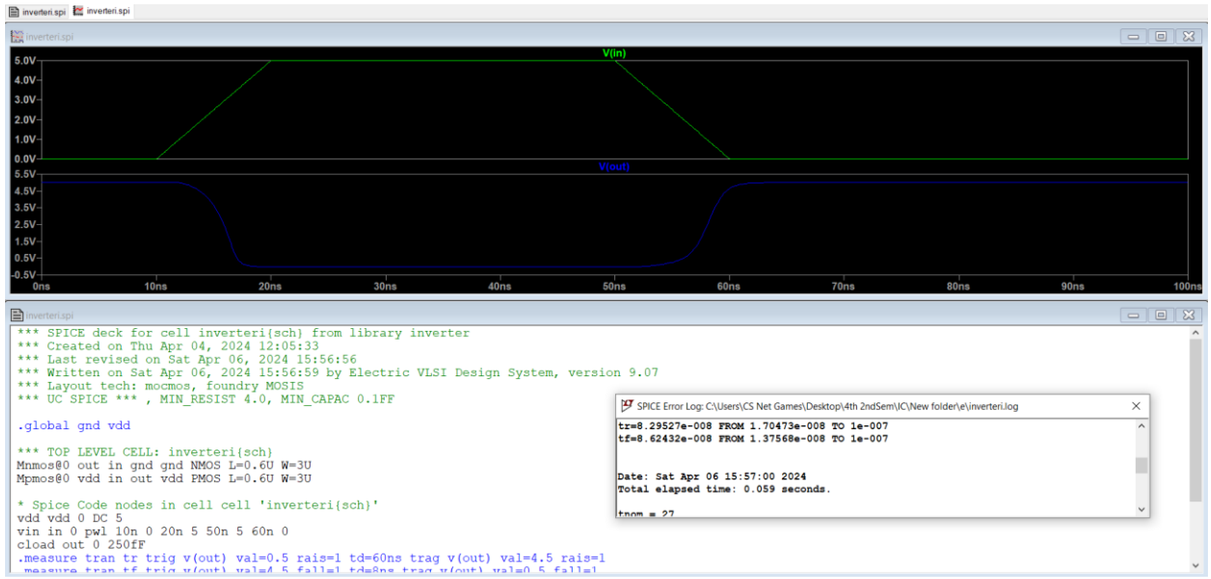


Figure 3 invertor simulation1

Schematic view:

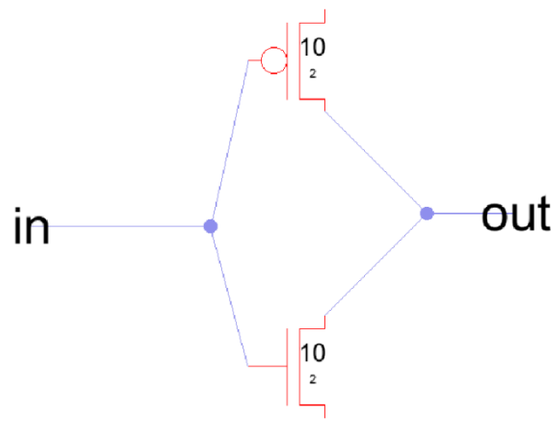


Figure 4 schematic view

1.2 Icon:

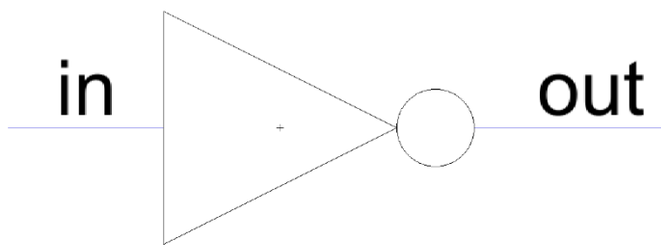


Figure 5 invertor icon

1.3 Layout:

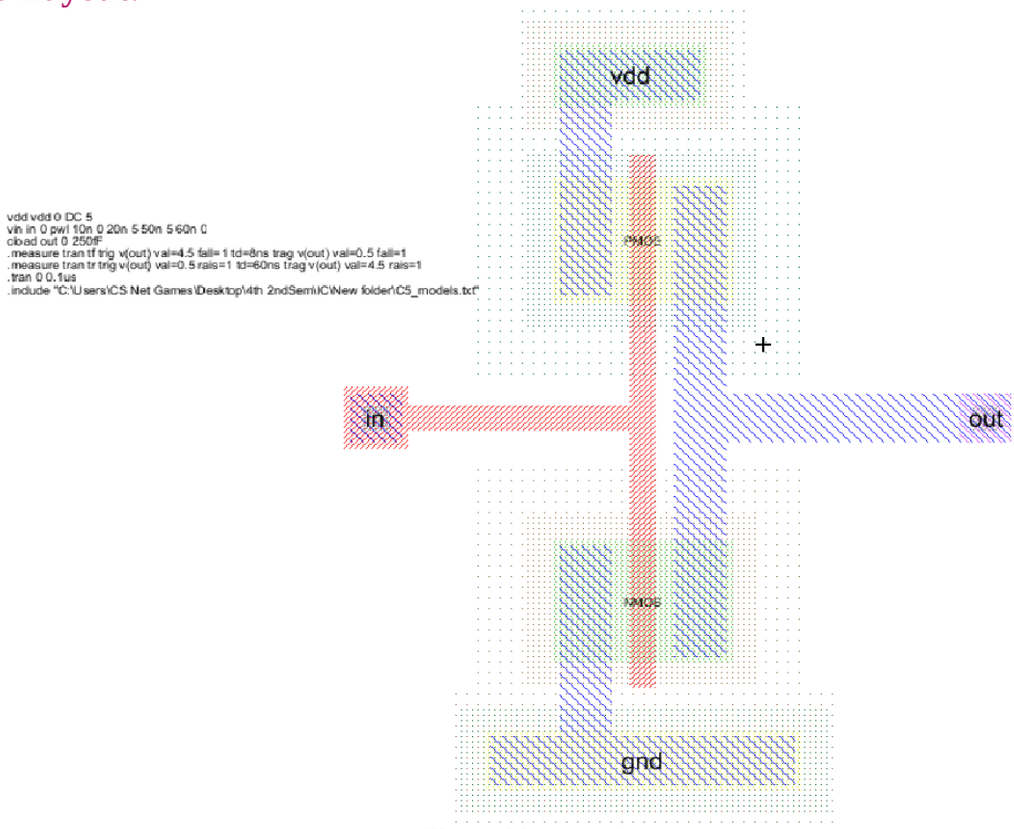


Figure 6 invertor layout

The measurement I used are:

PMOS: 10 width, 2 length, NMOS: 10 width, 2 length.

VDD: 12 length, width 5, as the maximum length is 12 for VDD (nwell).

GND: 25 length, 5 width.

Gate to input: 2 widths.

P, N, Act to output: 4 widths.

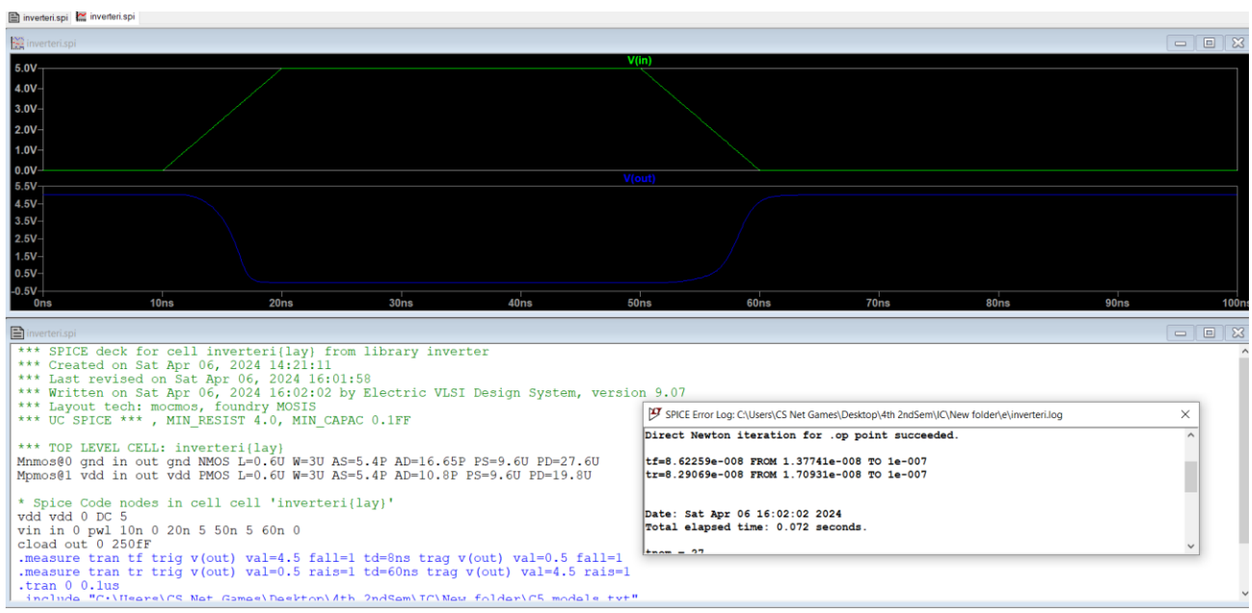


Figure 7 layout simulation:

Layout view:

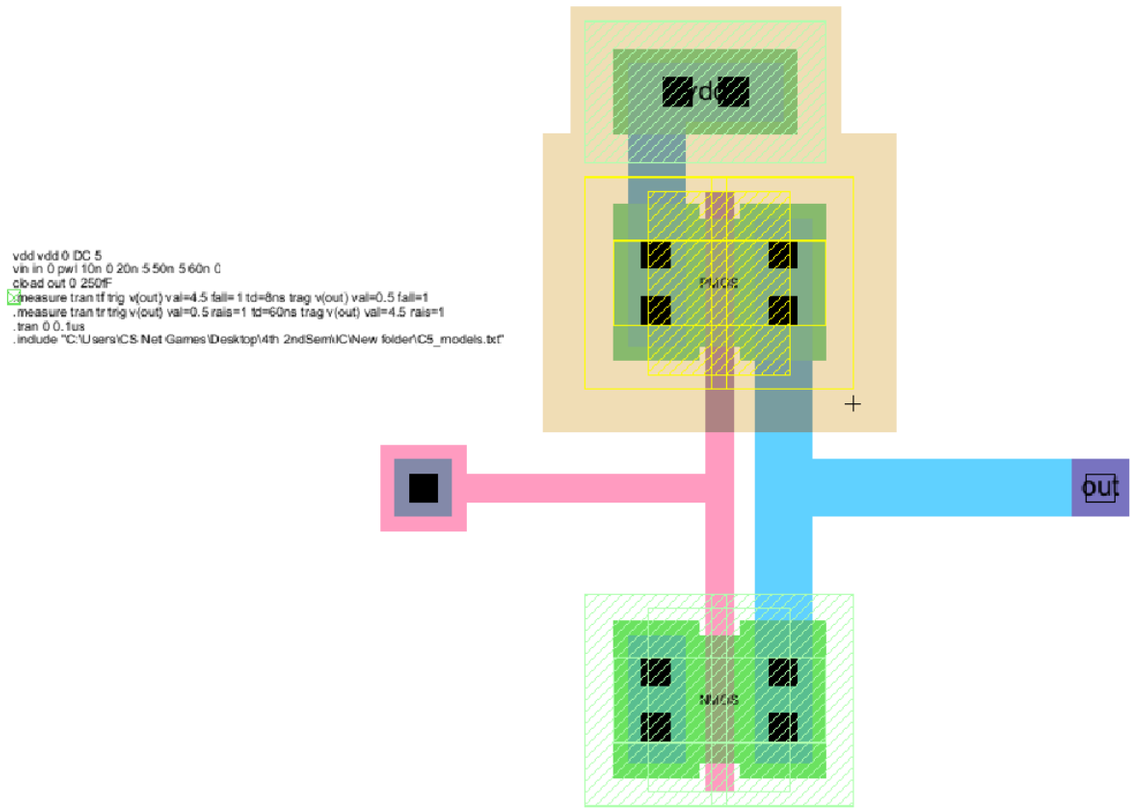


Figure 8 invertor layout view

Error check:

```
Checking Wells and Substrates in 'inverter:inverteri{lay}' ...
   Geometry collection found 8 well pieces, took 0.001 secs
   Geometry analysis used 8 threads and took 0.003 secs
NetValues propagation took 0.0 secs
Checking short circuits in 2 well contacts
   Additional analysis took 0.0 secs
No Well errors found (took 0.004 secs)
================================32================================
Hierarchical NCC every cell in the design: cell 'inverteri{sch}'  cell 'inverteri{lay}'
Comparing: inverter:inverteri{sch} with: inverter:inverteri{lay}
  exports match, topologies match, sizes not checked in 0.001 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.002 seconds.
```

Figure 9 error check for invertor

1.4: buffer using two invertors:

```
vdd vdd 0 DC 5
vin in 0 pwl 10n 0 20n 5 50n 5 60n 0
cload out 0 250fF
.measure tran tf trig v(out) val=4.5 fall=1 td=8ns trag v(out) val=0.5 fall=1
.measure tran tr trig v(out) val=0.5 rais=1 td=50ns trag v(out) val=4.5 rais=1
.tran 0 0.1us
.include "C:\Users\CS Net Games\Desktop\4th 2ndSem\IC\New folder\C5_models.txt"
```

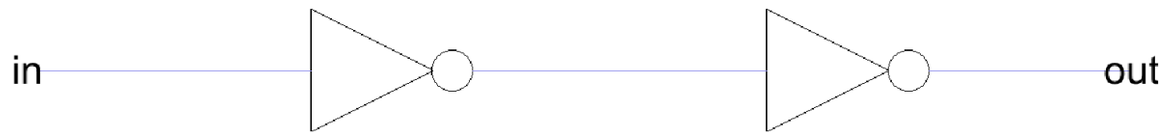


Figure 10 buffer using two invertors

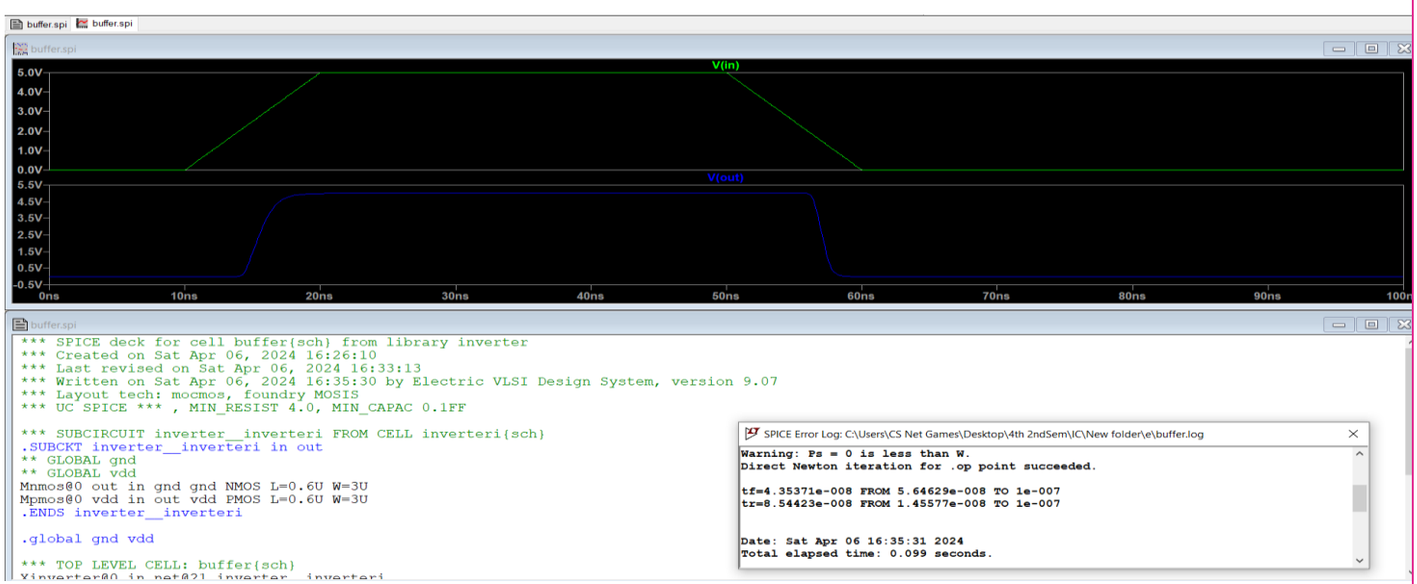


Figure 11 simulation of buffer

Part2: buffer:

1.1 schematic:

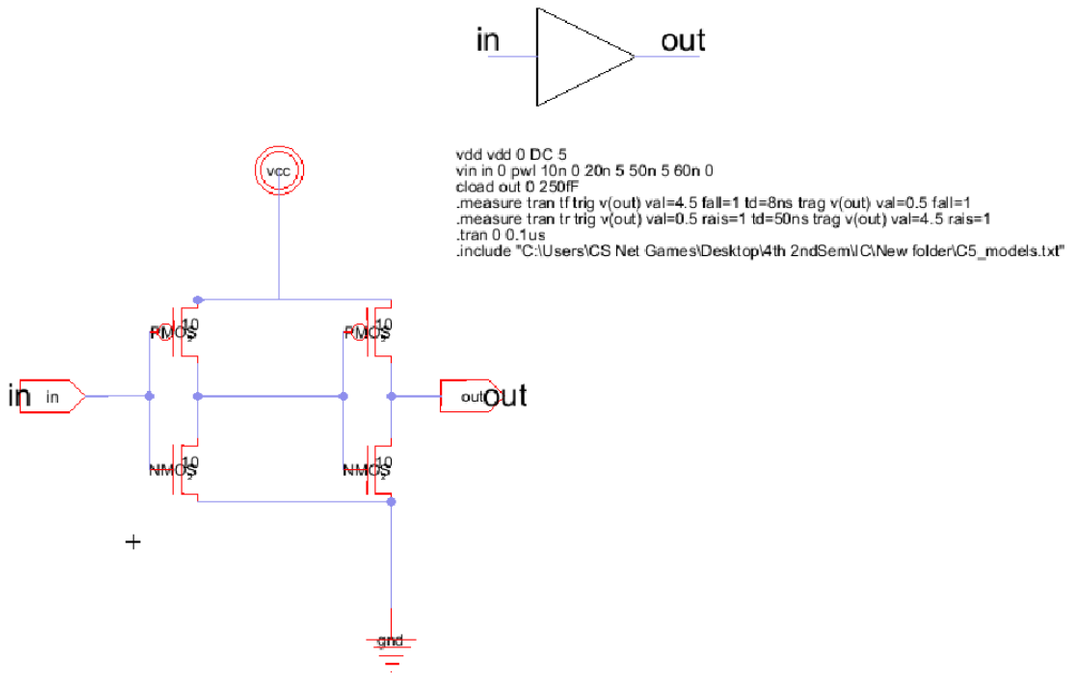


Figure 12 buffer schematic

Simulation:

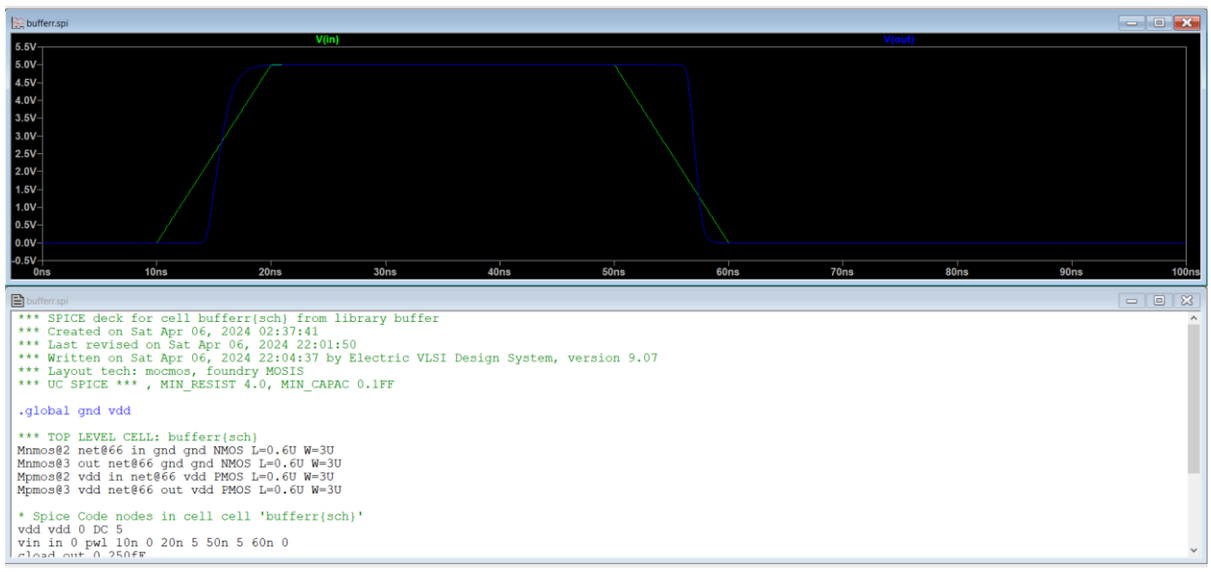


Figure 13 buffer simulation1

Schematic view:

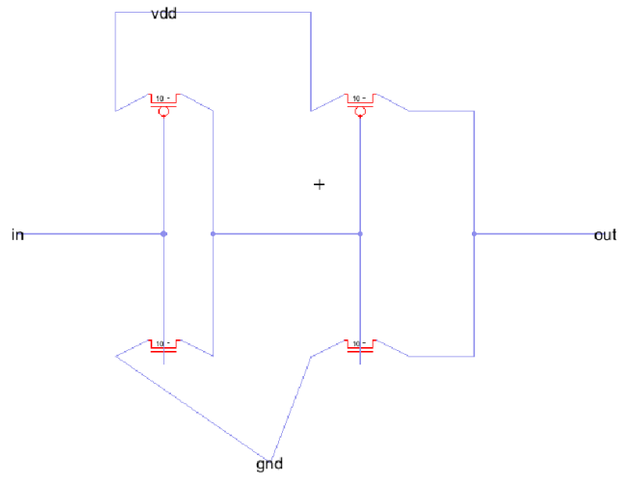


Figure 14 buffer schematic view

1.2 Icon

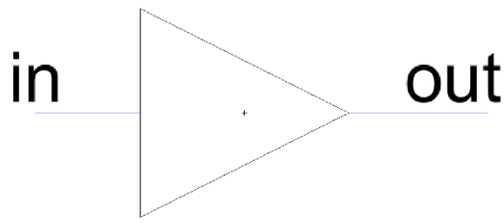
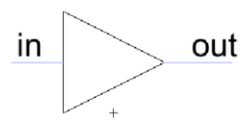


Figure 15 buffer icon

Icon schematic:




```
vdd vdd 0 DC 5
vin in 0 pwl 10n 0 20n 5 50n 5 60n 0
cload out 0 250fF
.measure tran tf trig v(out) val=4.5 fall=1 td=8ns trag v(out) val=0.5 fall=1
.measure tran tr trig v(out) val=0.5 rais=1 td=50ns trag v(out) val=4.5 rais=1
.tran 0 0.1us
.include "C:\Users\CS Net Games\Desktop\4th 2ndSem\IC\New folder\C5_models.txt"
```

Figure 17 schematic as component

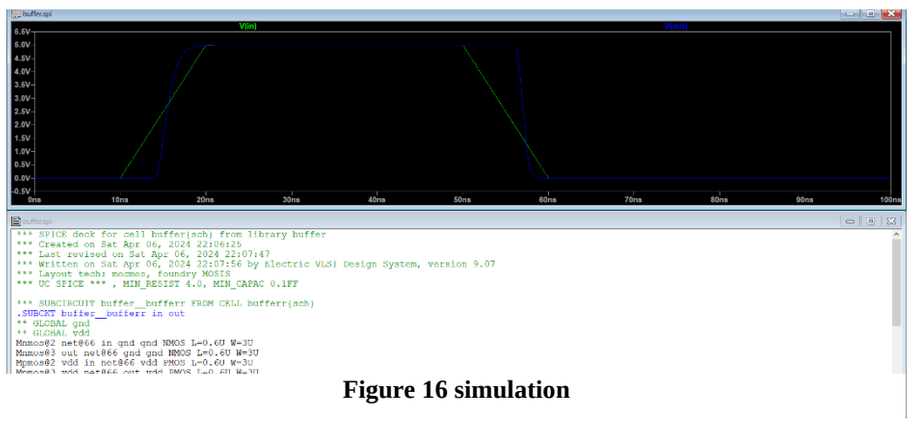


Figure 16 simulation

1.3 layout:

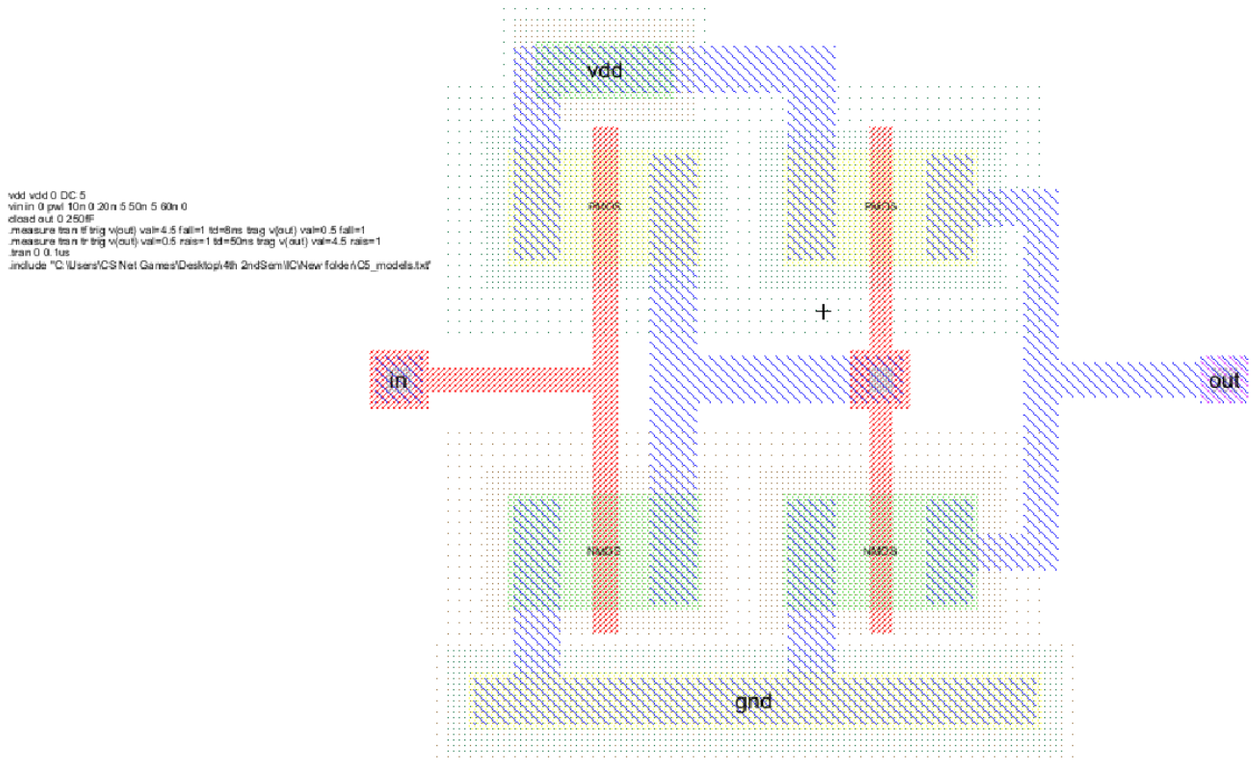


Figure 18 buffer layout

Simulation:

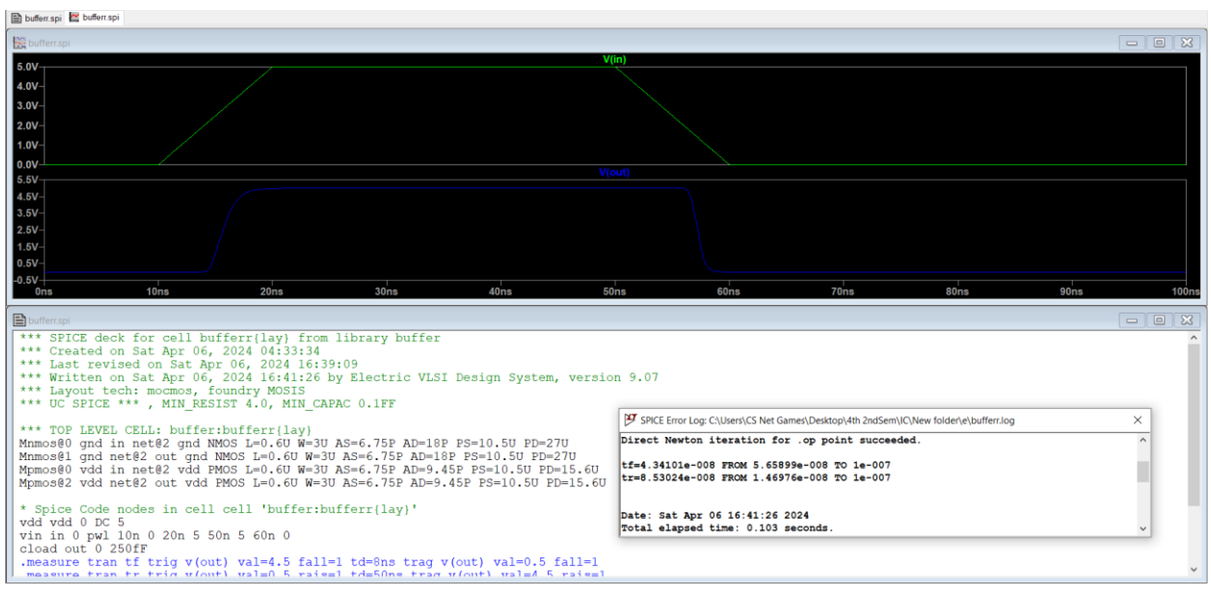


Figure 19 buffer simulation

Layout view:

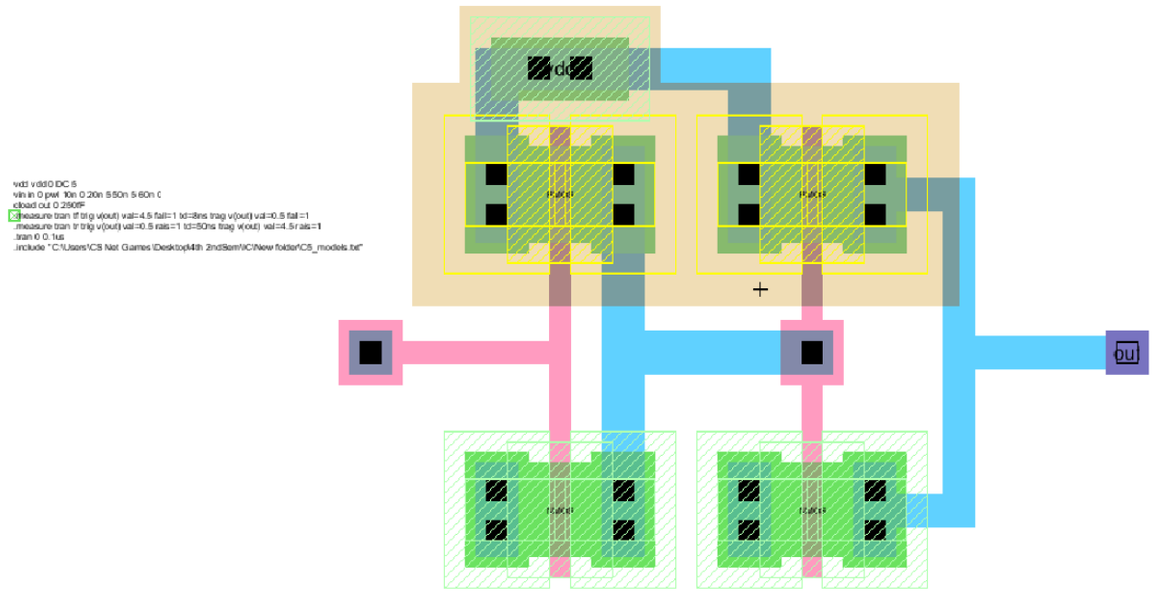


Figure 20 buffer layout view

Error checks:

```
Checking library 'buffer' for repair... library checked
No errors found
================================34================================
Checking Wells and Substrates in 'buffer:bufferr{lay}' ...
   Geometry collection found 22 well pieces, took 0.002 secs
   Geometry analysis used 8 threads and took 0.001 secs
NetValues propagation took 0.001 secs
Checking short circuits in 2 well contacts
   Additional analysis took 0.0 secs
No Well errors found (took 0.004 secs)
================================35================================
Hierarchical NCC every cell in the design: cell 'bufferr{sch}'  cell 'bufferr{lay}'
Comparing: buffer:bufferr{sch} with: buffer:bufferr{lay}
  exports match, topologies match, sizes not checked in 0.002 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.002 seconds.
```

Figure 21 error check for buffer

Code:

```
vdd vdd 0 DC 5
vin in 0 pwl 10n 0 20n 5 50n 5 60n 0
cload out 0 250fF
.measure tran tf trig v(out) val=4.5 fall=1 td=8ns trag v(out) val=0.5 fall=1
.measure tran tr trig v(out) val=0.5 rais=1 td=50ns trag v(out) val=4.5 rais=1
.tran 0 0.1us
.include "C:\Users\CS Net Games\Desktop\4th 2ndSem\IC\New folder\C5_models.txt"
```

I used the same code for invertor and for the buffer.

References

https://en.wikichip.org/wiki/File:Buffer_gate_cmos.png