Faculty of Engineering and Technology

Electrical and Computer Engineering Department

DIGITAL INTEGRATED CIRCUITS– ENCS3330

Assignment No. 2 Report

3-Input NAND and XOR using electric

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Section: 1

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Assignment parts:

Lambda" Design Rules– lambda, λ, = 1/2 minimum feature size

The program has scaling number we have to follow, which is 3µm.

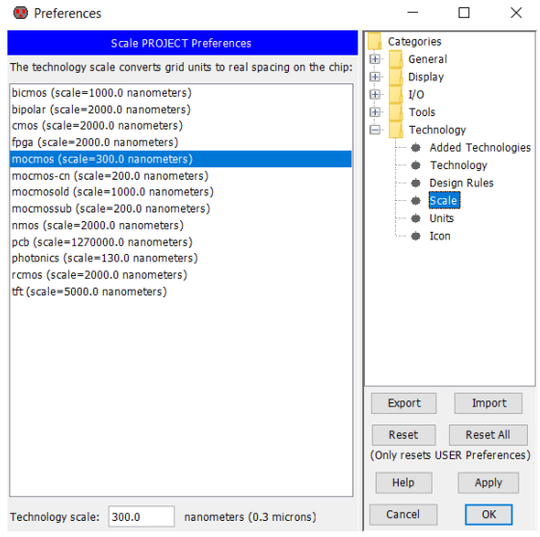

Figure 1 Scales

Part 1: 3-NAND:

1.1 NAND gate:

The three-input NAND gate produces an output only when all three inputs are low. This means that if any of the three inputs are high, the output will be low.

3-input Nand gate follows the truth table below:

Table 1 NAND3 truth table

Input			output
C	B	A	out
0	0	0 (0-10ns)	1
0	0	1(20-30ns)	1
0	1	0(40-50ns)	1
0	1	1(60-70ns)	1
1	0	0(80-90ns)	1
1	0	1(100-110ns)	1
1	1	0(120-130ns)	1
1	1	1(140-150ns)	0

Which we will use later on to determine the spice code for the circuit.

1.2 Schematic:

First part is to build a three input NAND with width 10 and length 2. For PMOS and 30 width, length 2 for NMOS as the following:
as in the 3 input NAND gate, the width of the PMOS devices is the same as the base widths because they are connected in **parallel**. However, the NMOS devices were set to the base width multiplied with their number which means (10*3=30) because they are connected on **series**.

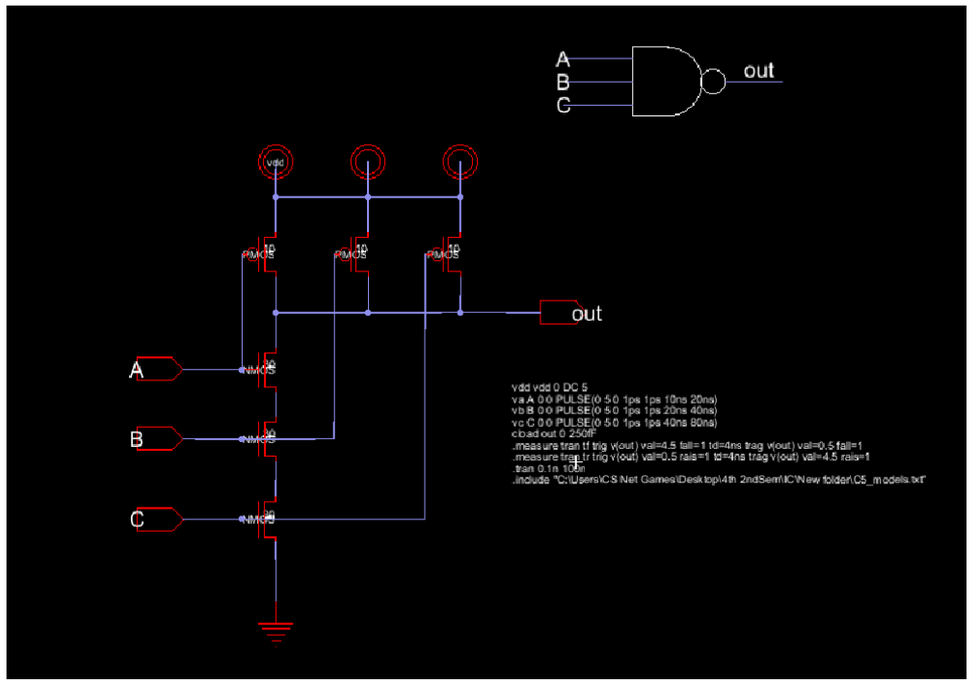

Figure 2 3input Nand schematic

1.3 Simulations:

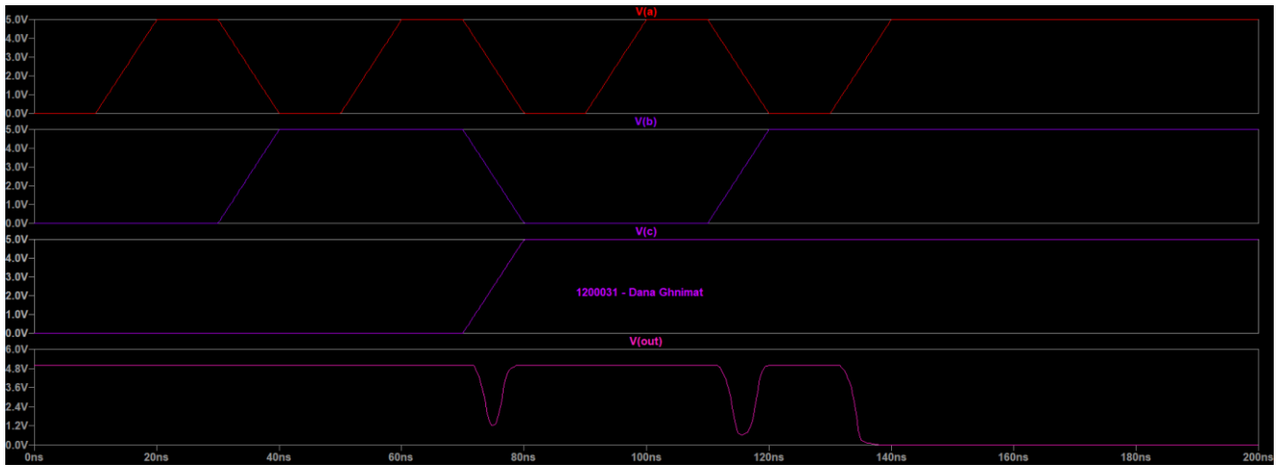

Figure 3 Simualtion1 in NAND gate

Spice code:

```
vdd vdd 0 DC 5
va A 0 pwl 10n 0 20n 5 30n 5 40n 0 50n 0 60n 5 70n 5 80n 0 90n 0 100n 5 110n 5 120n 0 130n 0 140n 5 150n 5
vb B 0 pwl 30n 0 40n 5 70n 5 80n 0 110n 0 120n 5 150n 5
vc C 0 pwl 70ns 0 80ns 5
cload out 0 250fF
.measure tran tf trig v(out) val=4.5 fall=1 td=4ns trag v(out) val=0.5 fall=1
.measure tran tr trig v(out) val=0.5 rais=1 td=4ns trag v(out) val=4.5 rais=1
.tran 200n
.include "C:\Users\CS Net Games\Desktop\4th 2ndSem\IC\New folder\C5_models.txt"
```

Simulation using pulsing:

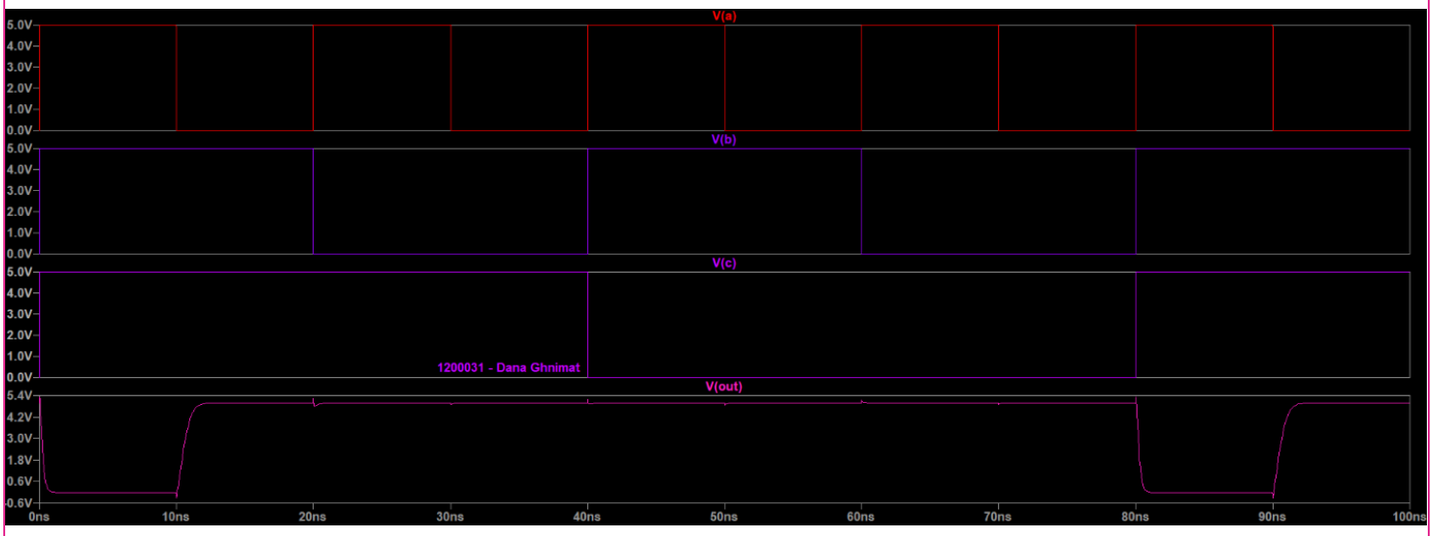

Figure 4 3-Input Nand gate using pulse inputs

From figure 5, the output included all the cases as well, yet it was easier to read.

Noticing from 0 to 10ns the input for all cases is 1, so the output is 0 matched the truth table, same when it was A, B, C 0 1 1 which is 1 and so on like the following truth table:

Table 2 NAND 3-inputs time and truth table

Input			Time	output
C	B	A		out
0	0	0	(70-80ns)	1
0	0	1	(60-70ns)	1
0	1	0	(50-60ns)	1
0	1	1	(40-50ns)	1
1	0	0	(30-40ns)	1
1	0	1	(20-30ns)	1
1	1	0	(10-20ns)	1
1	1	1	(00-10ns)	0

Spice code:

```
vdd vdd 0 DC 5
va A 0 0 PULSE(0 5 0 1ps 1ps 10ns 20ns)
vb B 0 0 PULSE(0 5 0 1ps 1ps 20ns 40ns)
vc C 0 0 PULSE(0 5 0 1ps 1ps 40ns 80ns)
cload out 0 250fF
.measure tran tf trig v(out) val=4.5 fall=1 td=4ns trag v(out) val=0.5 fall=1
.measure tran tr trig v(out) val=0.5 rais=1 td=4ns trag v(out) val=4.5 rais=1
.tran 0.1n 100n
.include "C:\Users\CS Net Games\Desktop\4th 2ndSem\IC\New folder\C5_models.txt"
```

1.4 Icon:

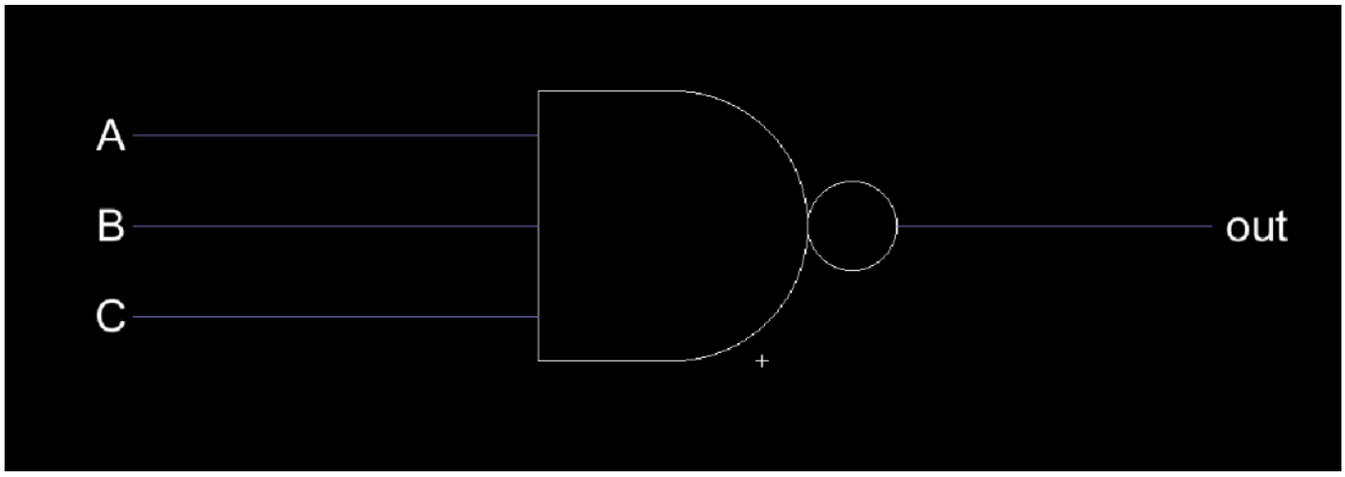

Figure 5 3-input Nand gate icon

Simulation of the icon:

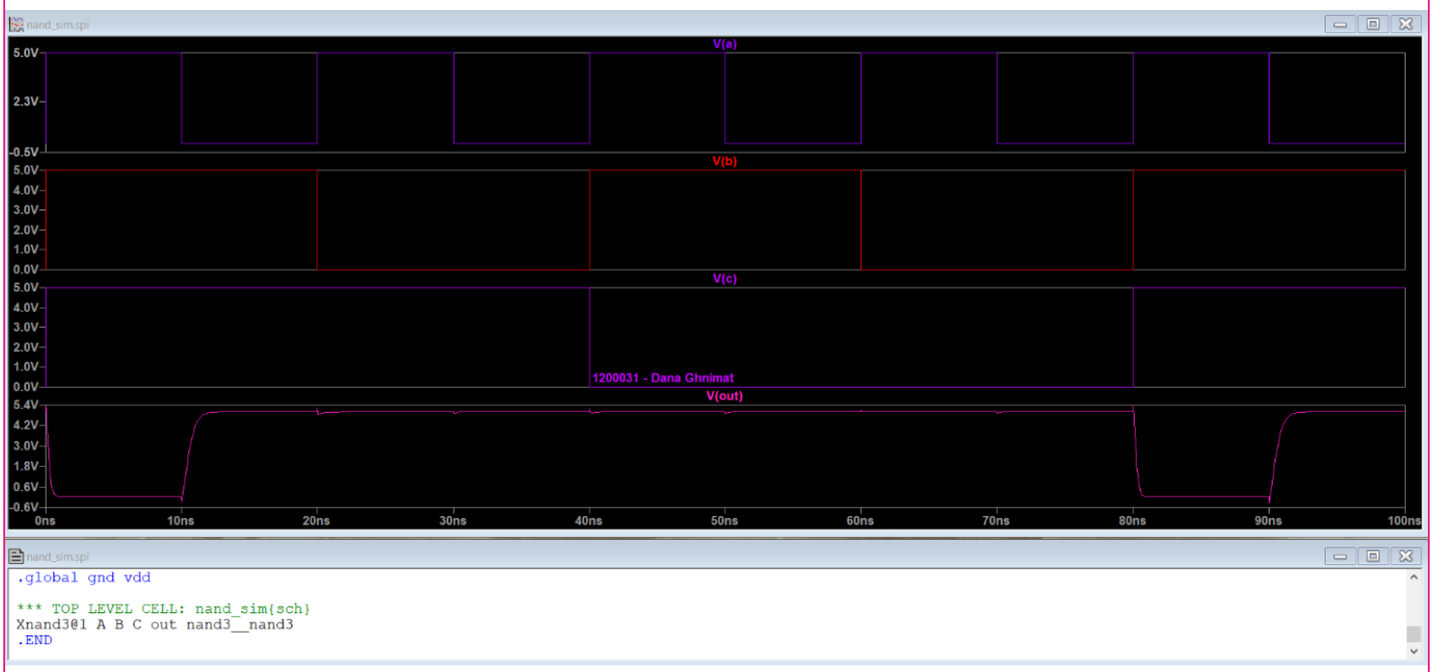

Figure 6 Icon 3-input Nand simulation

1.5 Layout:

And for more visibility I used a white background to show names ot the components.

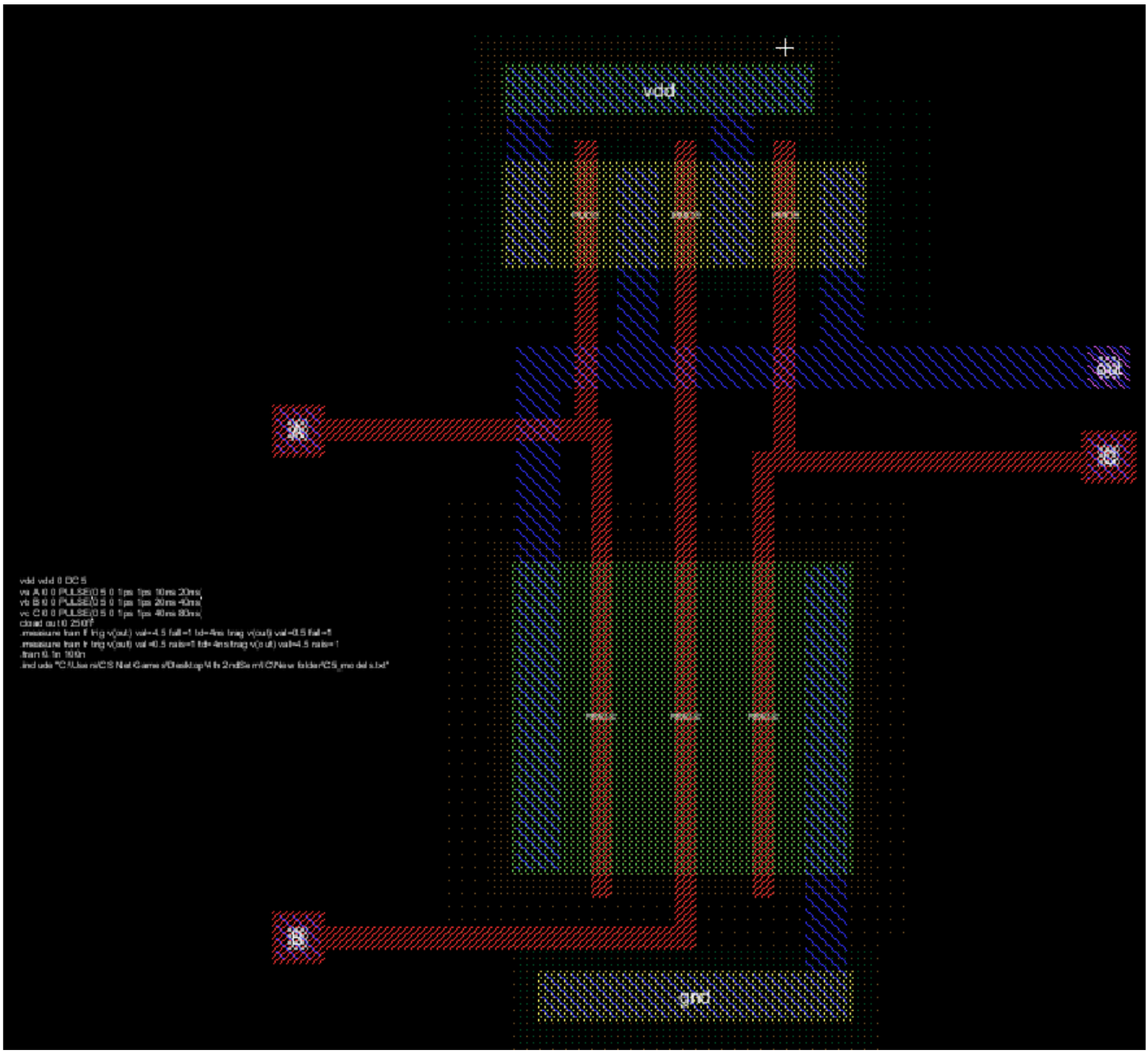

Figure 7 Layout using black background

Layout2:

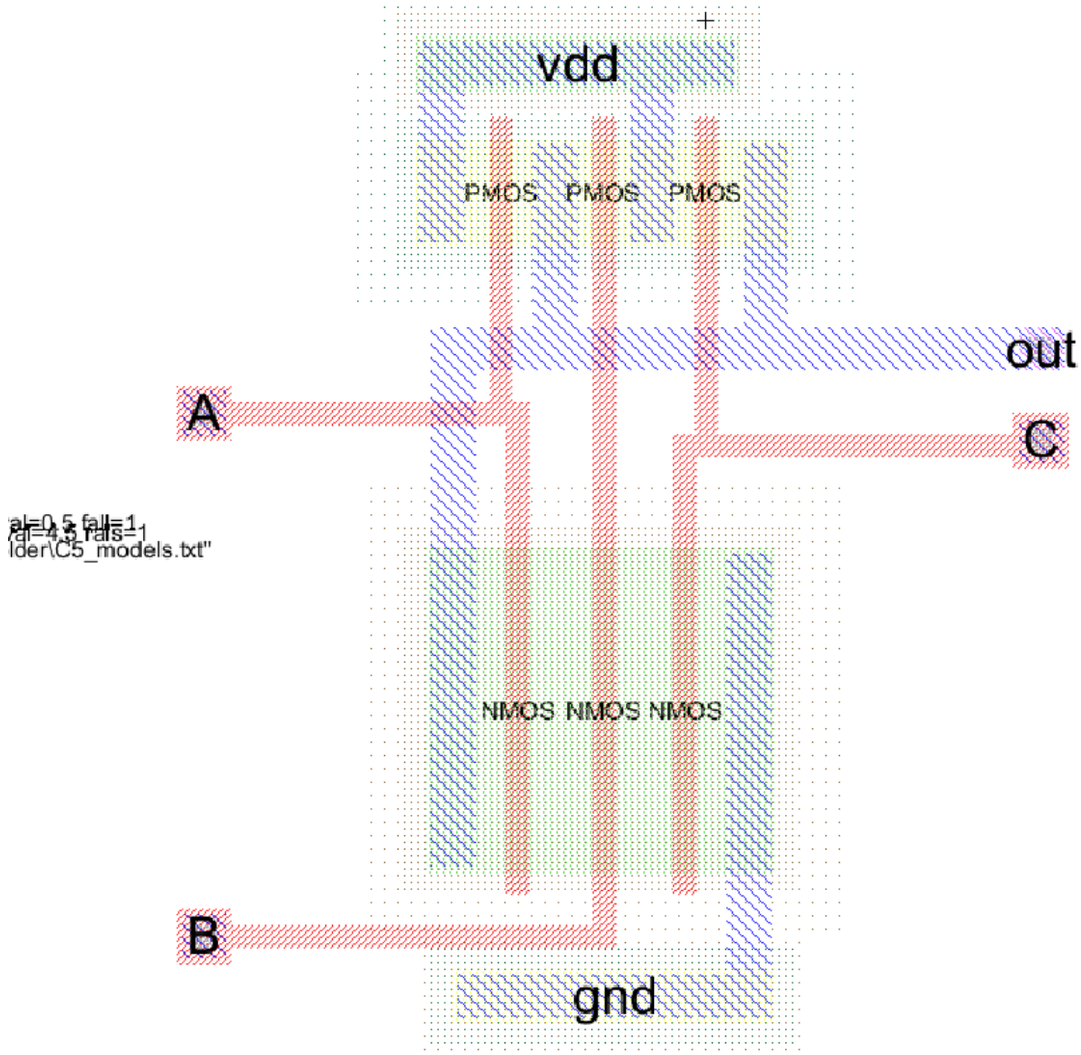

Figure 8 layout using white background

Simulation:

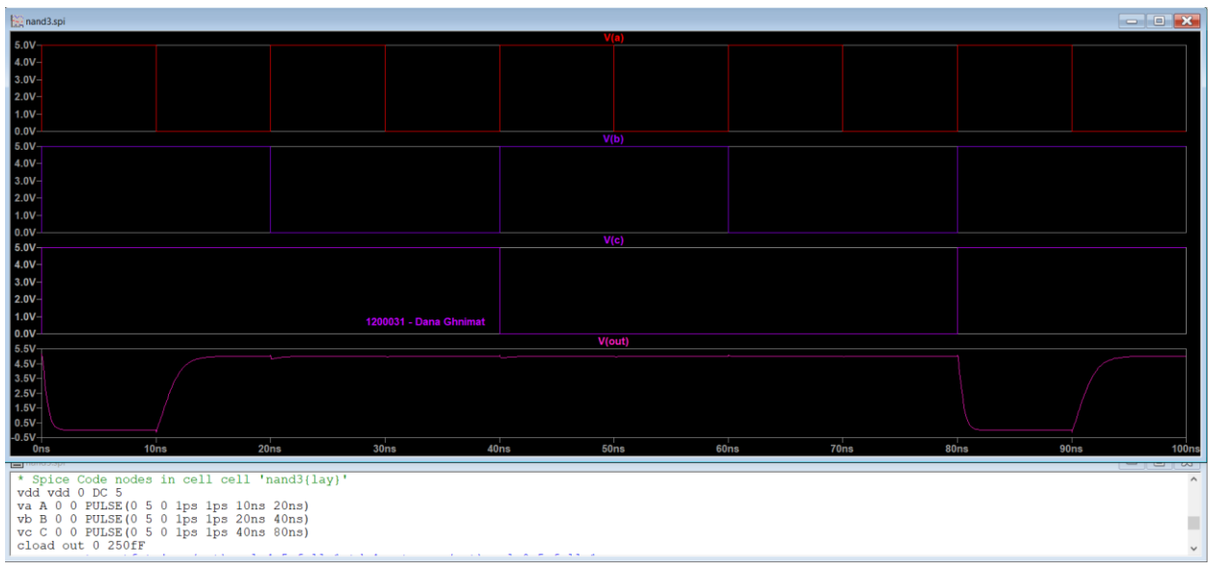

Figure 9 Simulation of the layout

1.6 Error checks :

```
---------------------------------963---------------------------------
Checking Wells and Substrates in 'nand3:nand3{lay}' ...
   Geometry collection found 22 well pieces, took 0.001 secs
   Geometry analysis used 8 threads and took 0.002 secs
NetValues propagation took 0.0 secs
Checking short circuits in 2 well contacts
   Additional analysis took 0.0 secs
No Well errors found (took 0.003 secs)
=================================964=================================
Hierarchical NCC every cell in the design: cell 'nand3{sch}'  cell 'nand3{lay}'
Comparing: nand3:nand3{sch} with: nand3:nand3{lay}
  exports match, topologies match, sizes not checked in 0.004 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.004 seconds.
=================================965=================================
Running DRC with area bit off, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 15 networks
Checking cell 'nand3{lay}'
        No errors/warnings found
0 errors and 0 warnings found (took 0.014 secs)
```

Figure 10 Errors for Nand gate

From the program analysis, the Nand gate does not have any error or wells or extra substrates.

Part 2: 3-NOR:

1.1 NOR gate:

The nor gate truth table below:

Table 3 3-input nor gate

Input			Time	output
C	B	A		out
0	0	0	(70-80ns)	1
0	0	1	(60-70ns)	0
0	1	0	(50-60ns)	0
0	1	1	(40-50ns)	0
1	0	0	(30-40ns)	0
1	0	1	(20-30ns)	0
1	1	0	(10-20ns)	0
1	1	1	(00-10ns)	0

Spice code:

```
vdd vdd 0 DC 5
va A 0 0 PULSE(0 5 0 1ps 1ps 10ns 20ns)
vb B 0 0 PULSE(0 5 0 1ps 1ps 20ns 40ns)
vc C 0 0 PULSE(0 5 0 1ps 1ps 40ns 80ns)
cload out 0 250fF
.measure tran tf trig v(out) val=4.5 fall=1 td=4ns trag v(out) val=0.5 fall=1
.measure tran tr trig v(out) val=0.5 rais=1 td=4ns trag v(out) val=4.5 rais=1
.tran 0.1n 100n
.include "C:\Users\CS Net Games\Desktop\4th 2ndSem\IC\New folder\C5_models.txt"
```

1.2 Schematic:

According to the rule of sizing , the width for all Nmos is 10, and length 2, And Pmos of 30 width and 2 length.

In the NOR gate as NMOS devices are connected in parallel (NMOS width =10) and PMOS devices are connected on series (PMOS width =3*10=30).

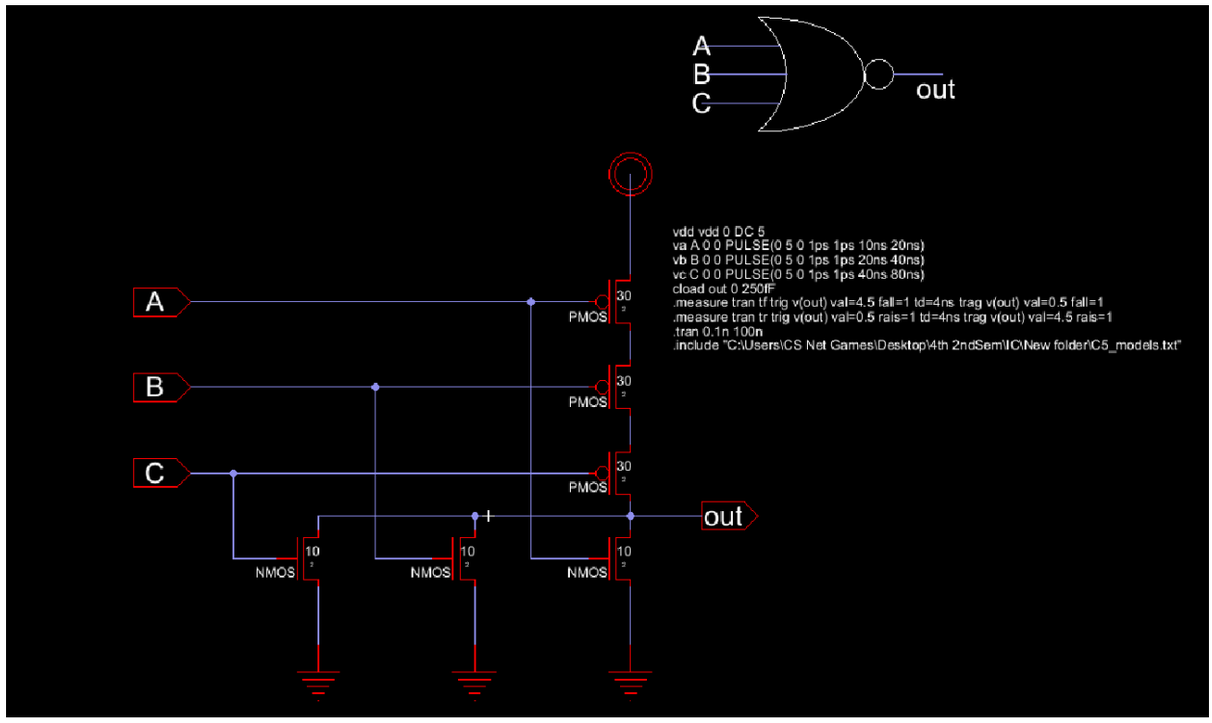

Figure 11 Schematic view of 3 input nor

1.3 Simulations:

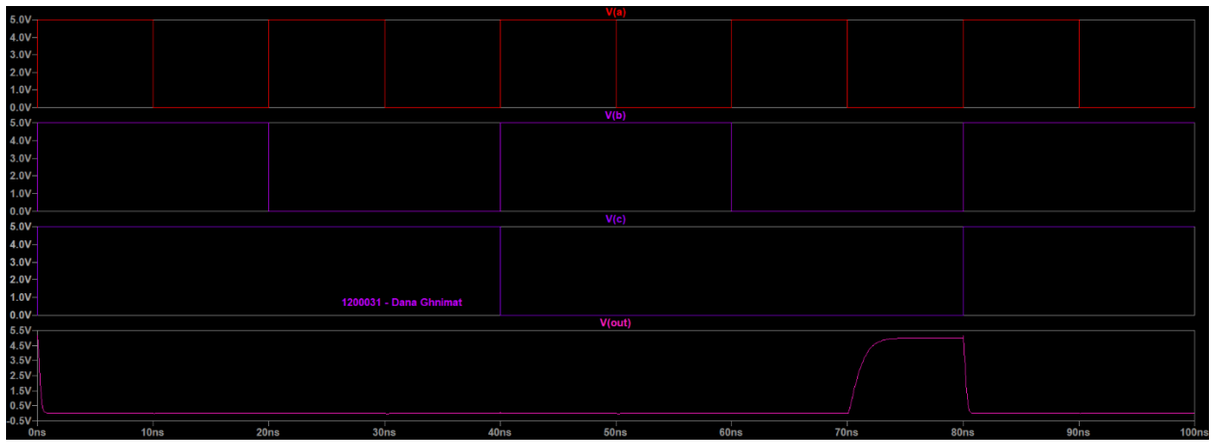

Figure 12 Simulation of 3 input nor gate

As seen in the simulation the cases of the inputs match the ones in the truth table, as all cases goes to 0 unless all A, B, C are 0 the output is 1.

1.4 Icon:

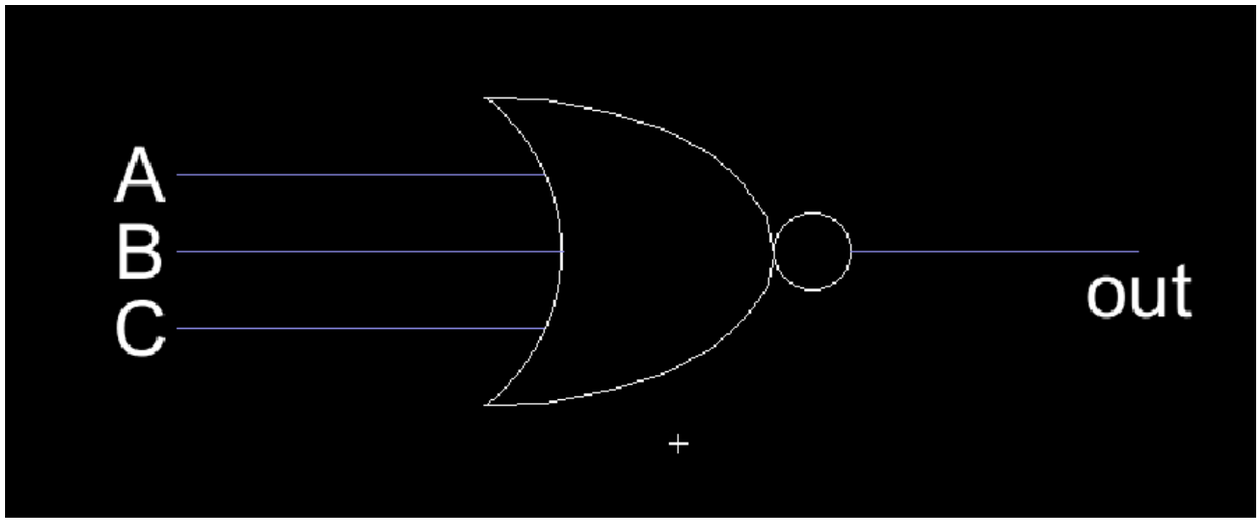

Figure 13 Icon of 3input nor

Simulation:

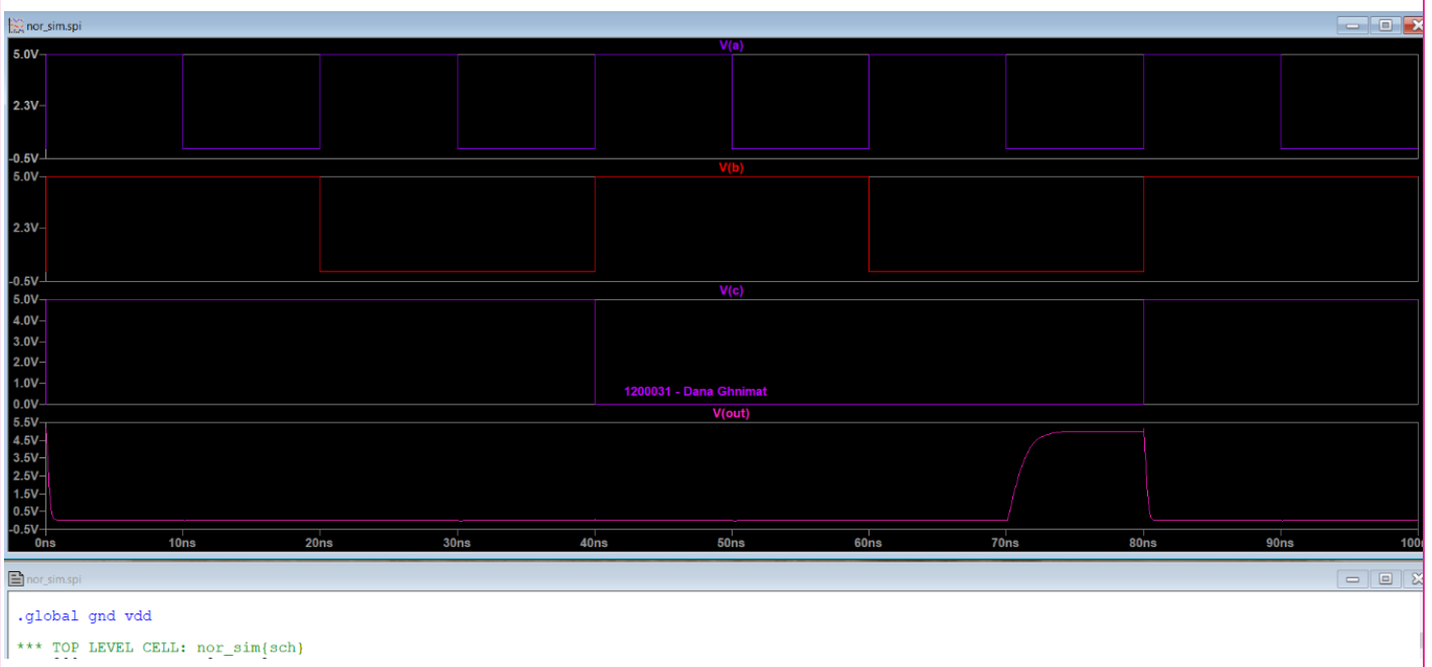

Figure 14 Simulation of 3input nor icon

1.5 Layout:

Layout in black background:

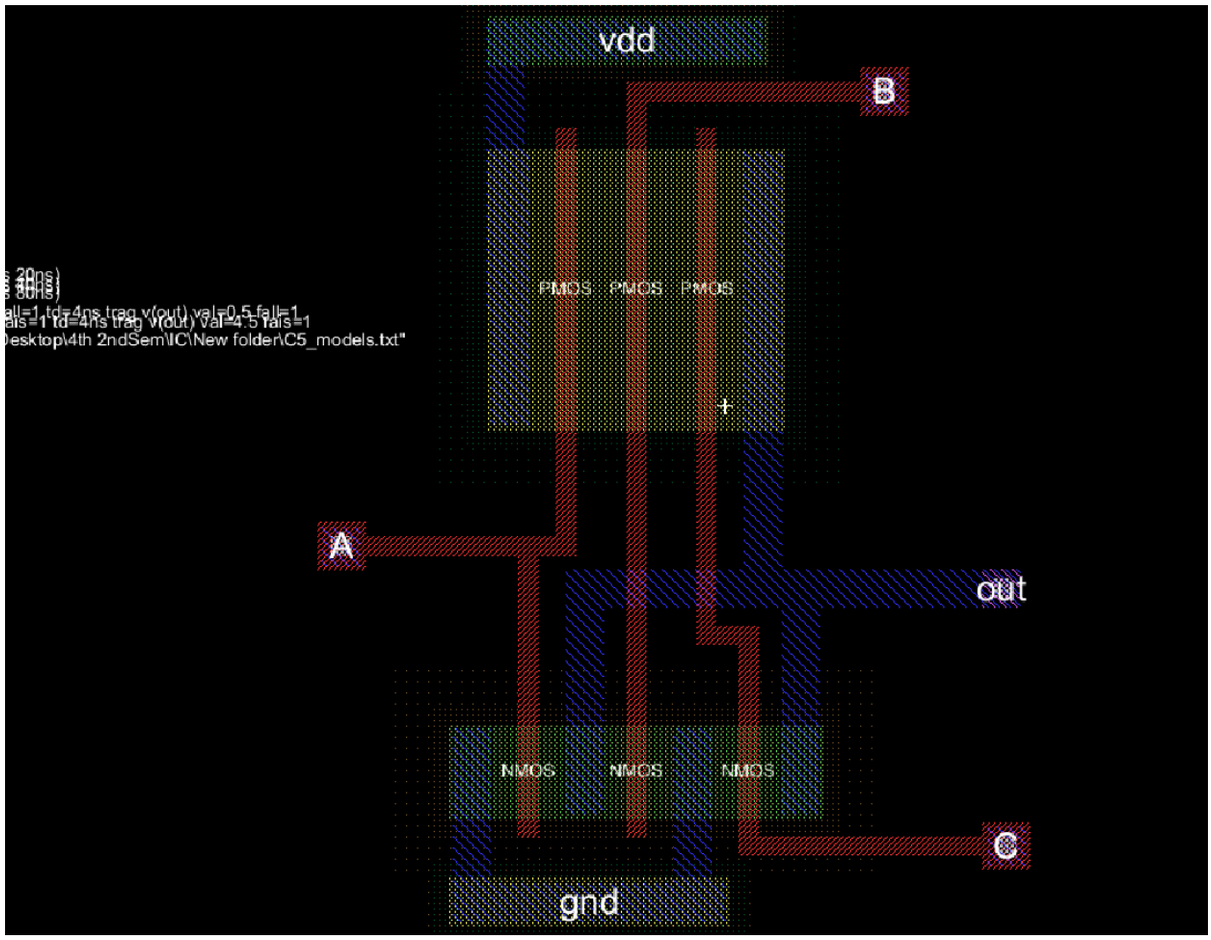

Figure 15 Layout 3-input nor

Code I used for this nor gate is the same as the Nand gate:

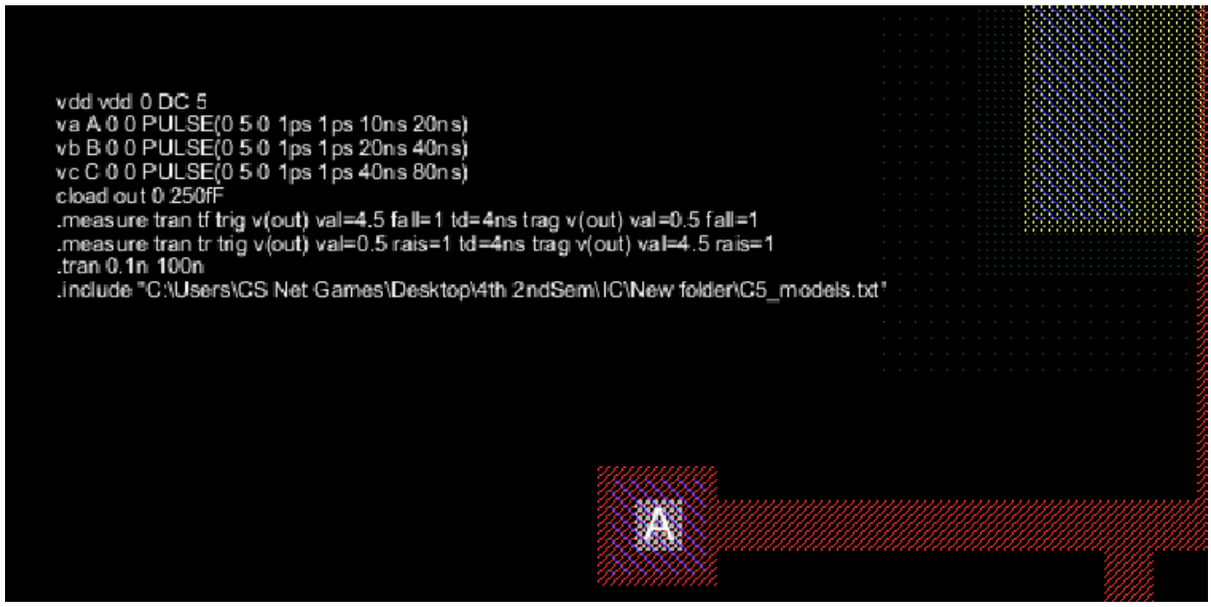

Figure 16 Code in the layout

When rising the text size, the text crumbles in the code and not quite visible.

In white background:

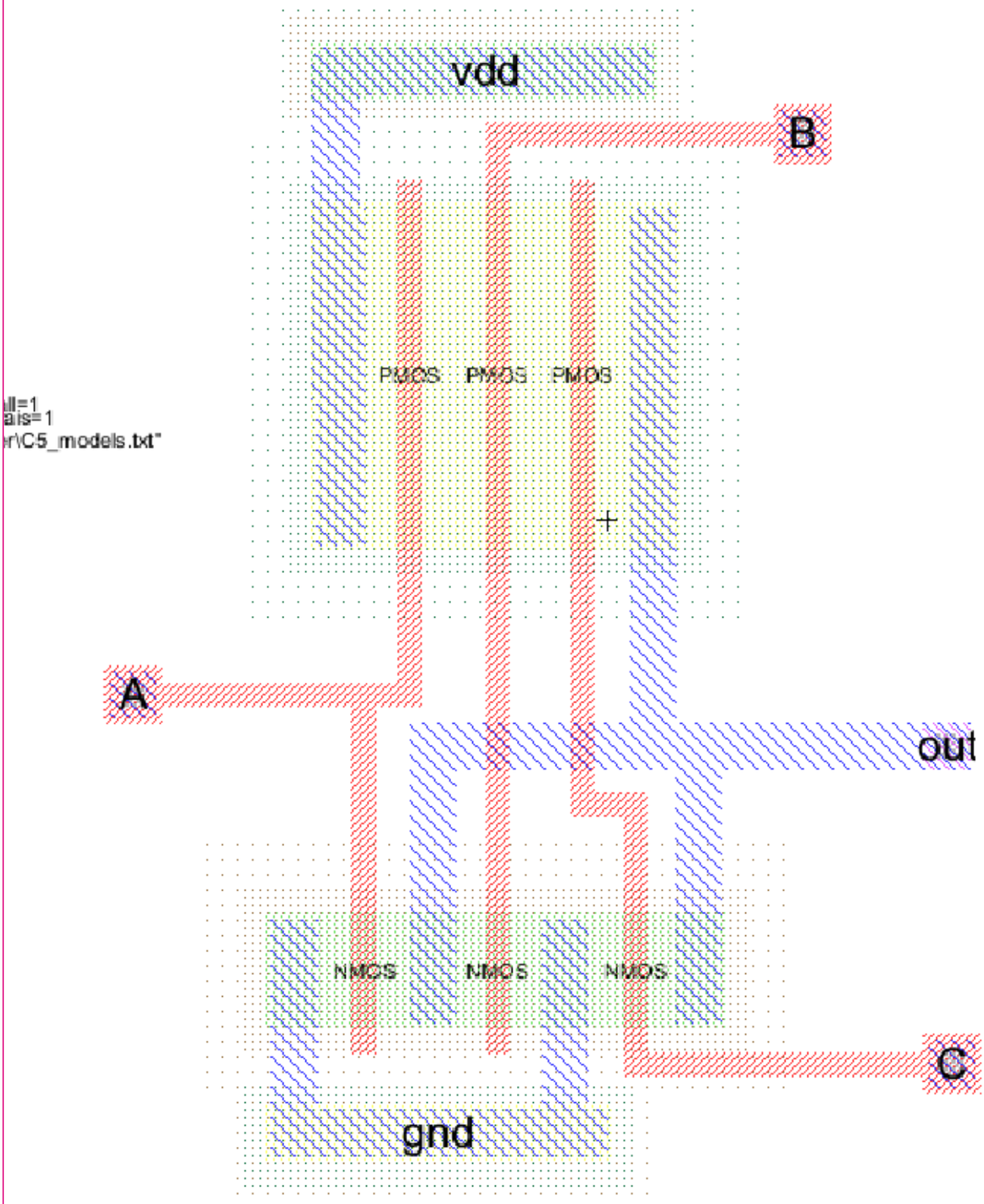

Figure 17 Layout for 3input nor

Simulation:

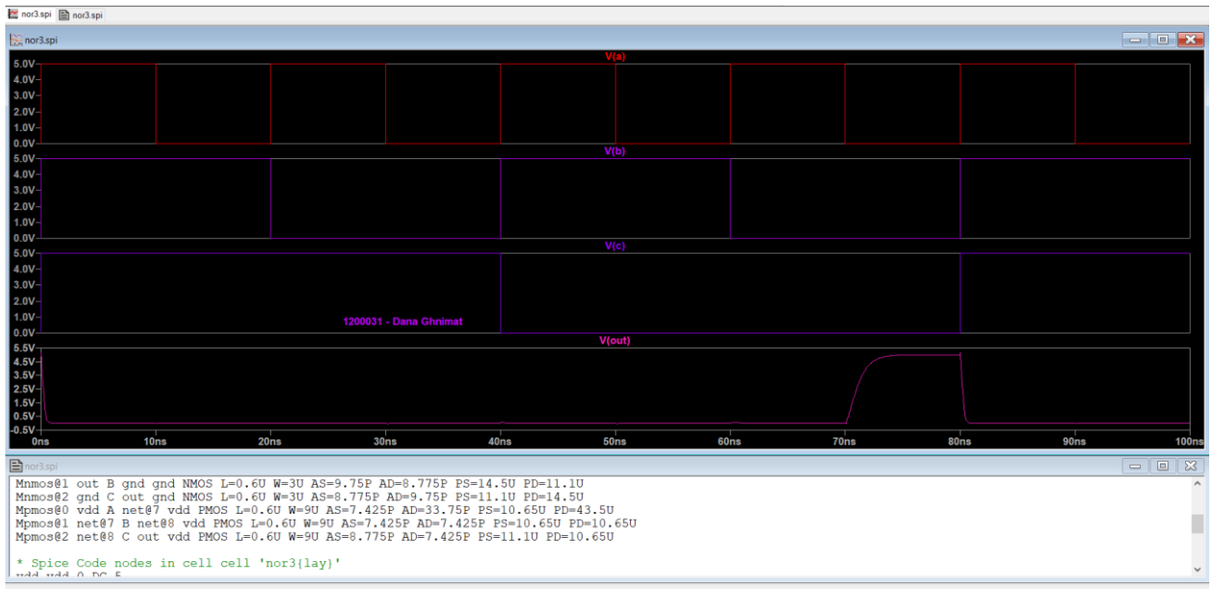

Figure 18 Simulation for 3-input nor layout

1.6 Errors checks of layout:

To check after building the layout for 3 input nor gate:

```
Running DRC with area bit off, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 15 networks
Checking cell 'nor3{lay}'
        No errors/warnings found
0 errors and 0 warnings found (took 0.007 secs)
==================================951==================================
C:\Users\CS Net Games\Desktop\4th 2ndSem\IC\New folder\e\nor3.spi written
Running spice command: C:\PROGRA~1\LTC\LTspiceXVII\XVIIx64.exe -i nor3.spi -r nor3.raw -o nor3.out
==================================952==================================
Moved text (-21,-10.5)
==================================953==================================
Moved text (-19,0.5)
```

Figure 19 check hierarchically msg for nor gate

1- wells and NCC checks for any leaks or other wires:

```
==================================955==================================
Hierarchical NCC every cell in the design: cell 'nor3{sch}'  cell 'nor3{lay}'
Comparing: nor3:nor3{sch} with: nor3:nor3{lay}
  exports match, topologies match, sizes not checked in 0.032 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.041 seconds.
==================================956==================================
Checking Wells and Substrates in 'nor3:nor3{lay}' ...
   Geometry collection found 24 well pieces, took 0.001 secs
   Geometry analysis used 8 threads and took 0.002 secs
NetValues propagation took 0.001 secs
Checking short circuits in 2 well contacts
   Additional analysis took 0.0 secs
No Well errors found (took 0.004 secs)
```

Figure 20 NCC and Wells and substrates checks

References

https://www.javatpoint.com/nand-gate-in-digital-electronics

https://www.javatpoint.com/nor-gate-in-digital-electronics