| | Max Mark | Student Mark |
|---|---|---|
| **Problem 1** | 45 | |
| **Problem 2** | 20 | |
| **Problem 3** | 20 | |
| **Problem 4** | 15 | |
| Sum | 100 | |

**Problem 1 Solution(45 pts)**

| 1 | 2 | 3 |
|---|---|---|
| C | D | C |
| 4 | 5 | 6 |
| D | D | C |
| 7 | 8 | 9 |
| B | B | C |
| 10 | 11 | 12 |
| E | C | B |
| 13 | 14 | 15 |
| A | B | C |

**Problem 1 Solution(45 pts)**

**Please fill the Answer in the table shown in the first sheet . (3 Point each)**

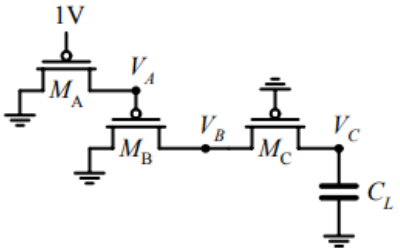
1. **The design flow of IC design system is :**
   1. architecture design 2. market requirement 3.Layout 4. HDL coding 5. logic design
   - **A.** 5-1-2-4-3
   - **B.** 2-1-5-3-4
   - **C.** 2-1-5-4-3
   - **D.** 4-1-3-2-5
   - **E.** 5-3-2-1-4

2. **CMOS NANS gate is better than CMOS NOR gates because**
   - A. CMOS nor takes more space than NAND
   - B. CMOS NOR uses P channel transistor in parallel.
   - C. CMOS NAND uses P channel transistor in parallel.
   - D. Only A and C is correct.
   - E. All (A and B and C) are correct

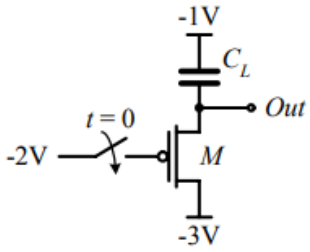
3. **How many transistors are required to implement a four-input OR using CMOS design style?**
   - A. 6
   - B. 8
   - C. 10
   - D. 12
   - E. None

4. **In order to have "pass" logic gate We need**
   - A. An N-channel and P-Channel transistor in series
   - B. We need only p-channel so it will pass good one.
   - C. We need only N-channel so it will pass good zero.
   - D. An N-channel and P-Channel transistor in parallel
   - E. None

5. **For the circuit in Fig. below, determine the final value of VA, VB, VC, assuming initial condition at each of the nodes is 3V and VTP = −0.5V (ignore body effect).**
   - **A.** VA = 3V VB = 2V VC = 1.5V
   - **B.** VA = 1.5V VB = 1.5V VC = 1.5V
   - **C.** VA = 2V VB = 2V VC = 2V
   - **D.** VA = 1.5V VB = 2V VC = 2V
   - **E.** None




6. **Assuming that switch as shown in figure below closes at time t = 0, what is the output voltage at t = 0+ and t = ∞? CL was initially discharged, VTP = −0.5V.**
   - **A.** Vout (t = 0+ ) = +1V Vout (t = ∞) = −1.5V
   - **B.** Vout (t = 0+ ) = −1V Vout (t = ∞) = +1.5V
   - **C.** Vout (t = 0+ ) = −1V Vout (t = ∞) = −1.5V
   - **D.** Vout (t = 0+ ) = +1V Vout (t = ∞) = +1.5V
   - **E.** None

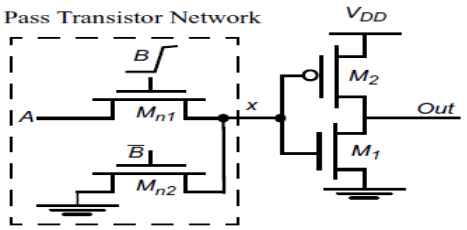



7. **The delay of a static CMOS inverter is minimized** if (W/L)p / (W/L)n = µn / µp.
   - **A.** True
   - **B.** False
   - **C.** None
8. **The load capacitance of a static CMOS gate has no effect on its VTC**
   - **A.** False
   - **B.** True
   - **C.** None
9. **---------- connects between 2 segments of metal layers**
   - A. Contact
   - B. Poly
   - **C. Via**
   - D. Diffusion
   - E. None

10. **CMOS Transmission (Pass) Gates , capable of passing both '1' and '0'**
    - **A. Good "1"**
    - **B. Good "0"**
    - **C. Poor "1"**
    - **D. Poor "0"**
    - **E. Both A and B only**

**11. What is the logic function performed by this circuit?**

**A. The circuit is a NOR gate.**
**B. The circuit is a XOR gate.**
**C. The circuit is a NAND gate.**
**D. The circuit is a NOT gate.**
**E. None**




**12. Increasing power supply voltage, VDD, will**

**A.** Does not change the speed performance of CMOS gates.
**B.** Increase the speed performance of CMOS gates.
**C.** Decrease the speed performance of CMOS gates.
**D. None**

**13. The IN and OUT bus lines in IC design should be in**

A. Metal
B. Contact
C. Polysilicon
D. Diffusion
E. Silicon
F. None

**14. If an NMOSFET gate's dielectric were changed from SiO2 to a low-κ material with half the permittivity of SiO2, what would happen to its ID? You may assume that VGS ≥ VTN**

**A.** Id does not change.
**B.** ID being halved.
**C.** ID doubled.
**D. Id does not change.**
**E. None**

**15.** Which one is the right order for the following the following interconnect fabrication steps :

• Etch metal. • Expose photoresist using mask. • Remove all photoresist.
• Deposit photoresist. • Deposit metal everywhere.

A. 1)Deposit metal everywhere. 2) Expose photoresist using mask. 3). Deposit photoresist 4) Etch metal. 5) Remove all photoresist
B. 1) ) Deposit photoresist 2) Deposit metal everywhere 3) Expose photoresist using mask. 4) Etch metal. 5) Remove all photoresist
C. 1)Deposit metal everywhere. 2) Deposit photoresist. 3) Expose photoresist using mask. 4) Etch metal. 5) Remove all photoresist
D. 1)Deposit metal everywhere. 2) Expose photoresist using mask. 3) Deposit photoresist. 4) Etch metal. 5) Remove all photoresist
E. None

**IC Design ENCS333** **Midterm Jun-16-2023**

Student Name : _____ Stud BIRZEIT UNIVERSITY _____

**Problem 2: (20 pts)**

A. Consider an N-channel MOSFET. You may assume that this MOSFET has no oxide charge. Fill in the blank cells in the table, using the following symbols: ↑ for increase, ↓ for decrease, and → for no change. If the cell has already been provided with an X it means that you are not responsible for filling that cell out. When moving along a row consider only the change brought on due to the parameter specified in the first cell of that row. **(7 pts)**

| | $V_t$ | $V_{FB}$ | $\mu_s$ | $I_{ds}$ |
|---|---|---|---|---|
| $T_{ox}$ ↑ | increase | No change | ***Assume $V_t$ is unchanged*** increase | ***Assume $\mu_s$ remains unchanged*** decreas |
| Temperature ↑ | **X** | decreas | decrease | **Assume $V_t$ is constant and** decrease |

B. Answer the following Questions about the figure shown below : **(13 pts)**

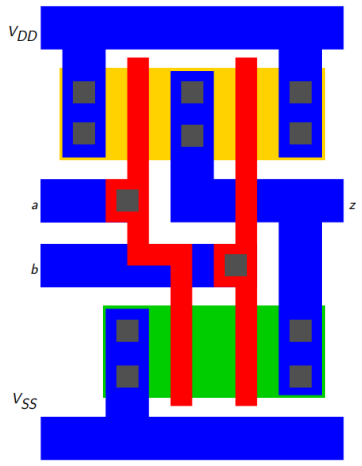
a. What does this layout represent ? _____

b. How many contacts does it Have ? _____

c. How Many Poly head/contact it has ? _____

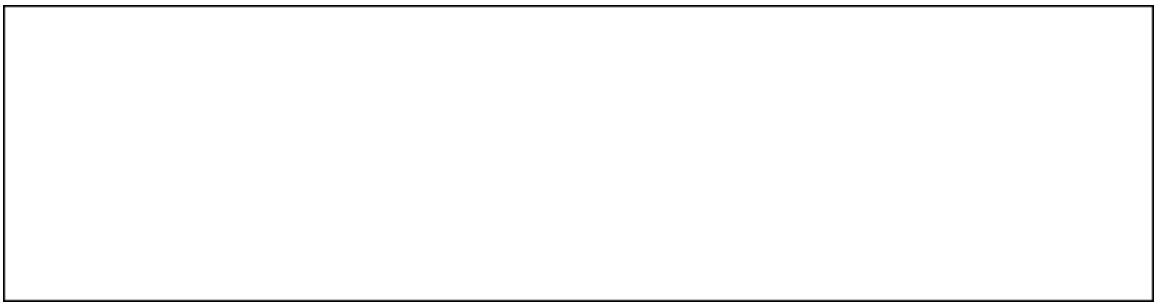
d. Mark the length(Ln) and the width (wp, wn) of devices on the figure

e. Sketch the equivalent detail schematic and the schematic symbol view.

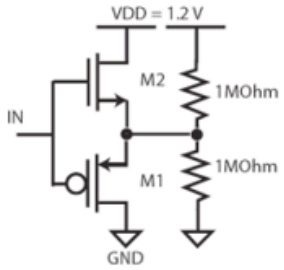


**Problem 3: (20 pts)**

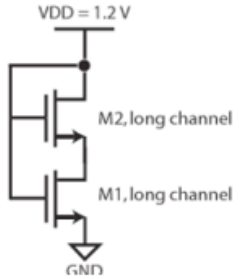
1. Indicate the regions of operation of the transistors shown in the circuits in the tables next to the circuits. Assume short channel devices unless otherwise stated VTn=VTp= 0.3 V, Vvsatn= 0.3 V, Vvsatp= 0.6 V and neglect the body effect. **(10 pts)**



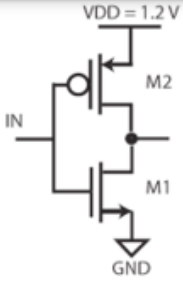
Solutions:




| Voltage IN | Region of Operation M1 | Region of Operation M2 |
|---|---|---|
| GND (0 V) | O cutoff<br>O linear<br>X saturation<br>O vel. saturation | X cutoff<br>O linear<br>O saturation<br>O vel. saturation |
| VDD (1.2 V) | X cutoff<br>O linear<br>O saturation<br>O vel. saturation | O cutoff<br>O linear<br>X saturation<br>O vel. saturation |

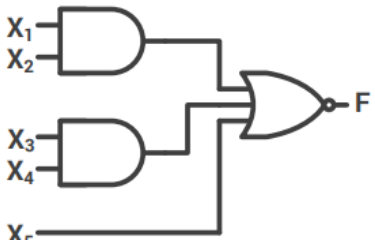



| Region of Operation M1 | Region of Operation M2 |
|---|---|
| O cutoff<br>X linear<br>O saturation | O cutoff<br>O linear<br>X saturation |

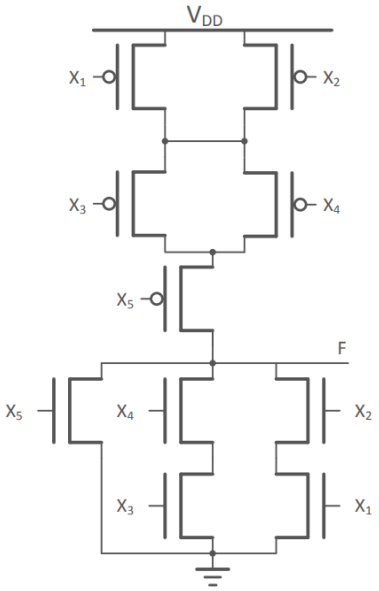



| IN | M1 | M2 |
|---|---|---|
| GND (0 V) | X cutoff<br>O linear<br>O saturation<br>O vel. saturation | O cutoff<br>X linear<br>O saturation<br>O vel. saturation |
| VDD (1.2 V) | O cutoff<br>X linear<br>O saturation<br>O vel. saturation | X cutoff<br>O linear<br>O saturation<br>O vel. saturation |

2. Consider the And-OR-Inverter (AOI) cell shown in Figure below. Derive the CMOS complex gate that implements this cell with minimum number of transistors. **(5 pts)**




Solutions:




T1 =$X_1.X_2$

T2 = $X_3.X_4$

Pull-Up Network

F = $(X_1.X_2 + X_3.X_4 + X_5)'$

F = $(X_1'+X_2')\ (X_3'+X_4').X_5'$

F = $(X_1'X_3'+X_1'X_4'+X_2'X_3'+X_2'X_4')X_5'$

Pull-Down Network

F = $(X_1.X_2) +(X_3.X_4)+X_5'$

3. Consider the layout in Figure below **(5 pts)**

(a) What type of logic function does this layout implement?

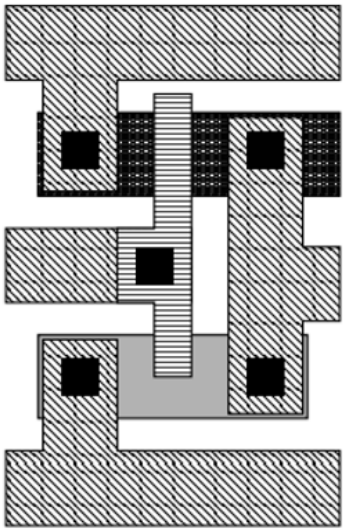
A messed up inverter.

(b) Point out the three largest problems with this layout. For each explain the impact on gate behavior. When possible, indicate the ways in which important parameters are influenced, e.g., k 0 .

i. The bottom half of the NMOSFET gate is missing.

ii. . The PMOSFET drain is bigger than it needs to be, increasing capacitance without benefit.

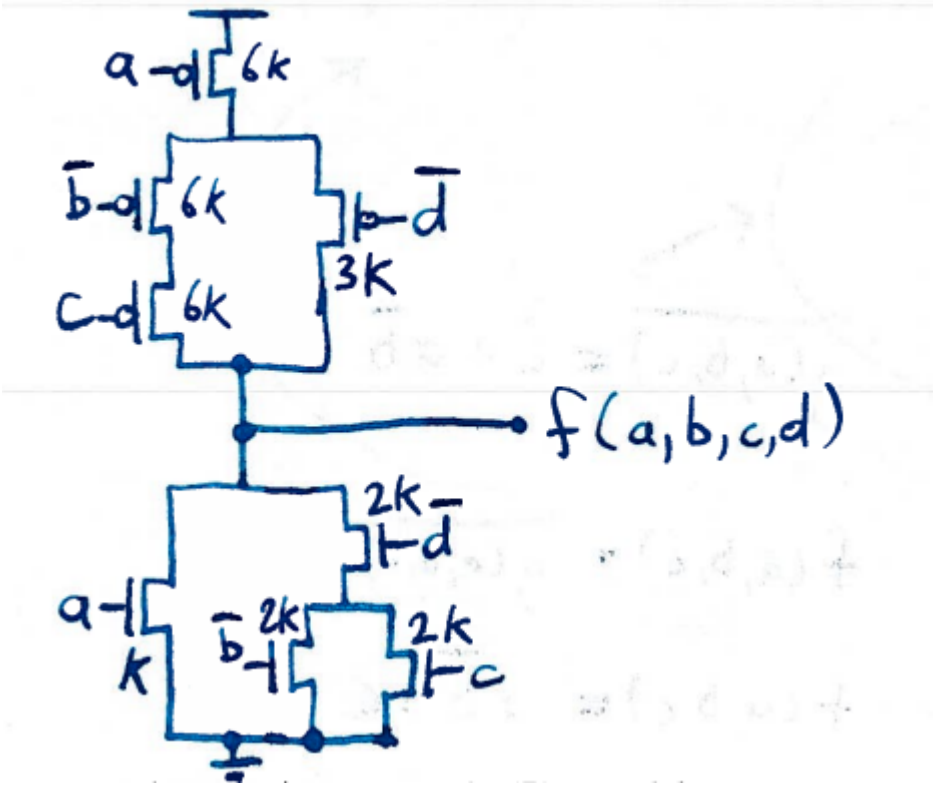
iii. The NMOSFET and PMOSFET active regions are the same width, which would result in asymmetric pull-up and pull-down resistances if the gates were designed correctly.



**Problem 3: (15 pts)**

1. **Implement the following function as a single logic gate. Indicate the widths of all gates in terms of k, the minimal gate width. Size the transistors to achieve the same worst-case resistance as a balanced, minimal width inverter (i.e., an inverter with a w-wide NMOSFET and a 2k-wide PMOSFET). (5 pts)**

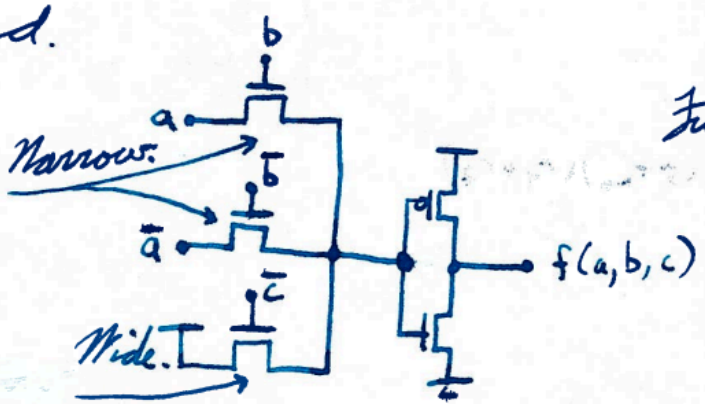
$$f(a, b, c, d) = a'(bc' + d)$$




2. **Implement the following function using the minimal number of transistors. The output of your implementation should have full output range, from VSS to VDD. However, it needn't be particularly fast or can have weak signal at some stages. You may use literals as direct inputs. (5 pts)**

$$f(a, b, c) = (ab' + a'b)c$$

Most or full credit was given for some designs w. ≤ 8 transistors. However, I wanted to see how far this could be pushed.




Fun, huh?