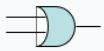
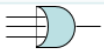
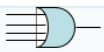
| Question | Full Grade | Student Grade | ABET OUTCOME |
|---|---|---|---|
| 1 | 10 | | a |
| 2 | 20 | | a |
| 3 | 20 | | c |
| 4 | 20 | | c |
| 5 | 20 | | k |
| 6 | 20 | | k |

**Question 1 (10)**

**A)** Show how you can optimize the design for power given that: **(4 points)**

Y= a + b + c + d given that power per cell is given as shown below

| Cell | Power |
|---|---|
|  | 2 |
|  | 2.5 |
|  | 3 |

Using one 4-input OR gate:4-input OR gate to compute a+b+c+d (power 3)Total power consumption: 3

**B)** Explain the difference between latch and FF? **(4 points)**

Latch:
A latch is a level-sensitive device, meaning it is transparent when the control signal (enable or clock) is active. It continuously follows the input when enabled and retains the last state when disabled.
Example: D-latch changes its output based on the input whenever the enable signal is high.
Flip-Flop:
A flip-flop is an edge-sensitive device, meaning it changes state only at specific moments of the control signal (usually on the rising or falling edge of a clock signal).
Example:
D flip-flop changes its output only on the clock edge (positive or negative), making it more precise in timing.

C) What do we mean by Transparency? Does it affect latch based design or FF based design? **(2 points)**

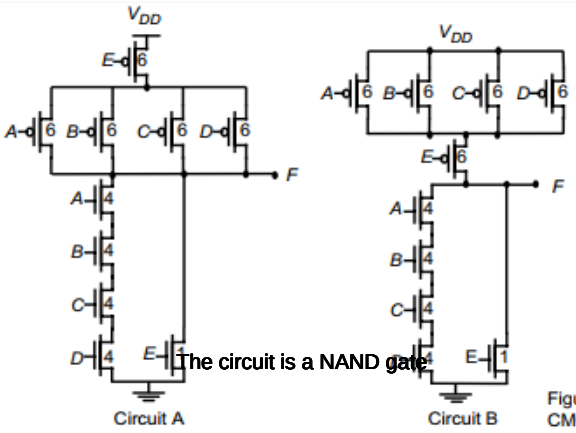
ransparency in digital electronics refers to the behavior of a device (such as a latch) where the output directly follows the input when the control signal (usually called the enable signal) is active. This means that as long as the enable signal is active, any changes at the input will immediately be reflected at the output. When the enable signal is inactive, the output retains its last state, regardless of changes at the input.

Transparency:
Latch-Based Design: Transparency means the output follows the input when enabled, potentially leading to timing issues and requiring careful design management.

Flip-Flop-Based Design: Transparency is not a concern as flip-flops are edge-sensitive, ensuring state changes only at clock edges, leading to simpler and more predictable designs.

## Question 2 (20)

A) Consider the following CMOS logic circuits: What is the function for each? **(5points)**

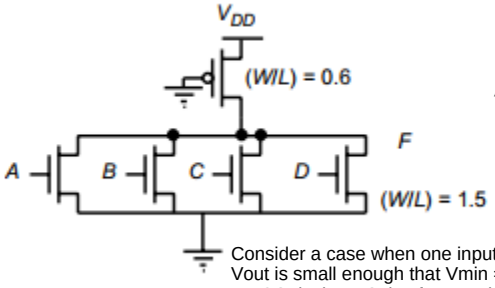


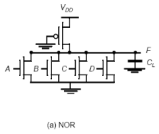

The circuit is a NAND gate

Figure 0.1: Two static CMOS gates.

Yes, they implement the same logic function :
F = (ABCD + E) = (A + B + C + D).E

B) For the circuit below, what is the output voltage if only one input is high? If all four inputs are high? Explain your answer. **(4 points)**



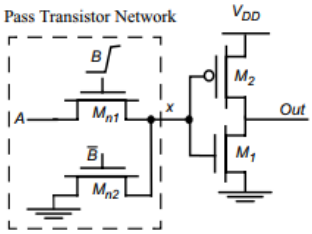



Any High will give the answer as low so , in both answers it will be low output since its nor gate

Ratioed Logic (pseudo-NMOS style)

Consider a case when one input is high: A = VDD and B = C = D = 0 V. Assume that Vout is small enough that Vmin = VDSAT for the PMOS device, and Vmin = VDS = Vout for the NMOS devices. Solve for Vout by setting the drain currents in the PMOS and NMOS equal to each other, |IDP| = |IDN|, where the drain currents are functions of Vout, VDD, and the device parameters.

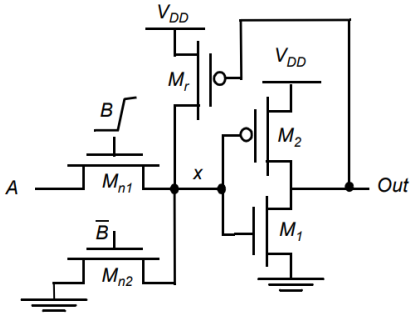
C) Explain why the circuit below has **non-zero static power** dissipation. **(5 points)** Using only just 1 transistor, design a fix so that there will not be any static power dissipation. Explain how you chose the size of the transistor.




The circuit is a NAND gate

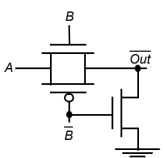
When A=B= VDD, the voltage at node x is VX=VDD-VtN. This causes static power dissipation at the inverter the pass transistor network is driving.

The modified circuit is shown in the next figure.




The size of $M_r$ should be chosen so that when one of the inputs A or B equals 0, either $M_{n1}$ or $M_{n2}$, would be able to pull node X to $V_{DD}/2$ or less.

The circuit is shown below.



D) What function does this layout represent? **(6 points)**

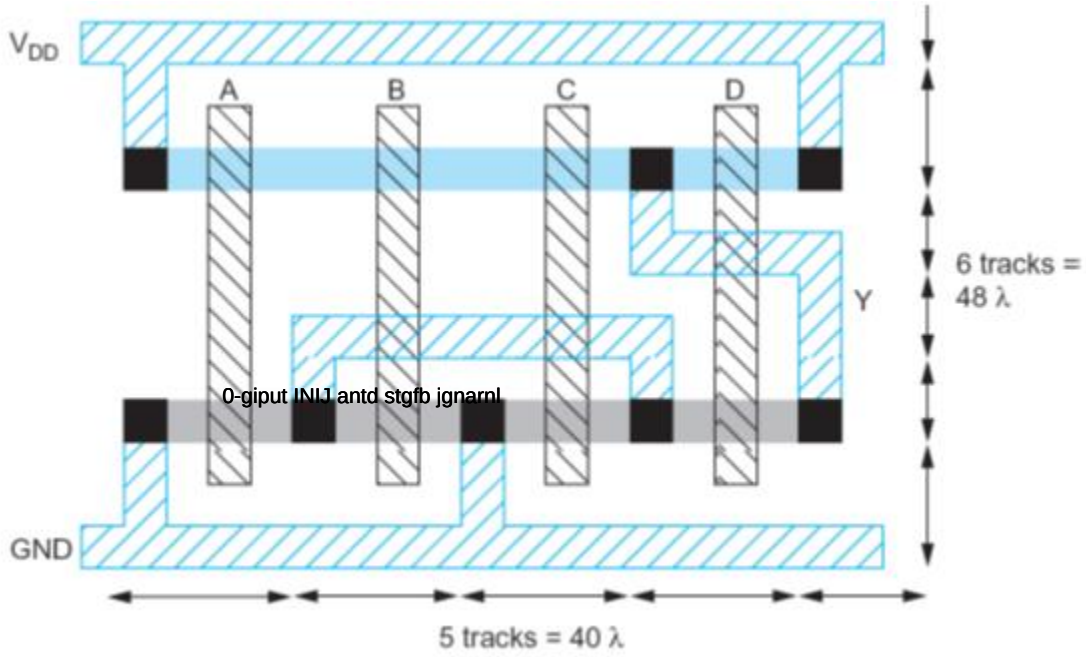



**FIGURE 1.47** CMOS compound gate for function $Y = \overline{(A + B + C) \cdot D}$

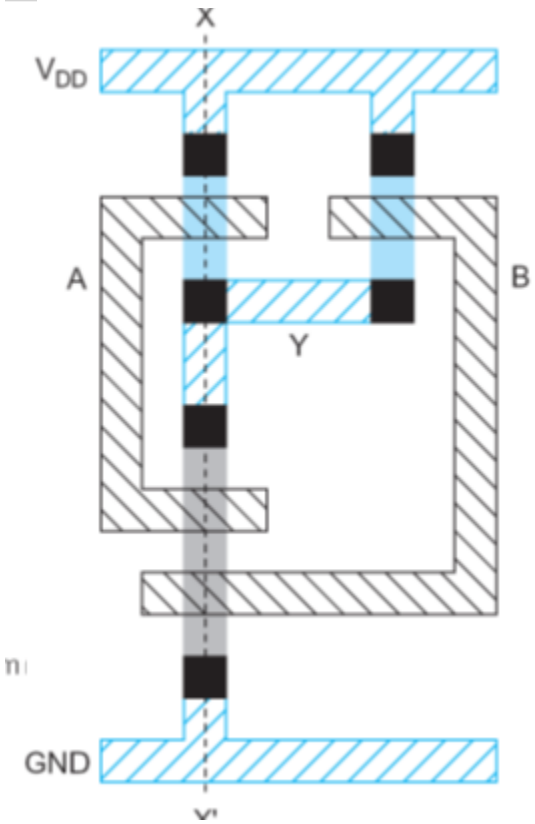



**FIGURE 1.74** 2-input NAND gate stick diagram

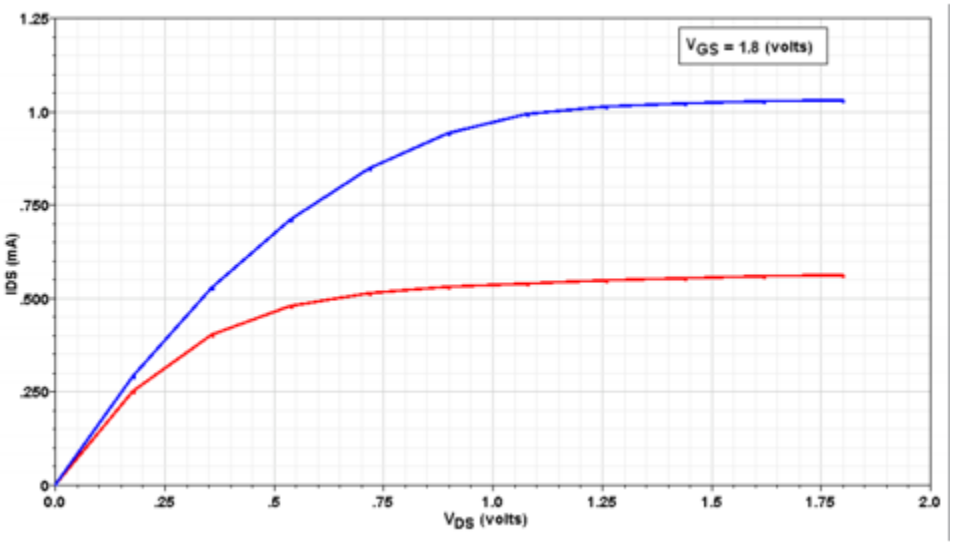
NAND GATE

## Question 3 (20)

A) If we simulate using 0.18 µm CMOS technology environment, the following two CMOS transistors (NMOS type) and we plotted the VDS versus ID for a VGS = 1.8 volts afte we Sweep VDS from 0 volt up to 1.8 volts using 9 steps

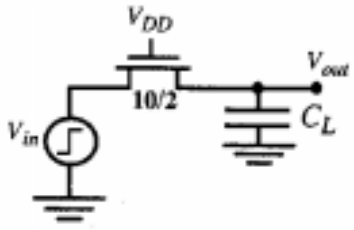
Transistor no.1: was L1 = **0.18 µm** & W1= 5*L1
Transistor no.2: L2 = **1.2 µm** & W2= 5*L2

Below graph shows the simulation results, What do you conclude from comparing both plots , which transistor for which curve? **(6 points)**




B) Consider the following below circuit :

$C_L$ can be assumed to be large and equals 10 pF.




a. Assume that $V_{out}(t = 0) = 0$ V. Determine $V_{out}$ (t = ∞) when $V_{in}$ is raised from 0 V to $V_{DD}$ at $t = 0$. Assume $V_{DD} = 3$ V. You may assume that $L = L_{eff}$, or that the lateral diffusion can be ignored in this problem. **(4 points)**

c. Determine the energy that is stored on $C_L$ at the end of the low-to-high transition. How much energy was dissipated in the MOS transistor? How much was delivered by the input source? **HINT: Derive the results; Do not take the equations in the book for granted!** **(6 points)**

d. Assume that the NMOS is replaced by a PMOS device of the same size with its gate connected to GND. Determine the impact on the following design parameters, and give a short explanation

**(6 points)**

1. $V_{out}$ (t = ∞)
   - o Larger
   - o Equalm
   - o Smaller

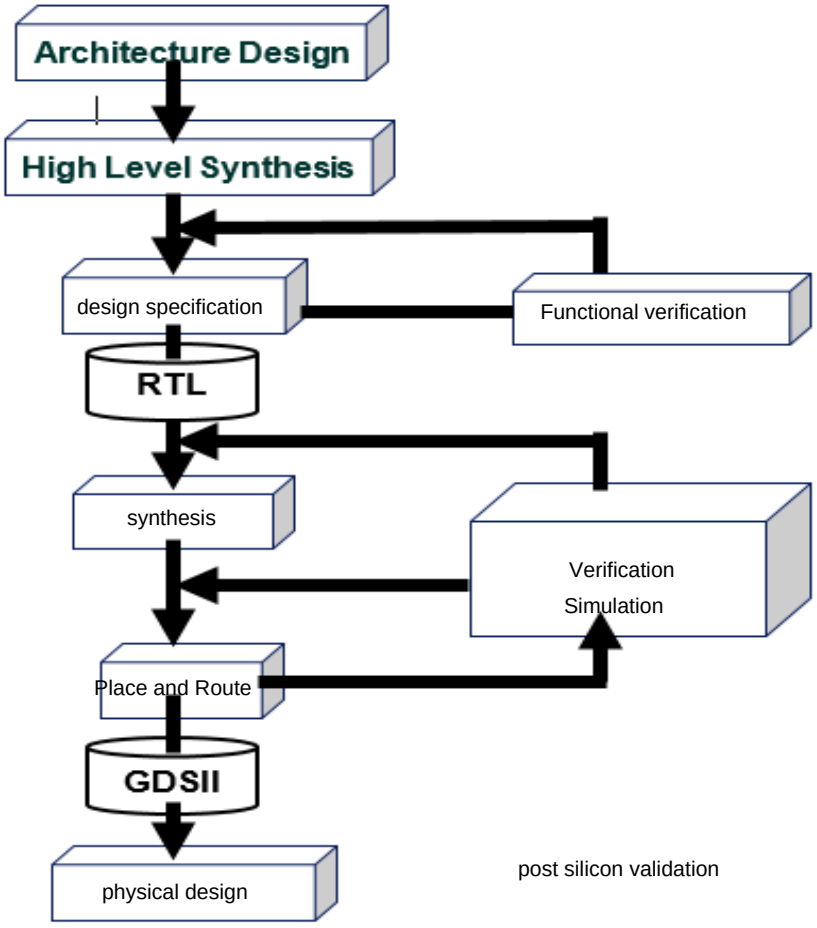
2. $t_{pLH}$:
   - o Larger
   - o Equalm
   - o Smaller

e. Describe in a couple of sentences how you would decrease the delay of this gate. Is there an absolute lower limit on the delay, and if yes explain why and give an approximate value of this delay.:

**(3 points)**

Question 4: (20 points)

A) Complete the missing block name from the level design flow for chip/IC (6 points)




B) The transistor **current changes** with the operating temperature mainly through the mobility and Vt temperature dependences. Explain how does Te temperature affect the current? **( 2 points)**

Carrier Mobility (μ): Decreases with increasing temperature, leading to a reduction in current.
Threshold Voltage (V_t): Decreases with increasing temperature, which can increase the current in certain operating regions but often leads to increased leakage current in the off state.

C) When the hot-e happens (which region of operation) and how can we avoid it? **( 2 points)**

saturation region of operation of MOSFETs. In this region, the electric field is strong near the drain, which accelerates electrons to high energies.

Design Techniques to Avoid Hot-Electron Effect:
Scaling Down Voltage: Reducing the supply voltage (VDD) reduces the electric field, thus lowering the energy gained by the electrons.
Channel Engineering: Techniques like lightly doped drain (LDD) structures can be used to reduce the electric field near the drain.
Use of Longer Channel Devices: In critical regions where the hot-electron effect is prominent, using devices with slightly longer channel lengths can mitigate the issue.
Use of Low-Power Techniques: Applying low-power design techniques to reduce the overall power dissipation can also help in minimizing the hot-electron effect.

D) What are the main three Physical Synthesis Steps? **(3 points)**

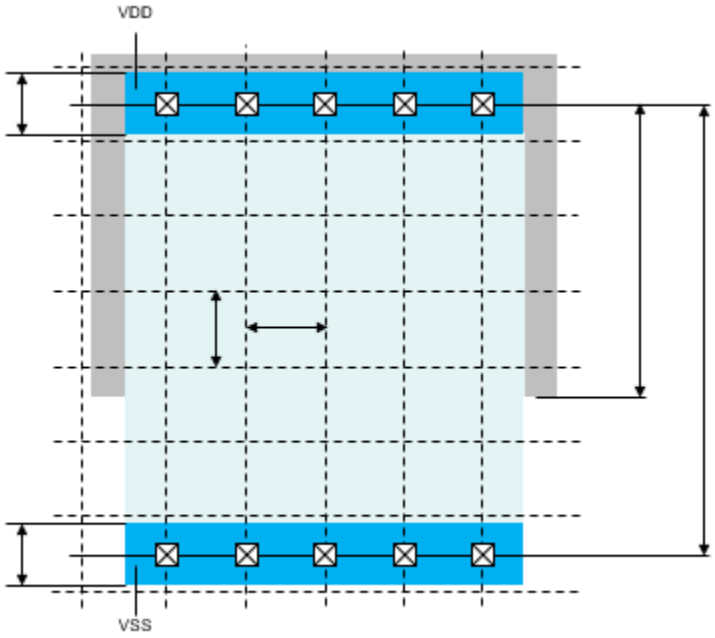
Placement: Determining the optimal positions of standard cells and macro blocks within the chip area to minimize wirelength and meet timing constraints.
Clock Tree Synthesis (CTS): Designing a clock distribution network to ensure the clock signal reaches all sequential elements (flip-flops, latches) with minimal skew and jitter.
Routing: Connecting all the placed cells according to the netlist while minimizing wirelength, crosstalk, and ensuring the design meets timing and signal integrity constraints.

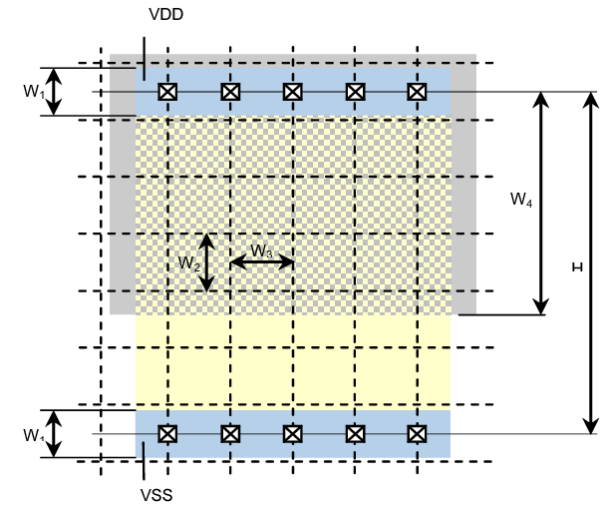
E) Is it true that all clock pins are driven by a single clock source for the same chip? If yes/no explain why? **(2 points)**

No, Different Performance Requirements: Different parts of the chip may require different clock frequencies to optimize performance and power consumption.
Power Management: Separate clock domains can be powered down independently to save power.
Clock Domain Crossing: Managing timing and synchronization between different clock domains requires careful design to avoid timing errors.

F) Given that the physical structure for standard cell design is shown below, match or mark the following parameters to the cell **( 5 points)**

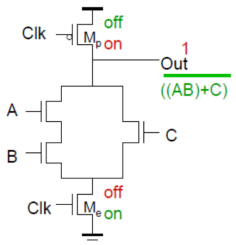
| Parameter | Symbol |
|---|---|
| Cell height | H |
| Power rail width | $W_1$ |
| Vertical grid | $W_2$ |
| Horizontal grid | $W_3$ |
| N-Well height | $W_4$ |



Question 5: (20 points)

A) Draw dynamic logic gates for F= $\overline{((AB)+C)}$ **(2 points)**




B) What are the main Issues in Dynamic Design and how we can fix/avoid ? **(2 points)**

Main Issues:
Charge Sharing:
Leakage Currents: Noise Sensitivity:
.How to Fix/Avoid:Precharge and Evaluate Phases: .Leakage Mitigation Techniques: Use high-threshold transistors, Shielding and Guard Rings:

C) Define ( 4 points)

- Setup time The minimum time before the clock edge that the data input must be stable to ensure correct data is latched
- Hold time The minimum time after the clock edge that the data input must remain stable to ensure correct data is latched.
- Clk to out delay The delay from the clock edge to the time when the output of a flip-flop or latch becomes valid.
- Data to out delay The delay from the data input to the time when the output becomes valid, considering both the setup and clock-to-out delays.

D) Based on the figure below, Assuming 100ps setup time, skew and clk-out delay **(8 points)**

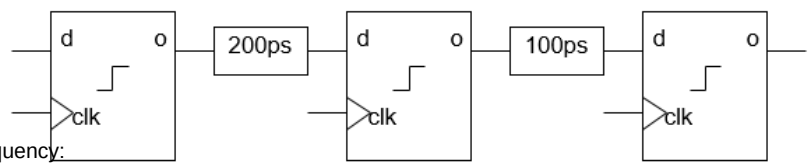
- How many paths are there and how many cycles? **( 2 points)**

  2 paths

- What is max frequency this circuit could run? **( 3 points)**

  3.33 GHZ

- What are the advantage of time borrowing? How can we benefit of time borrowing in this question ? **( 3 points)**




Increased Clock Frequency:

By effectively utilizing the clock period, time borrowing can help achieve higher clock frequencies, which translates to better performance of the circuit.
Mitigation of Variability Effects:

Balancing Pipeline Stages:Time borrowing helps in balancing the timing of pipeline stages, making sure that no single stage becomes a bottleneck due to an excessively long critical path. This leads to a more uniform distribution of delays across the pipeline.

Improved Timing Margins:

By allowing critical paths in one stage to borrow time from subsequent stages, time borrowing helps to meet timing constraints more easily. This can lead to an overall improvement in the circuit's ability to run at higher clock frequencies.



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By allowing critical paths in one stage to borrow time from subsequent stages, time borrowing helps to meet timing constraints more easily. This can lead to an overall improvement in the circuit's ability to run at higher clock frequencies.

Question 6: **(20 points)**

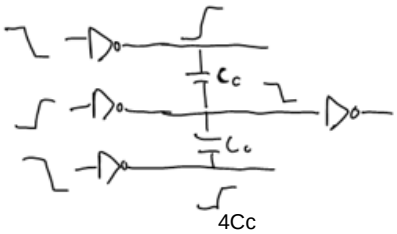
A) What are the two line model? **( 2 points)**

Two Line Model: Describes the interaction between two parallel conductors considering mutual and self-capacitance and inductance.

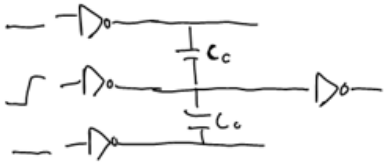
B) Why and where we use repeaters? **( 3 points)**

Why: Restore signal strength, reduce delay, minimize crosstalk.
Where: Long interconnects, high-frequency signals, critical timing paths.
Coupling Capacitance:
Definition: Capacitance between adjacent conductors.
Effect: Causes crosstalk and signal integrity issues.
Figures: Closely spaced parallel lines have higher coupling capacitance.

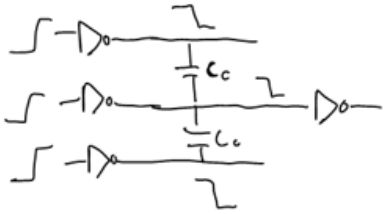
**E)** What is Coupling Capacitance? Which of the below figures have bigger coupling caps? **( 4 points)**




4Cc



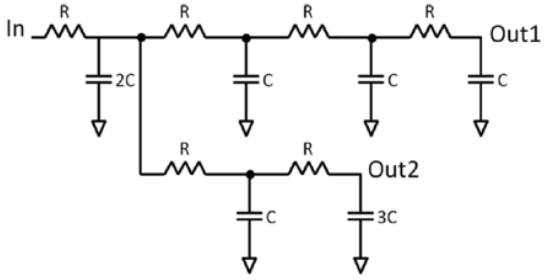

2Cc




Zero

Capacitive coupling is the transfer of alternating electrical signals from one segment of a circuit to the other using a capacito

F) Calculate Elmore delay from In to out1 and from In to out2? (5 points)

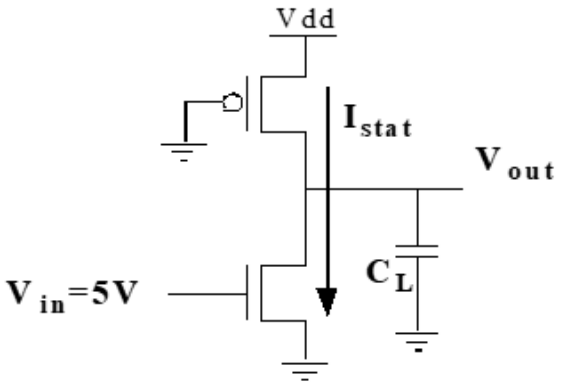



Elmore to out1 is 15RC
Elmore to out2 is 16RC

out1 = R (2C + C+3C) + (R+R)C + (R+R+R)C + (R+R+R+R)C = 6RC + 2RC + 3RC + 4RC = 15 RC

out2 = R(2C +C+C+C)+ (R+R)C + (R+R+R)3C = 5RC + 2RC + 9 RC = 16 RC

G) What kind of power dissipation in each circuit below : ( 3 points)




Pstat = P(In=1).Vdd . Istat

Dominates over dynamic consumption
- Not a function of switching frequency

H) What type of power we define as : $P = \alpha f C V_{DD}^2$ , what does each factor represent and how it affect the power ? ( 3 points)

Types of Power:
Dynamic Power: Due to charging and discharging of capacitors.
Short-Circuit Power: During switching when both PMOS and NMOS are momentarily on.
Leakage Power: Due to subthreshold leakage and gate oxide leakage.
Minimization Techniques:
Reduce supply voltage.
Use clock gating.
Apply power gating.
Optimize transistor sizing and threshold voltages.
Employ multi-V

t

design techniques.