Student Name : _____ ID: _____

Question	Full Grade	Student Grade	ABET OUTCOME
1	20		
2	20		
3	20		
4	15		
5	25		

Question 1: (20POINTS)

1. **Integrated circuits (IC) is a complex set of electronic components and their interconnections etched on a chip (T / F)**

2. **Role of IC Package : Package of IC providing possibilities of Power supply connections, Input and output of information signals, Protection from external environment and Heat removal (T / F)**

3. **CMOS ICs are fabricated on circular slices of silicon called** Wafers

4. **We can define the 'threshold voltage' as the V_{GS} that below it the transistor's current (I_{DS}) effectively reach maximum value. (T / F)**

5. **CMOS domino logic has**
   a) smaller parasitic capacitance b) larger parasitic capacitance c) low operating speed d) very large parasitic capacitance
6. **The IN and OUT bus lines in IC design should be in**
   a) metal b) polysilicon c) diffusion d) silicon
7. **Buffers are needed to drive**
   a) small capacitance b) large capacitance c) small resistance d) large resistance
8. **What type of power short circuit or dynamic or Leakage does the Sub-threshold current affect the most?** Leakage power

9. **Body effect will result in larger OR smaller VT? How does that affect performance of the device, does it make it Slower OR faster? (2 Point)** Larger Vt , Slower

10. **Hot-e degradation in devices happens When a MOS transistor is in Linear OR cut off OR saturation region. This affect which gate the most** gate voltage (VG **(2 Point)**
11. **GDSII file is** Layout file, Binary format **RTL/schematic/Layout file and it is in** _____ **the form of ASCI/DECEMEL/BINARY format, therefore it is not readable by the user. (2 Point)**
12. **List 2 methods used for Low power design techniques : (2 Point)**
    Clock Gating, Power Gating
13. **The design flow of IC VLSI design system is : (2 Point)**
    1. architecture design 2. Market requirement 3.Layout 4. HDL coding 5. logic design
    a) 2-1-5-4-3 b) 4-1-3-2-5 c) 5-3-2-1-4 d) 5-1-2-3-4
14. **Basic Steps/flow of Synthesis: (2 Point)**
    1- Circuit description 2. Logic Circuit 3. Layout 4. Physical Synthesis 5.Logic Synthesis

    a) 2-1-5-4-3 b) 4-1-3-2-5 c) 1-5-2-4-3 d) 5-1-2-3-4

Question 2: (20 POINTS)

A. Figure below shows IC Component. Please explain Type of design and what does each one of the following cell do : (3 points)

- **Input/Output (I/O) Cells :**

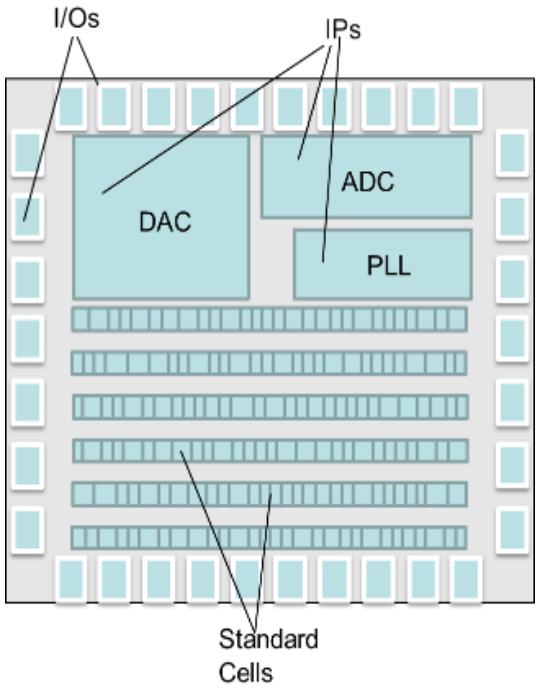
Function: These cells are responsible for interfacing the internal logic of the IC with the external environment. They handle the communication of signals between the IC and other components or systems.
Details: I/O cells typically include ESD protection circuits, level shifters, and input/output drivers. They ensure that the signals are within the correct voltage levels and are protected from electrostatic discharge.

- **Digital Standard Cells**

Function: These cells are the basic building blocks of digital logic in the IC. They include gates like AND, OR, NOT, flip-flops, multiplexers, and other combinational and sequential logic elements.
Details: Standard cells are used to implement the digital logic functions defined in the design. They are optimized for area, speed, and power consumption and are arranged in a regular grid pattern for easy routing and placement.

- **Intellectual Property (IP) Blocks :**

Function: These blocks are pre-designed and pre-verified modules that perform specific functions. They can be reused across different designs to save development time and ensure reliability.
Details: IP blocks can include processors, memory controllers, interfaces like USB or Ethernet, and other complex functions. They are integrated into the IC design to provide advanced functionality without the need to design these components from scratch.

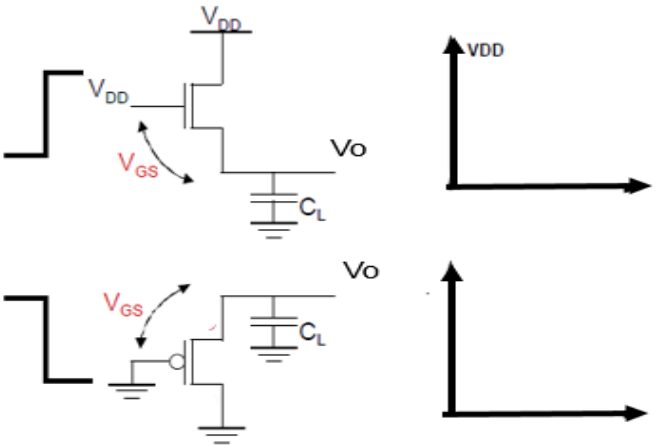


B. Physical structure of devices, draw the NMOS and PMOS structure (CROSS SECTION) and label all parts for each device like Gate, Drain, source , channel, P+, N+, N-WELL, Substrate. (4 points)

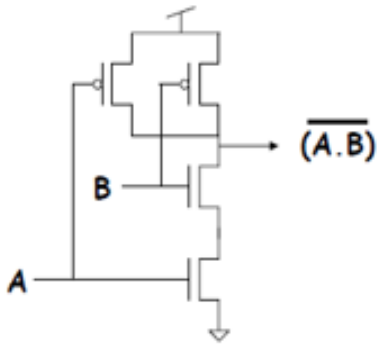
Components:
Gate: Controls the current flow between the source and drain.
Drain (D): Region where the current exits the transistor.
Source (S): Region where the current enters the transistor.
Channel: Region between the source and drain where current flows when the transistor is on.
P+ Regions: Heavily doped p-type regions for source and drain.
N-Well: Substrate region for NMOS.
Substrate (P-type): The base material for the NMOS transistor.

PMOS Structure (Cross-Section):
Components:
Gate: Controls the current flow between the source and drain.
Drain (D): Region where the current exits the transistor.
Source (S): Region where the current enters the transistor.
Channel: Region between the source and drain where current flows when the transistor is on.
N+ Regions: Heavily doped n-type regions for source and drain.
P-Well: Substrate region for PMOS.
Substrate (N-type): The base material for the PMOS transistor.

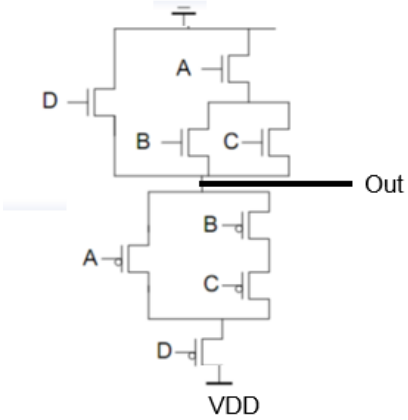
C. In the figure below draw Vo for each device and make the Source and Drain for each device (6 points)

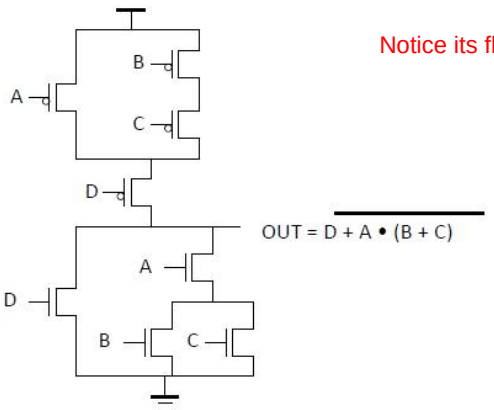


D. For the circuit below draw the complete detailed layout(5 points)



E. What is the output of this function? (2 points)





Notice its flipped , Nmos is up in the og

Question 3: (20 POINTS)

A. Draw transistor level for F= NOT ((ABC)+D) , consider D is the signal that comes the latest (5 POINTS)

B. Given the spice netlist below, draw the circuit (transistor level) (3 points)

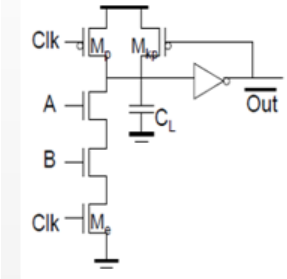
*.subckt **xxy***

mt1 out in vdd nmos l = 0.1u w = 0.75u

mt2 out in vdd pmos l = 0.1u w = 0.55u

.ends

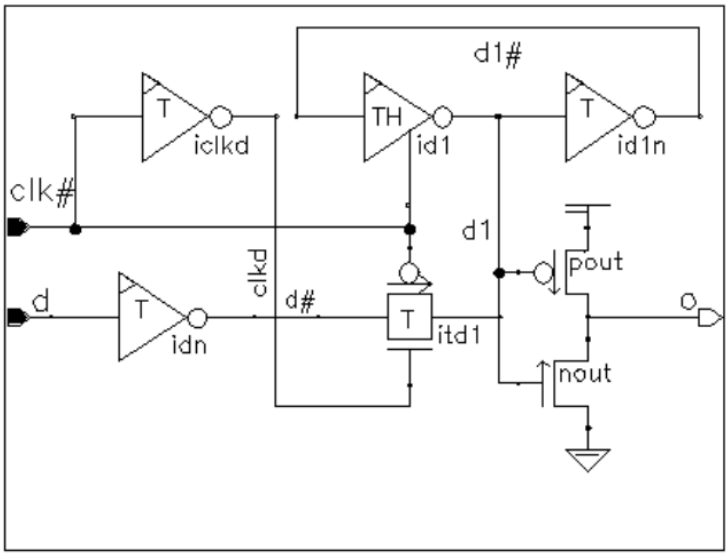
C. For the circuit shown below, what Type of circuit we have? What is the output of this circuit? What does the transistor Mkp used for? Is there another way to connect Mkp to do the same job? (5 points)



Precharge internal nodes using a clockdriven transistor
(at the cost of increased area and power)

Mkp to do the same job , Keeper

D. Draw circuit level for Traditional P-Latch (Phase 2 Latch) (using inverters symbol and transistor) (5 points)



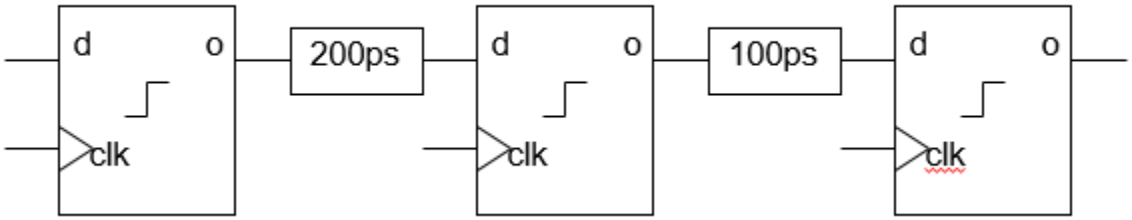
E. What are the two paths delay in the above latch OR ANY LATCH ? (2 POINTS)

The data path delay is the time it takes for a data input to propagate through the latch and produce an output. This delay is influenced by several factors, including the capacitive load on the data input, the strength of the transistors, and the configuration of the latch circuitry

The control path delay is the time it takes for a clock signal to enable or disable the data path within the latch. This delay is also known as the setup and hold time requirements of the latch, which are crucial for the correct timing of data latching.

Question 4: (15 POINTS)

A. Given the circuit below, Assuming 100ps setup time, skew and clk-out delay , How many paths are there and how many cycles? What is max frequency this circuit could run? (10 points)

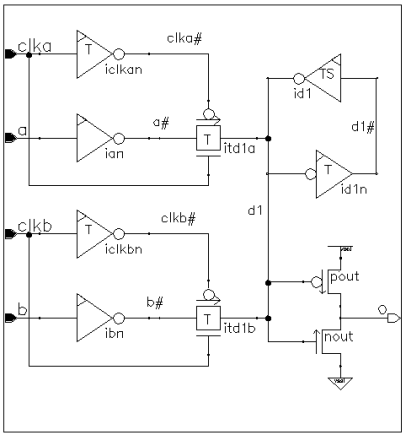


2 paths (A->B and B->C) each 1 cycle
- 200ps + 100ps = 300ps. 1/300ps = 3.33GHz
- 100ps + 100ps = 200ps. 1/200ps = 5.0GHz
- Max frequency = 3.33GHz

B. How can we increase frequency of the above system? (2 points)

Reduce Path Delays: Optimize the critical path by reducing the delay through better circuit design, faster transistors, or better routing.
Improve Clock Distribution: Ensure that the clock distribution network minimizes skew and jitter to enable higher clock frequencies.

C. What does this circuit do? (3 Points)



Mux latches
- Note selects are mutexed qualified clocks

Question 5: (25POINTS)

A. In 0.18um TSMC technology, 5x minimum inverter with effective resistance of 3Kohm , driving FO4 load (25fF) , what is delay ? if we change process to 0.10um do you expect delay to increase or decrease, explain your answer (3 points)

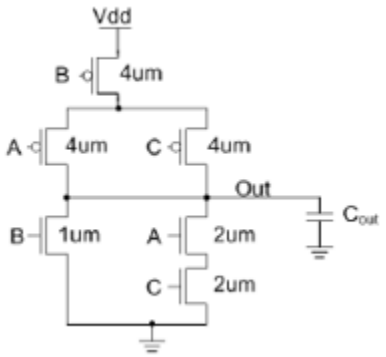
$$\text{Delay} = 3\,\text{k}\Omega \times 25\,\text{fF}$$
$$\text{Delay} = 3 \times 10^{3}\,\Omega \times 25 \times 10^{-15}\,\text{F}$$
$$\text{Delay} = 75 \times 10^{-12}\,\text{s}$$
$$\text{Delay} = 75\,\text{ps}$$

Decreased Resistance: Smaller technology nodes have lower resistance due to higher drive currents and shorter channel lengths.Decreased Capacitance: Smaller gate dimensions and reduced interconnect lengths lead to lower capacitance.

B. For the circuit shown below, (6 points)

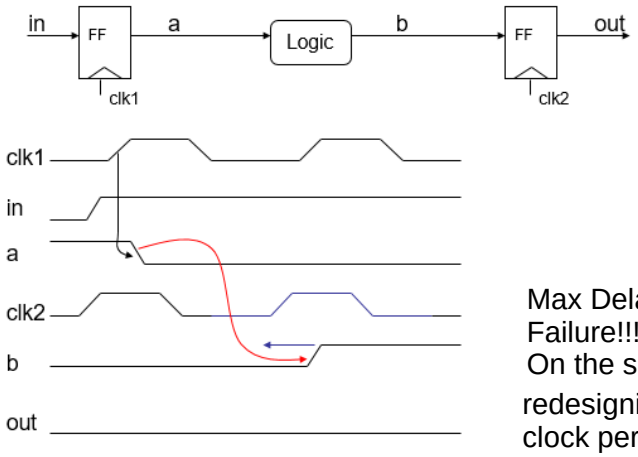
For this problem you should assume that L_{min} = 100nm, C_g=2 fF/μm, C_d=1.6 fF/μm, R_p=20 kΩ/□, and R_n=10 kΩ/□, C_{out} = 12fF.

a) If A = 1 and B = 0, draw the switch model you would use to calculate the delay of the gate when C transitions from 1 to zero (i.e., the output going high).



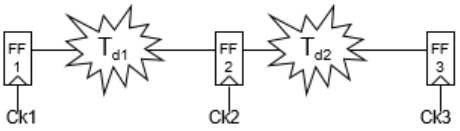
b) What is the delay of the gate in this case?

C. For the circuit below, based on timing diagram what type of failure we have ? How can you fix it? (3 points)



Max Delay
Failure!!!
On the second ff
redesigning the logic to be faster or by increasing the clock period
or adding a buffer.

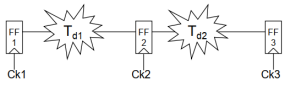
F. What is the Setup Margin in the circuit below from FF1→FF2 (5 points)



T_{d1}	0.185	T_{d2}	0.155
Clk->Q_{FF1}	0.023	$Setup_{FF1}$	0.038
Clk->Q_{FF2}	0.025	$Setup_{FF2}$	0.037
Clk->Q_{FF3}	0.024	$Setup_{FF3}$	0.041
$MaxSkew_{Ck1-Ck2}$	0.015	$MaxSkew_{Ck2-Ck3}$	0.010
Tcycle	0.250	Jitter	0.016

$Margin_{hold\ FF1->FF2}$ = Clk->$Q_{???}$ + $T_{d??}$ – $Hold_{???}$ - $MinSkew_{???}$
= 18+55-25-45
= 3

$Margin_{hold\ FF2->FF3}$ = Clk->$Q_{???}$ + $T_{d??}$ – $Hold_{???}$ - $MinSkew_{???}$
=20+40-28-40
=-8



T_{d1}	0.055	T_{d2}	0.040
Clk->Q_{FF1}	0.018	$Hold_{FF1}$	0.026
Clk->Q_{FF2}	0.020	$Hold_{FF2}$	0.025
Clk->Q_{FF3}	0.022	$Hold_{FF3}$	0.028
$MinSkew_{Ck1-Ck2}$	0.045	$MinSkew_{Ck2-Ck3}$	0.040

Marginhold = Clk->QFF1 + Td1 – HoldFF2 – MinSkewck1-ck2
= 0.023 + 0.185 -0.37-0.015
Marginsetup = Tcycle – Clk->QFF1 – Td1 – SetupFF2 – (MaxSkewck1-ck2 + Jitter)
= 0.250 -0.023 - 0.185 - 0.037 - (0.015+0.016)

G. What type and Where Does Power Go in CMOS logic? How we can minimize the power loss in CMOS logic? (3 points)

Dynamic Power (Switching Power):
Static Power (Leakage Power):

Lower Supply Voltage:
Capacitance: Optimize circuit design to minimize C L .Reduce Switching Activity:
Lower Clock Frequency:
Use High-Threshold Transistors:
Power Gating
Optimize Transistor Sizing:
Reduce Supply Voltage:

H. What type of clock buffers usually we have in a system? (2 points)

Inverting Buffers:Non-Inverting Buffers:Differential Clock Buffers:Clock Gating Buffers:Delay Buffers: