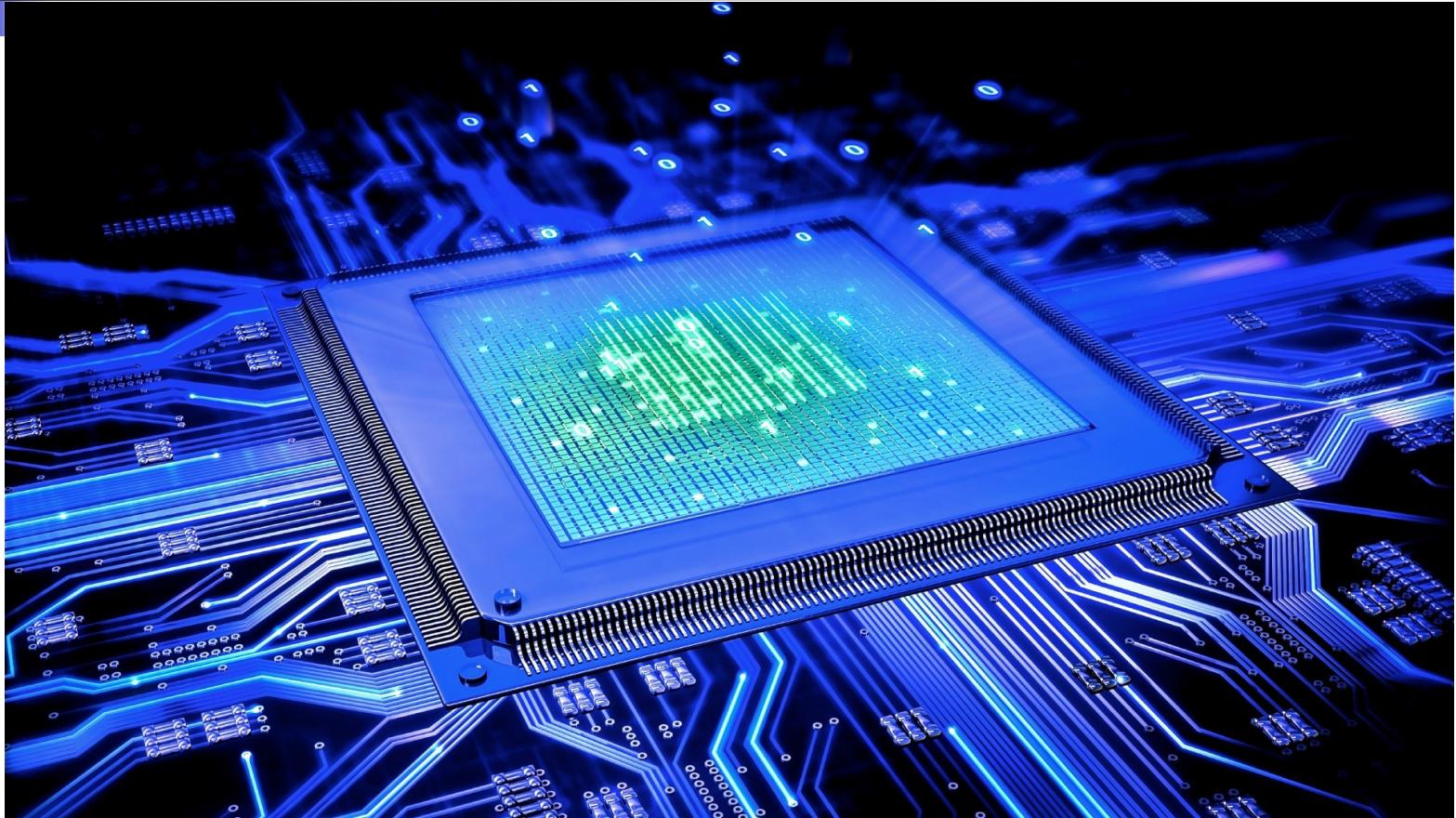
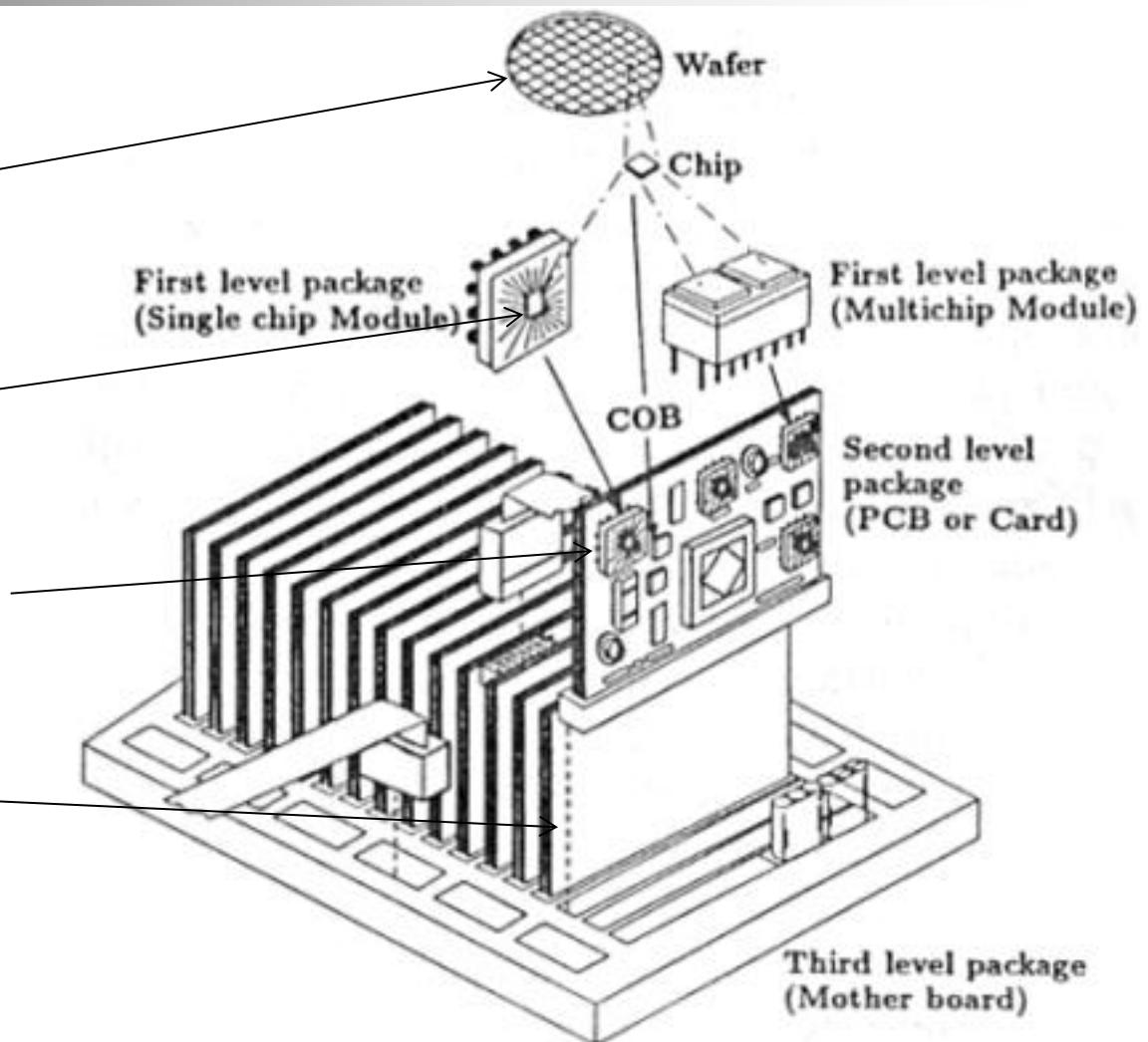


Integrated Circuit Assembly



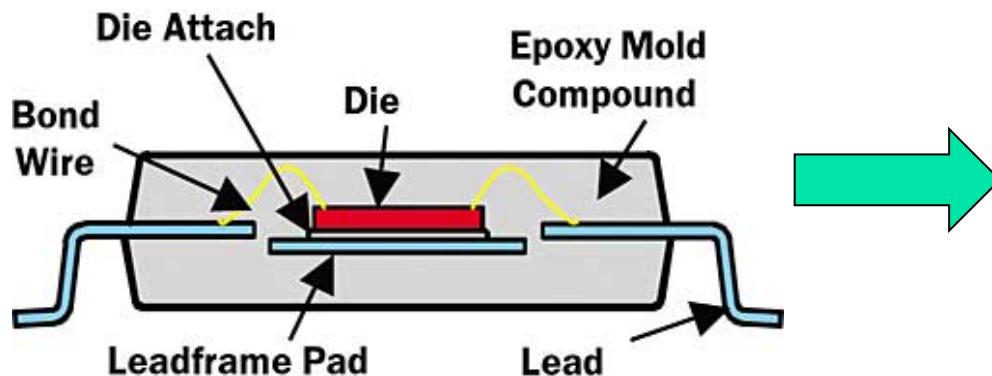
Packaging Hierarchy Review

- Level 0: Wafer level (gate-to-gate)
- Level 1: Chip level (chip-to-package)
'IC Assembly' Process
- Level 2: Board level (packaged chip to PCB)
- Level 3: System level (board-to-board)

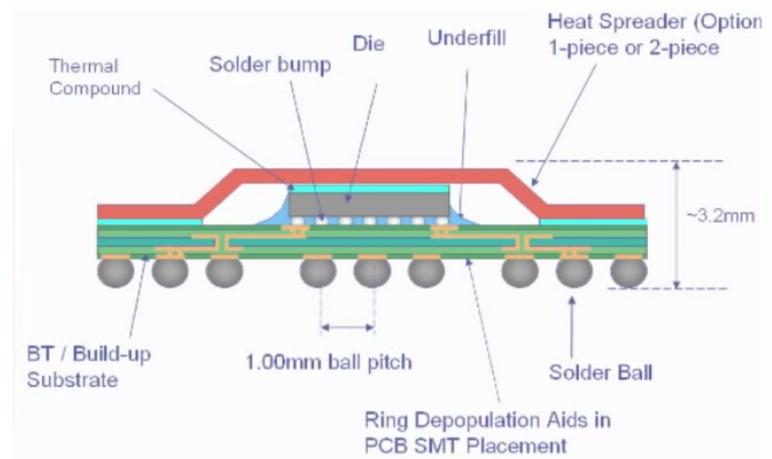


Level I Interconnect Advances

From: Active Side Up/Wire Bonds
→ To: Flip Chip/Solder bumps



Flip Chip Ball Grid Array (FCBGA)

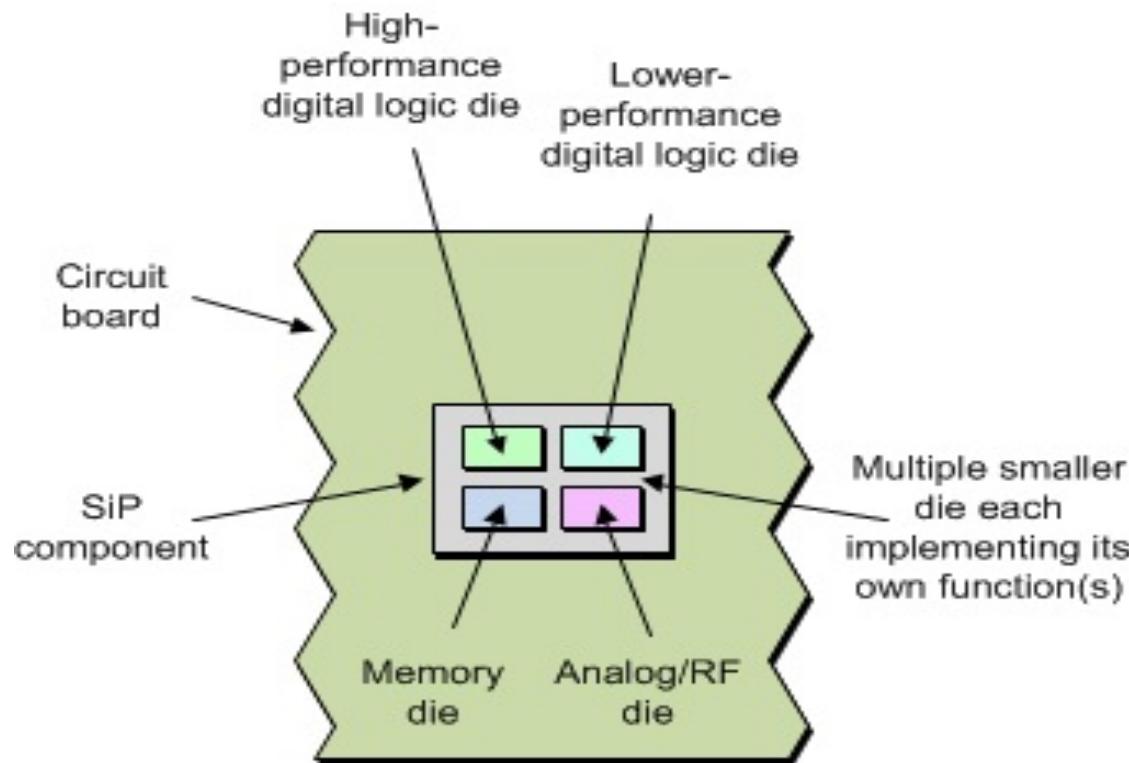


Smaller, Thinner, Lower Impedance, >I/O's

Advances in Integration

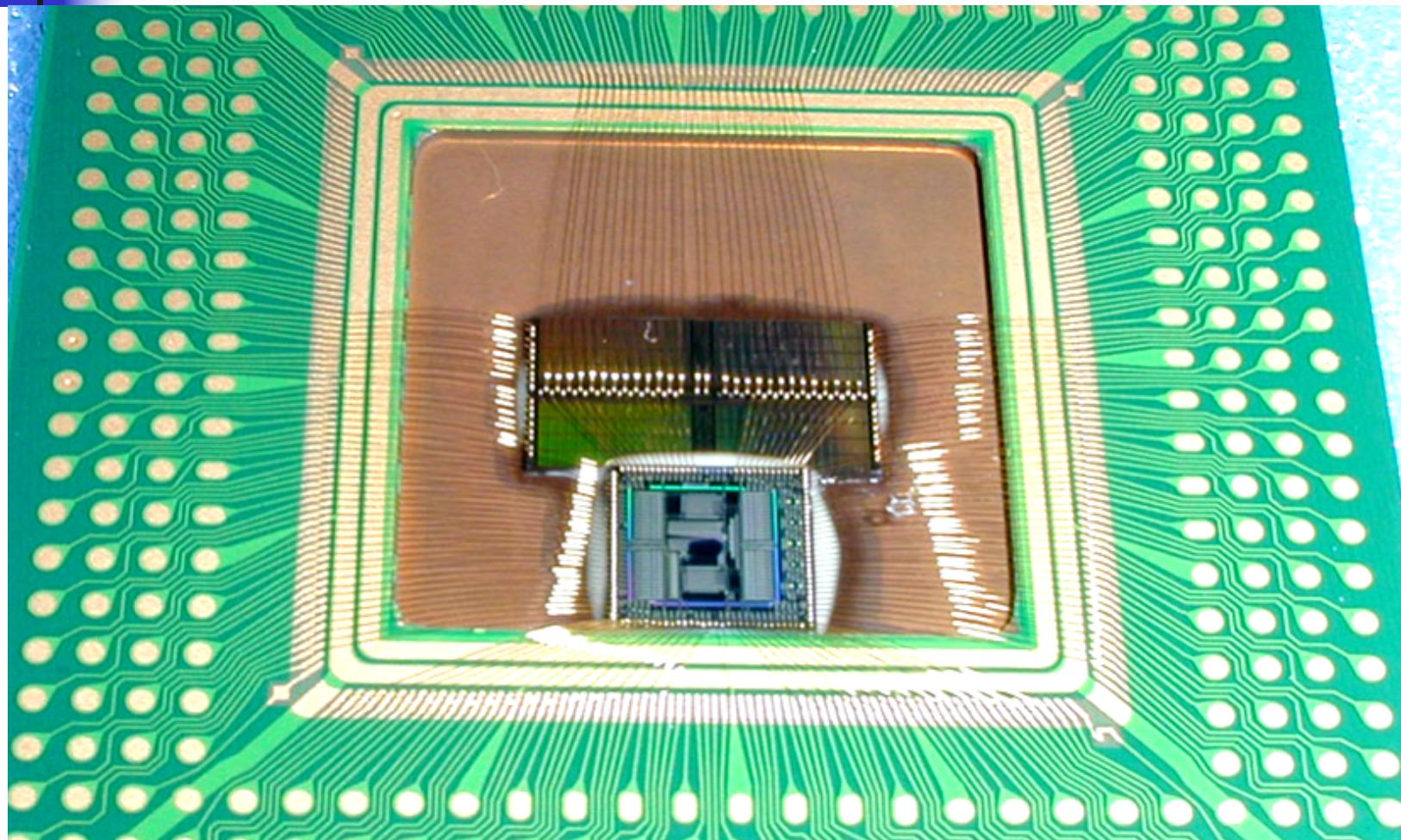
System in Package (SiP):

1. Multiple functional dies in a single package.



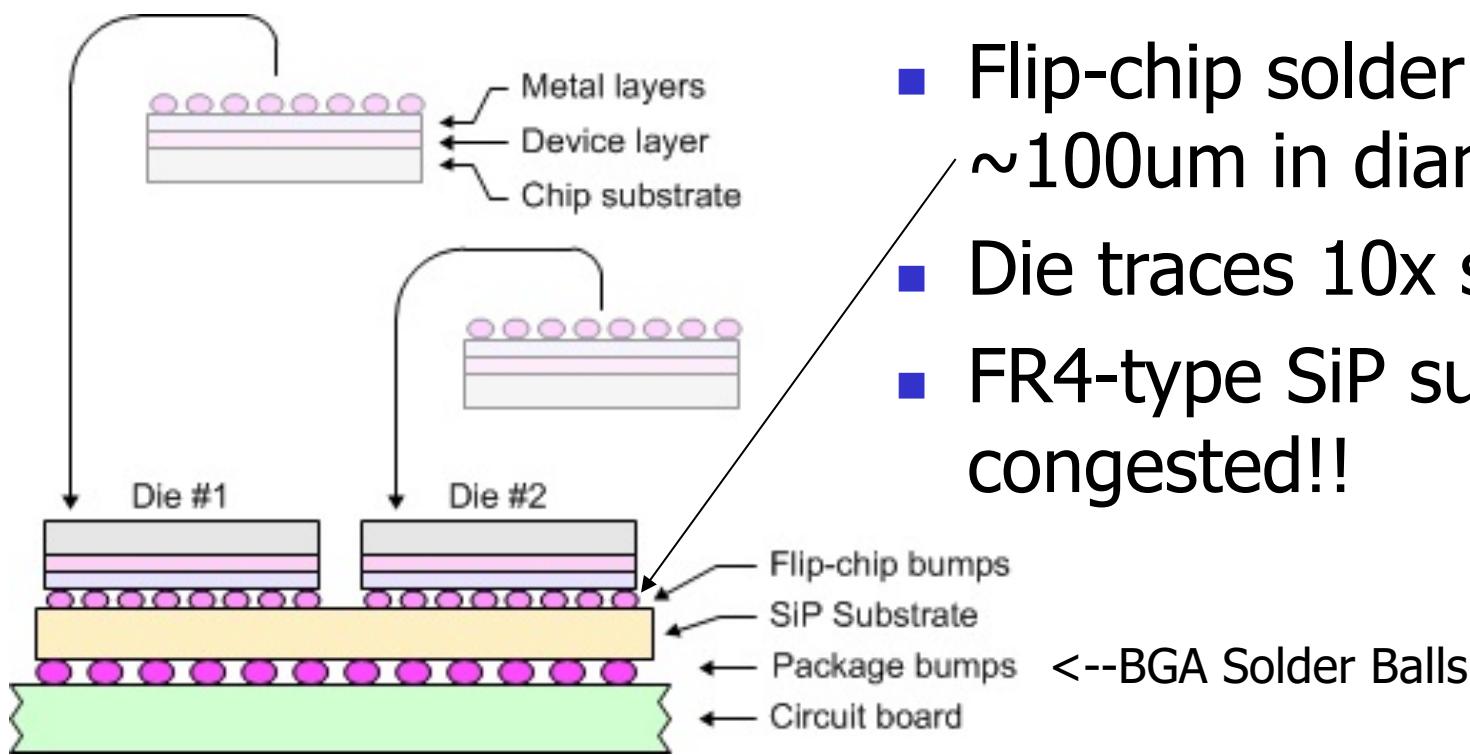
MCM – System in Package (SiP)

- For Ex: Logic + Analog/RF + Memory + A/D
- How are these dies interconnected?



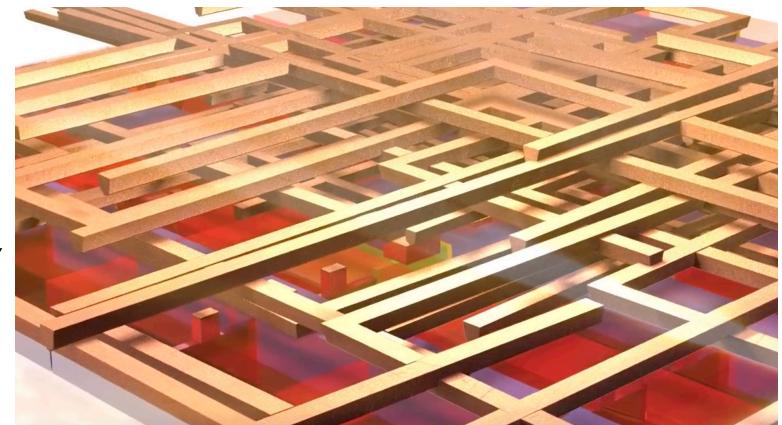
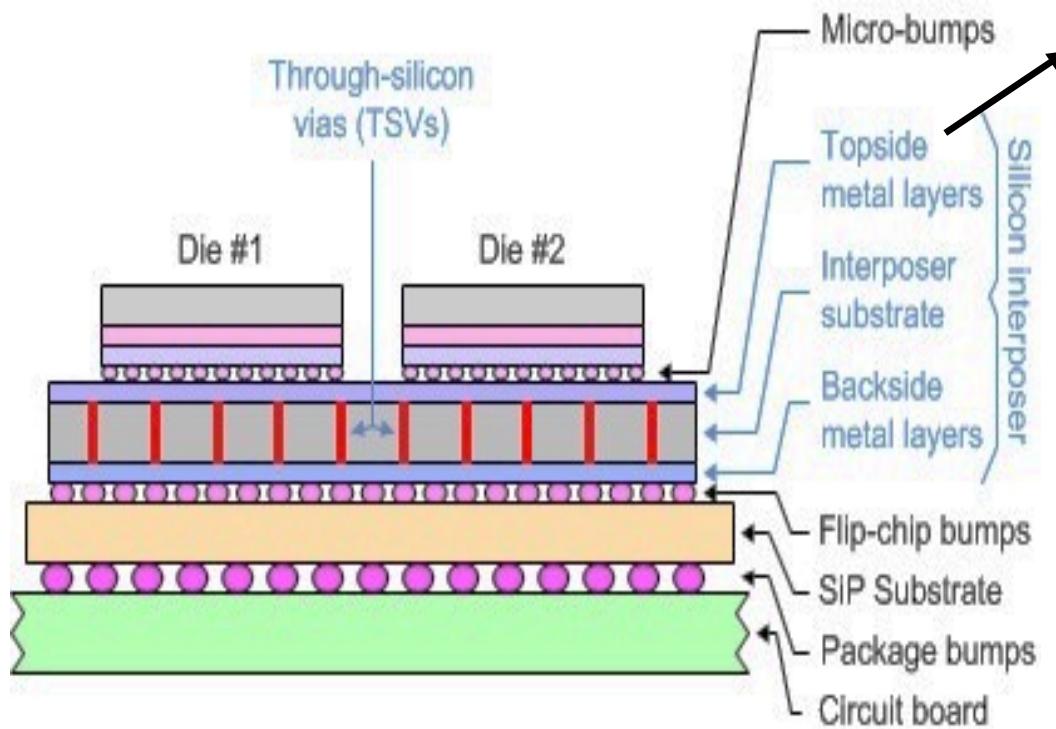
System in Package w/ Flip-Chip

- Special SiP Substrate Required



Enter: '2.5D' Silicon Interposer

■ Through-Si Via (TSV)

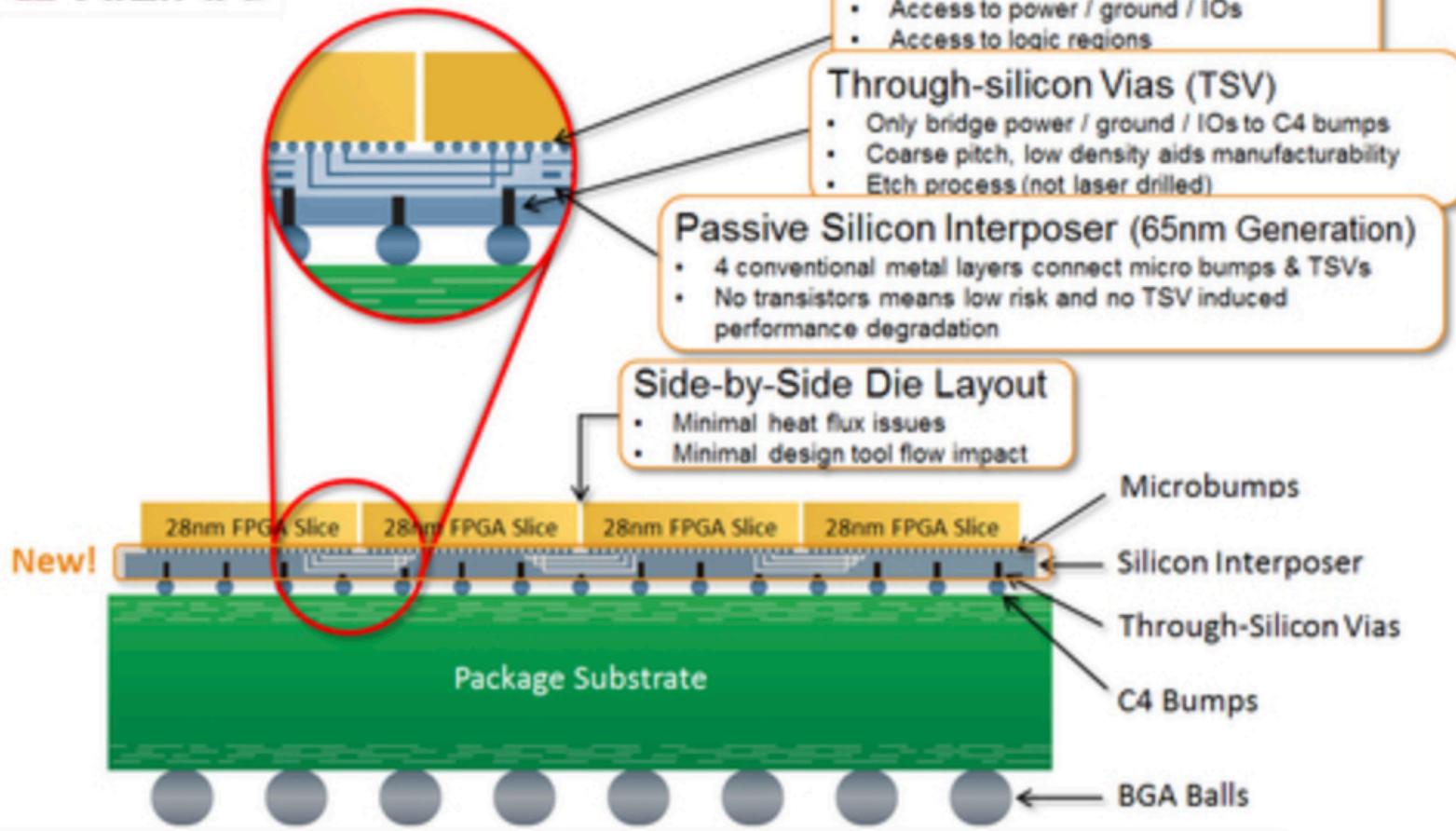


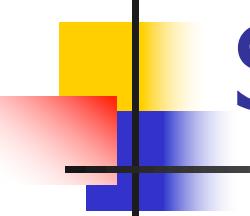
Key Interposer Features:

- Si w/ Cu-plated Vias
- Constructed using wafer manf. Process
- Micro-bumps ~10um

Not to Scale (dice & interposer ~.2mm thick!)

Si Interposer Advantages



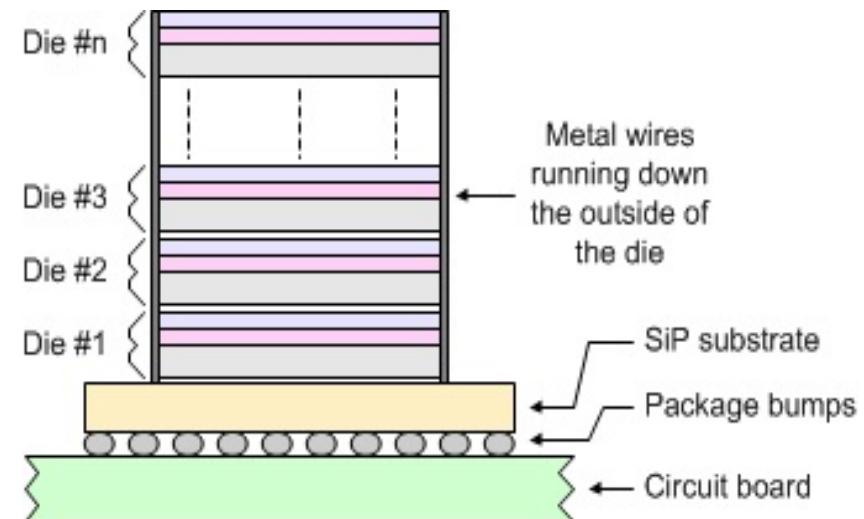
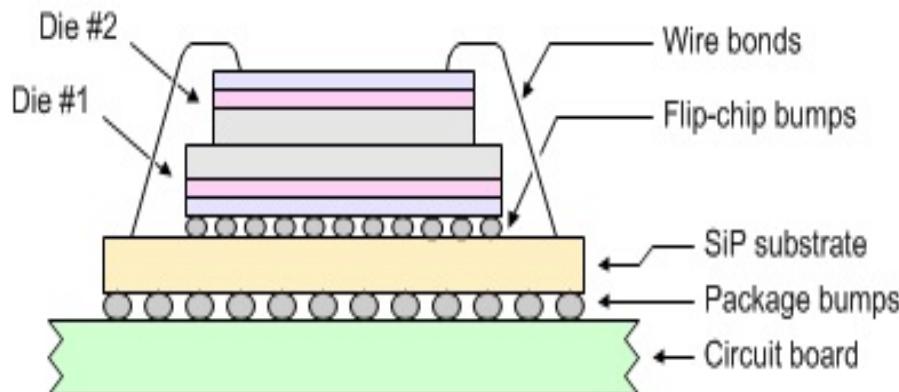


Si Interposer Advantages

- The CTE of a silicon interposer is the same as the chip, so a high density of I/O connections can be formed.
Temp changes won't cause failure.
- Due to their smoothness and dimensional stability, silicon interposers allow **smaller line widths to be printed on them than PCBs.** (1um Vs 20um)
- Infrastructure and depreciated tools **available now for chip processing** can produce silicon interposers.

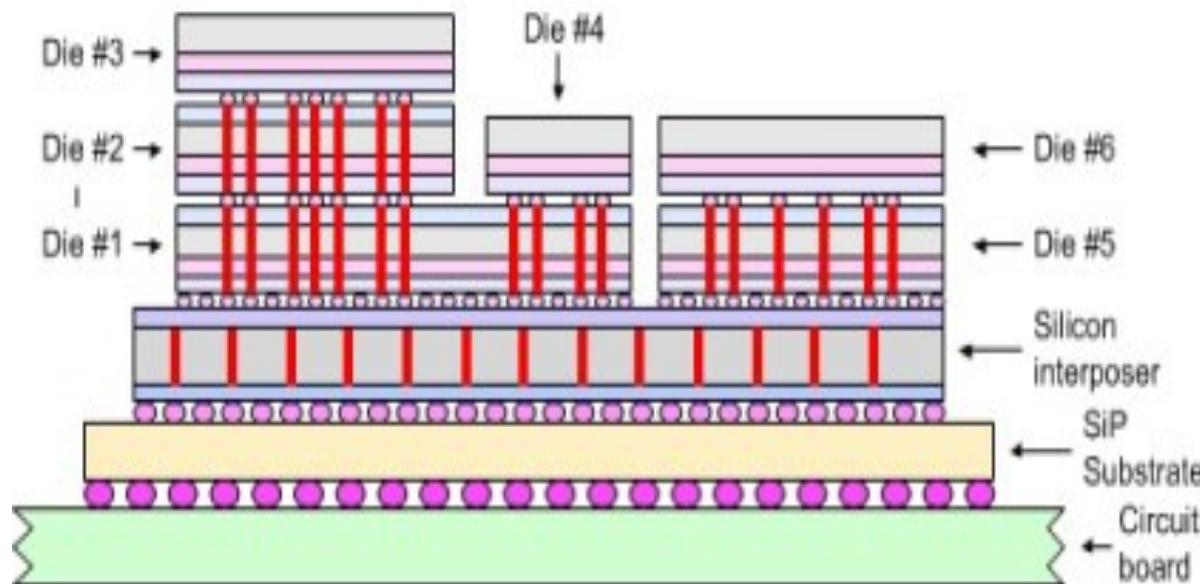
What's Next?: '3D' Packaging

- Basically – Stacked Dice (processor, memory, etc.)

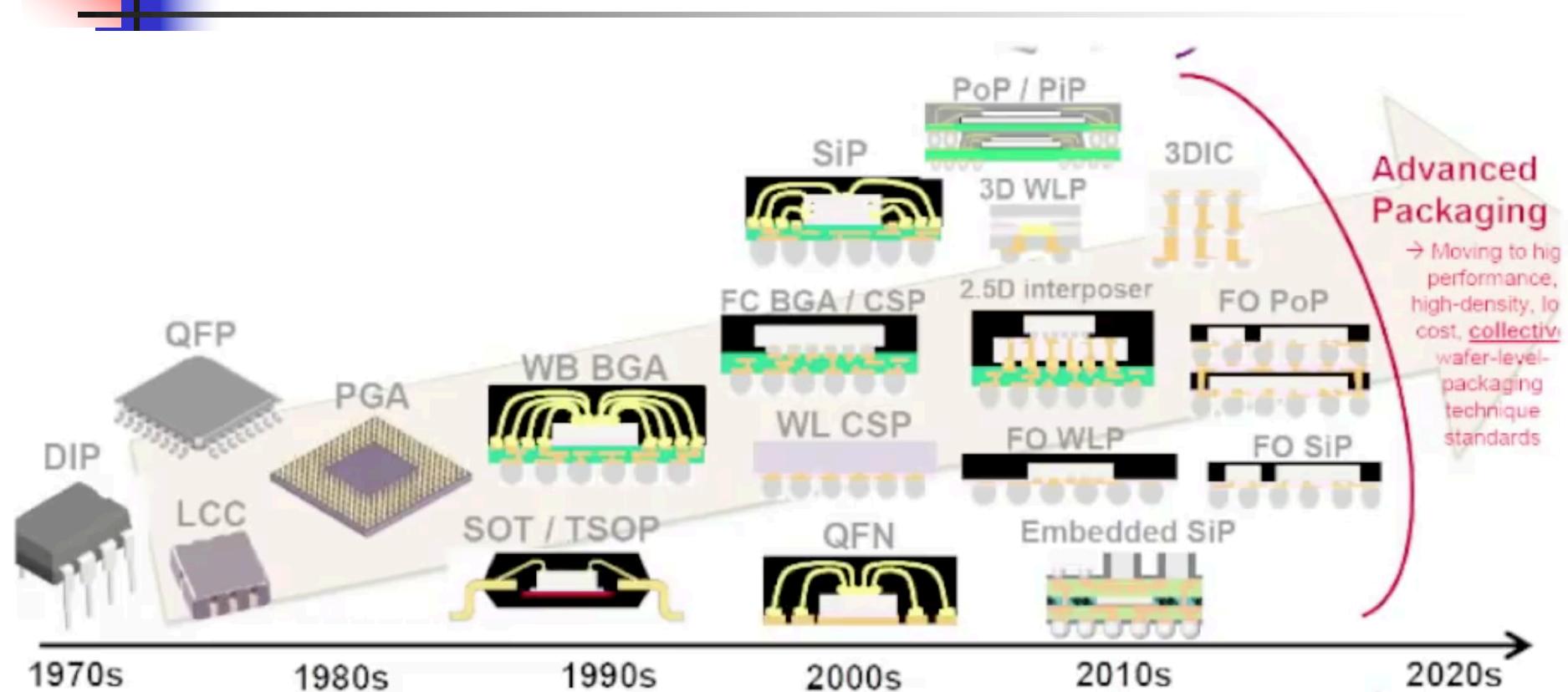


True '3D' Packaging

- Multiple Stacked Dice (processor, memory, etc. Plus sensors, MEMs)



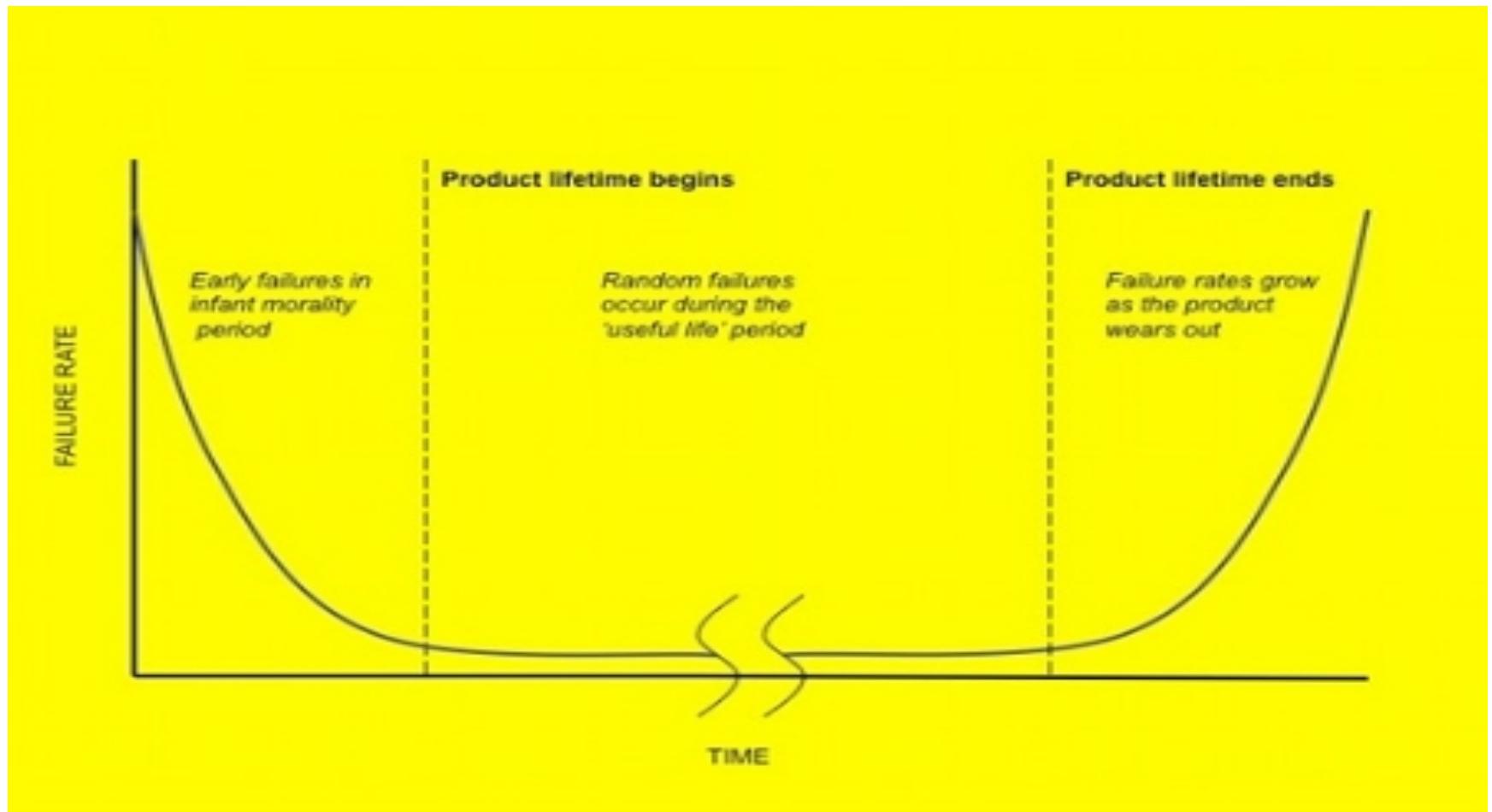
Evolution of Packaging

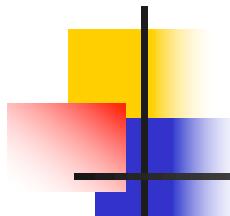


Glossary

WB BGA, SiP, FC BGA/CSP, WL CSP, QFN (Quad Flat Pack – No Lead), PoP/PiP, FO WLP, 3DIC, FO PoP, FO SiP, etc.

“Bath Tub Curve”





Electrical Testing

- Assembled board
 - Functional test
 - Verification of all circuit functionality
 - Not practical for complex circuits
 - Structural test
 - Verification circuit is constructed as designed
 - Does not directly demo circuit functionality
 - Often structural & partial functional test