Name:

CPE 133 Cal Poly Laboratory Final Exam

Closed book and notes. 100 (or so) points possible. Point values are listed in parentheses after problem number.

1. (2) What does the "HDL" in VHDL stand for?
2. (2) What is the exact cause of the glitches studied in CPE 133? Briefly explain.
3. (2) Briefly comment on the relation, if any, between a *sequential circuit* and a *sequential statement*.
4. (2) List at least two advantages to using structural modeling when modeling circuits in VHDL.
5. (2) Briefly describe what device gate-level implementations of comparators and parity generators had in common.
6. (2) Look-up tables are commonly modeled in VHDL using which type of digital device?
7. (3) Briefly describe the notions of component declaration and component instantiation in VHDL modeling.
8. (2) How many signals were used to drive the four "7-segment" displays on the Basys3 development board? Briefly describe the purpose of those signals.
9. (2) Briefly describe what the term "radix" represented.
10. (2) What is the most commonly used LUT in digital design?
11. (2) Briefly describe the two main attributes of modern digital design.