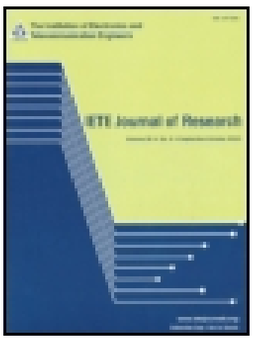

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A Novel Design of 12-bit Digital Comparator Using Multiplexer for High Speed Application in 32-nm CMOS Technology

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ABSTRACT

In the present scenario, power, speed, and area of an electronic device play a significant role specifically in the field of modern VLSI technology. In this research, small power dissipation and a less area-based single 12-bit comparator has been designed using a multiplexer. To improve the speed of the comparator a completely unique technique has applied, where three 4-bit comparator blocks have been used rather than a single 12-bit comparator. These comparator blocks compare simultaneously two signals each having 4-bits. The aim of this paper is to design and implement a 2-bit digital comparator using different logic techniques to compare power consumption, propagation delay, and transistor count. Finally, the novel technique has been applied to improve the overall performance of a 12-bit comparator. The results of this paper are simulated on the EDA tanner tool realized in 32-nanometer technology at 0.7 V supply voltage. It shows that the propagation delay of 12-bit digital comparator using the novel technique is 5.15 nanoseconds which is approximately 30% less than the proposed multiplexer-based single 12-bit comparator.

KEYWORDS

Conventional CMOS; digital comparator; multiplexer-based comparator; power dissipation; propagation delay; transistor count; transmission gate logic technique

1. INTRODUCTION

In today's world, the power consumption is a vital issue in digital CMOS circuits, wherever different methodologies are used to design circuits for low-power dissipation with small-sized and high-speed interface applications are developed [1–3].

The area of an integrated circuit not only depends upon the quantity of transistor and their sizes, but also depends on wiring complexity [4]. The wiring complixity is fluctuating from one logic technique to another logic technique and consequently, the reasonable judgement of logic style is important for circuit execution [5].

Digital comparator has several applications including Digital Signal Processing, Central Processing Unit, Microcontroller, etc. In this paper, 12-bit comparator has been designed with the low power consumption and better packing densities in 32-nanometer technology at 0.7 V supply voltage based on the multiplexer and the novel technique.

2. TWO-BIT DIGITAL COMPARATOR

A 2-bit digital comparator is a such type of logic circuit that compares the relative magnitude of two signals, each having two bits. After the comparison of two signals, it will set three output variables that will express whether A > B or A < B or A = B [6–7]. The block diagram of a 2-bit digital comparator is shown in Figure 1.

In the comparison process, the comparator will check the relative magnitude of two signals from the position of the most significant bit to the next successive bit position and so on. If most significant bits are not equal, then it will decide that either A is greater than or less than B. Otherwise check for the next successive bit position and goes on till the unequal bit position occurs [8–9]. Equations (1)–(3) are given to control the outputs of the 2-bit digital comparator [1–3].

$$A > B := A_0\overline{B}_0 + \overline{A}_0A_1\overline{B}_0\overline{B}_1 + A_0A_1B_0\overline{B}_1$$
$$= A_0\overline{B}_0 + A_1\overline{B}_1(A_0\ EX-NOR\ B_0) \quad (1)$$

$$A < B := \overline{A}_0B_0 + \overline{A}_0\overline{A}_1\overline{B}_0B_1 + A_0\overline{A}_1B_0B_1$$
$$= \overline{A}_0B_0 + \overline{A}_1B_1(A_0\ EX-NOR\ B_0) \quad (2)$$

$$A = B := \overline{A}_0\overline{A}_1\overline{B}_0\overline{B}_1 + \overline{A}_0A_1\overline{B}_0B_1 + A_0A_1B_0B_1$$
$$+ A_0\overline{A}_1B_0B_1$$
$$= (A_0\ EX-NOR\ B_0)(A_1\ EX-NOR\ B_1) \quad (3)$$

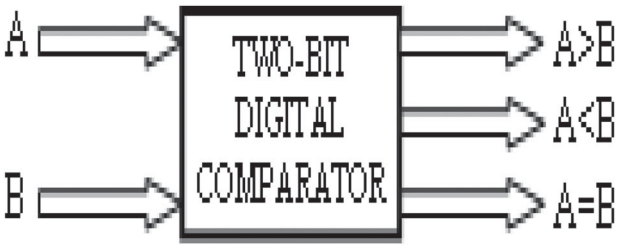

Figure 1: Block diagram of a 2-bit digital comparator.

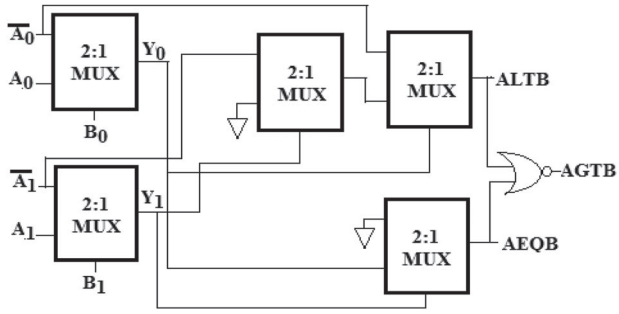

Figure 2: Design of 2-bit digital comparator using a multiplexer.

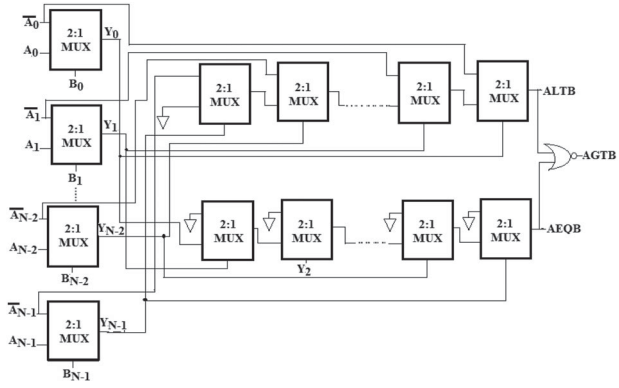

Figure 3: Design of N-bit digital comparator using a multiplexer.

3. REVIEW OF EXISTING TECHNIQUES FOR DIGITAL COMPARATOR DESIGN

According to Moore's Law, the quantity of transistors, in a chip, doubles in every 18 months. Thus, the circuit designers modify the circuit with less number of transistors for the identical functionality. In the new generation, several researchers have made CMOS comparator using various logic techniques like typical CMOS, PLT, TG, GDI and hybrid logic with different number of transistors to achieve low power consumption, high speed and less area.

Power consumption, speed and area are the three fundamental parameters to optimize the overall performance of a CMOS comparator design [10]. However, those parameters struggle with each other i.e. each individual parameter can't be optimized independently [11]. Two-bit digital comparator has been designed with the aid of Anjuli [12] the use of 40 T PTL logic style. It provides less PDP than other logic styles. Two- bit digital comparator has been designed with the aid of Shekhawat et al. [8] the use of 26 T PTL logic style. It provides less PDP and transistor count than GDI logic styles. One-bit digital comparator has been designed with the aid of Anjali and Pranshu [13] the use of four 10 T GDI full adder cells. Hassan and Mehra [14] has 1-bit CMOS comparator using three different approaches. The full-custom-based design consumes less power and takes less area than autogenerated and semicustom design. The proposed multiplexer-based two-bit comparator consisted of 18 T which is less when in comparison with the other comparator (two-bit) designs using CMOS, PTL and TG logic technique.

4. TWO-BIT DIGITAL COMPARATOR USING A MULTIPLEXER

In this technique, a digital comparator has been designed using a multiplexer. For the implementation of the design procedure using hardware, it requires two sub-block, where the first block is used to determine the equality of each single-bit data simultaneously of a 2-bit comparator. The first block is formed by using two 2:1 multiplexer. The second block is used to determine whether A is less than or equal to B. To implement the second block of a 2-bit digital comparator, three numbers of 2:1 multiplexers are required. Finally, these two outputs A < B and A = B are used as input of an NOR gate to determine whether A is greater than B or not. The multiplexer-based 2-bit digital comparator is shown in Figure 2. To implement 2-bit digital comparator , multiplexer 18 transistors are required.

Multiplexer-based N-bit digital comparator is shown in Figure 3. The number of transistors required to design a N-bit digital comparator is determined by Equation (4).

Number of transistors required = $(N+1)$ number of Inverter + N number of 2:1 MUX for block-1 + $2N$ number of MUX for block-2

$$\begin{aligned} &= (N+1) * (1p+1n) + N * (1p+1n) \\ &\quad + 2N * (1p+1n) \\ &= 8 * N + 2 \end{aligned} \tag{4}$$

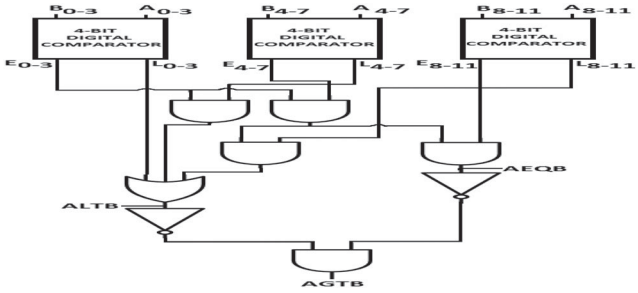

Figure 4: Novel technique-based 12-bit digital comparator.

5. NOVEL TECHNIQUE FOR HIGH-SPEED DIGITAL COMPARATOR

In today's world, the speed is a vital issue for any electronic devices. So, to achieve this demand a novel technique-based 12-bit comparator has been designed, as shown in Figure 4. This novel technique-based 12-bit comparator has three 4-bit comparator blocks which are operating simultaneously. After the comparison of each comparator blocks, they will individually decide whether A is less than or equal to B. Output of these three blocks will finally make a deceision whether A is greater than, less than or equal to B by using Equations (5–7).

$$A < B := L_{0-3} + E_{0-3}(L_{4-7} + E_{4-7} * L_{8-11}) \tag{5}$$

$$A = B := E_{0-3*}E_{4-7*}E_{8-11} \tag{6}$$

$$A > B := (A < B) * (A > B) \tag{7}$$

where L_{0-3}, L_{4-7} and L_{8-11} represents that the signal A is less than the signal B in these comparator blocks. Terms E_{0-3}, E_{4-7} and E_{8-11} shows that the signal A is equal to the signal B in these comparator blocks.

6. NOVEL TECHNIQUE-BASED 12-BIT COMPARATOR DESIGN DETAILS

The structure is divided into two stages. In the first stage, multiplexer-based three 4-bit comparator has been designed instead of a single 12-bit comparator to minimize the number of transistors and gate level. In this stage each comparator gives individual outputs of "A" less than "B" and "A" equal to "B". The output of a 4-bit comparator (A_{0-3}, B_{0-3}) is determined by Equations (8) and (9).

$$L_{0-3} = \overline{A}_0 B_0 + \sum_{K=1}^{3} [\overline{A}_K B_K \prod_{M=K-1}^{0} (A_m \odot B_m)] \tag{8}$$

$$E_{0-3} = \prod_{m=0}^{3} (A_m \odot B_m) \tag{9}$$

The second stage has been implemented by Equations (5–7) to compute the final outputs of a 12-bit comparator.

7. CONVENTIONAL CMOS LOGIC-BASED 2-BIT COMPARATOR

In the present scenario, low power and high speed are imperative factors in the field of digital VLSI circuits. Since CMOS consumes less power and provides high speed, it's thought-about because the best various style method within the digital circuit [1–3]. The conventional CMOS logic-based inverter consists of one NMOS transistor and one PMOS transistor. The gates of two transistor are shorted at where the input is applied. The drains of two transistors are also shorted. The source of the NMOS transistor is connected to the ground and the source of PMOS transistor is connected to the power supply. Output is taken from the drain terminal. The CMOS logic circuit is outlined in a way that stands out system is directing at once. The CMOS logic technique-based inverter is shown in Figure 5.

The CMOS logic style is basically associate extension of CMOS inverters to multiple inputs [15].

8. TRANSMISSION GATE LOGIC-BASED 2-BIT COMPARATOR

The transmission gate logic technique is one of the most prominent technique to design a comparator, which has low power consumption and less transistor count than conventional CMOS logic-based comparator. In this technique one NMOS and one PMOS transistors

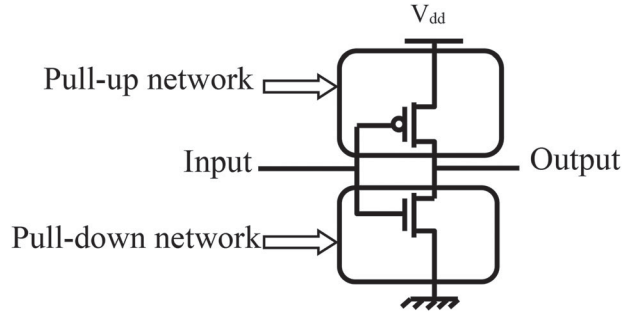

Figure 5: CMOS logic technique-based inverter.

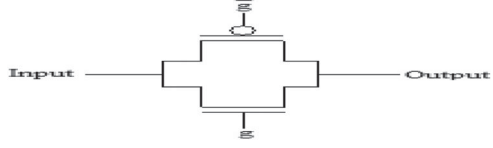

Figure 6: CMOS transmission gate.

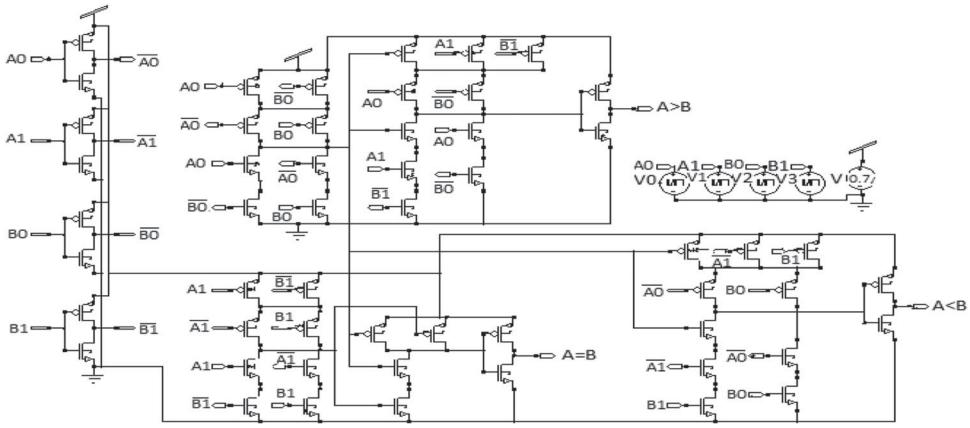

Figure 7: Schematic of the CMOS logic technique-based 2-bit comparator.

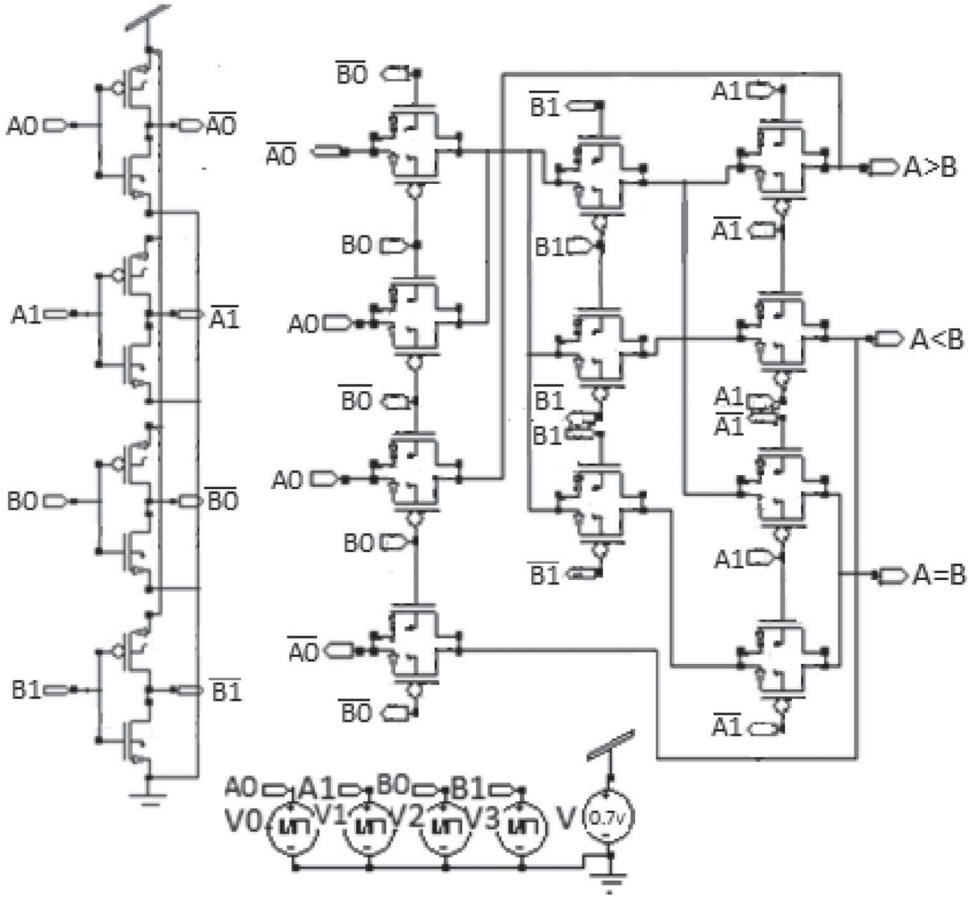

Figure 8: Schematic of the transmission gate logic-based 2-bit comparator.

are connected in parallel with complementary inputs at their gates. The CMOS transmission gate is shown in Figure 6 [3].

9. SIMULATION RESULTS

To compare the performance of the proposed comparator with the different logic techniques, EDA tanner tool has been used in 32-nanometre technology with 0.7 V supply voltage to design and implement all circuits. The schematic circuit configuration of CMOS logic and transmission gate logic-based 2-bit digital comparator are shown in Figures 7 [3] and 8, respectively. The schematic circuit configuration of multiplexer and novel technique-based 12-bit digital comparator are shown in Figures 9 and 10, respectively. The layout of

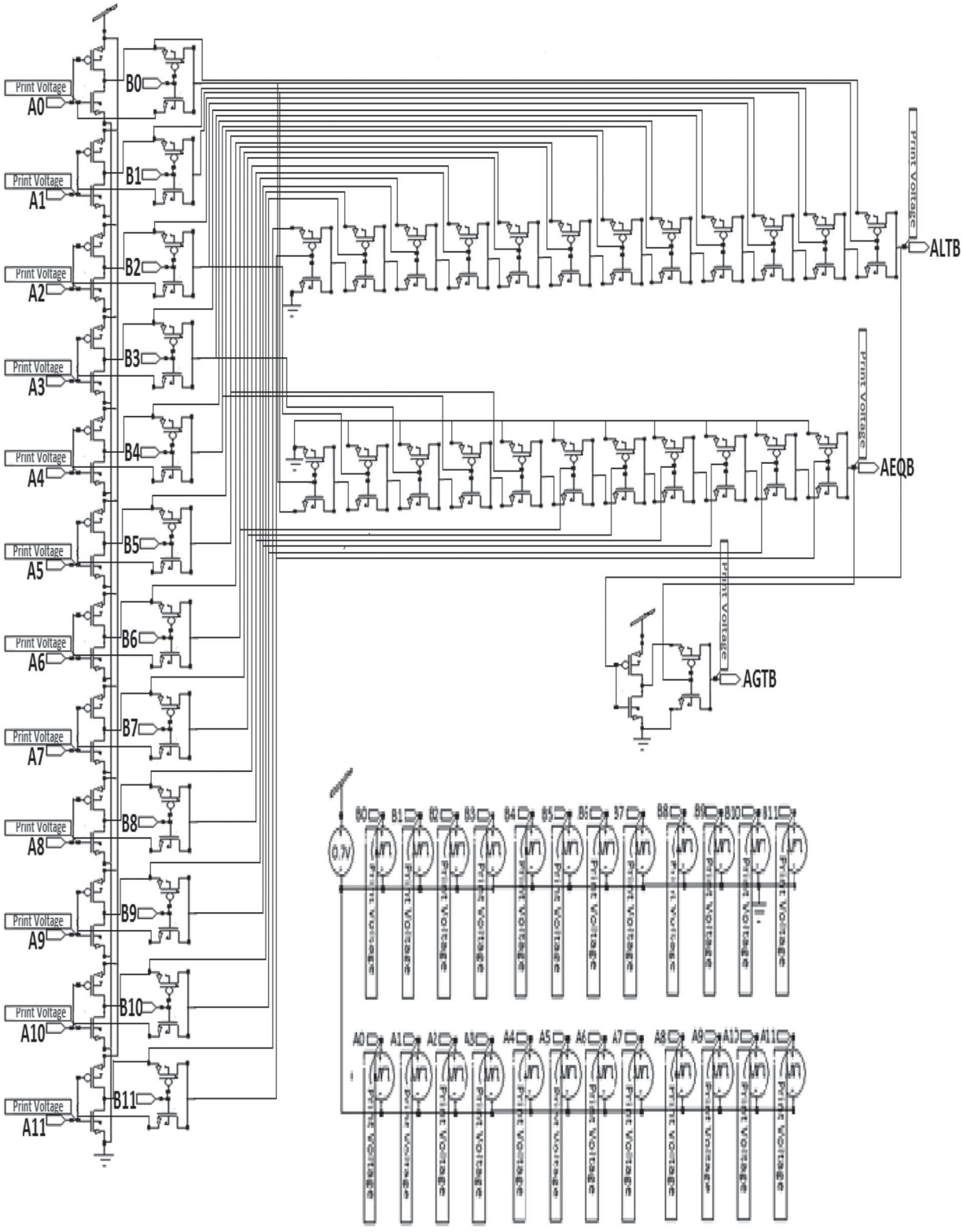

Figure 9: Schematic of the 12-bit digital comparator using a multiplexer.

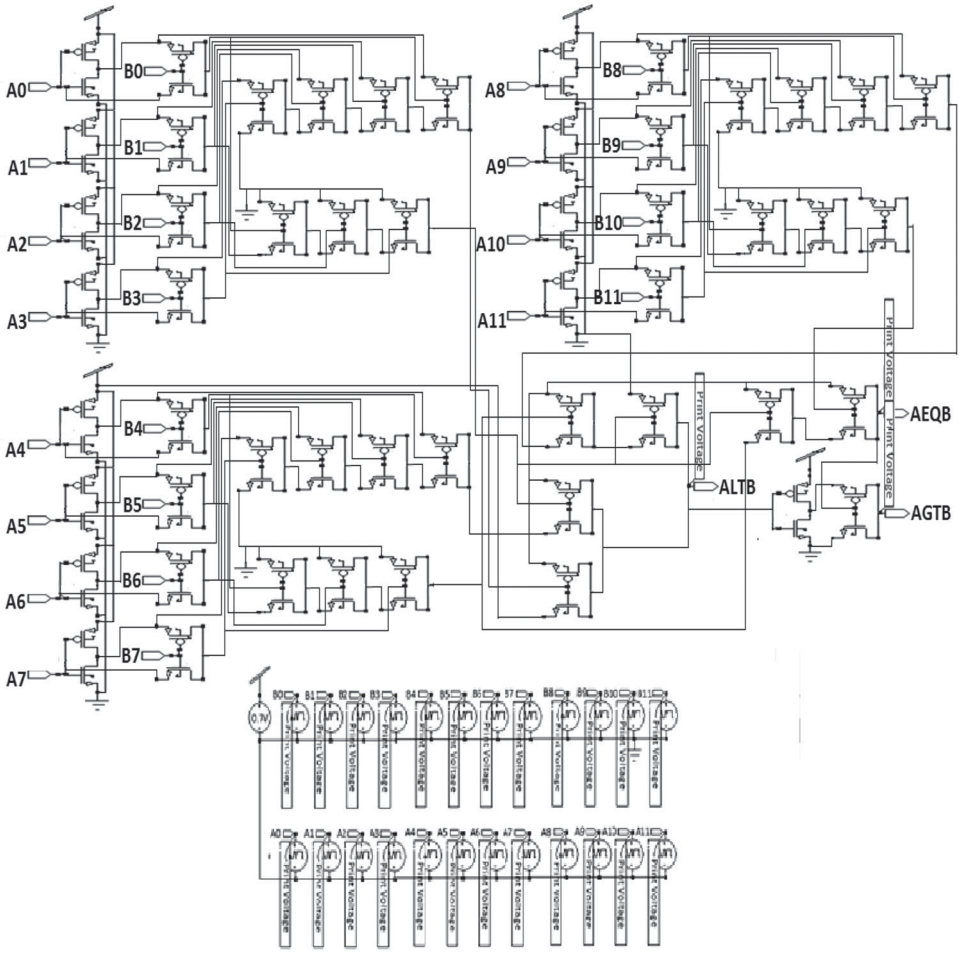

Figure 10: Schematic of 12-bit digital comparator using a novel technique.

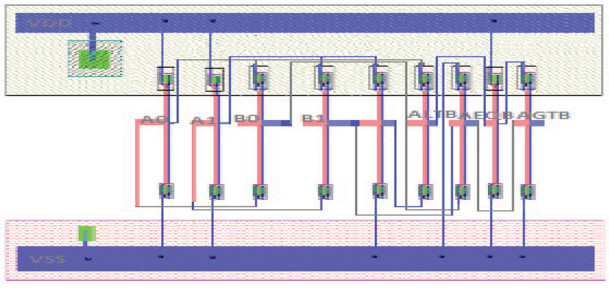

Figure 11: Layout of the multiplexer-based 2-bit digital comparator.

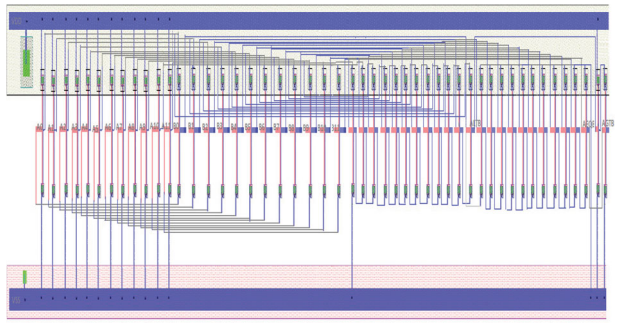

Figure 12: Layout of the multiplexer-based 12-bit digital comparator.

multiplexer-based 2-bit comparator, 12-bit comparator and novel technique-based 12-bit comparator are shown in Figures 1112–13, respectively.

The layout of the novel technique-based high-speed and low-power comparator is realized using the L-edit in EDA Tanner tool for performing the post-layout simulation. The effectiveness of the proposed comparator is analysed for both pre-layout and post-layout stages, for a power supply of 0.7 V. The power dissipation and the propagation delay of the novel technique-based 12-bit comparator in the post-layout simulation

Table 1: Performance comparison of a digital comparator.

Parameters	Conventional 2-bit comparator	Transmission Gate logic[12] based 2-bit comparator	Transmission Gate logic [1] based 2-bit comparator	Multiplexer-based 2-bit comparator	Multiplexer-based 12-bit comparator	Novel technique-based 12-bit comparator
Power consumption (μW)	0.53	0.41	0.23	0.09	0.54	0.56
Number of transistor	54	74	30	18	98	106
Propagation delay (n-sec)	6.97	7.13	5.32	4.52	7.38	5.15
Power delay Product (μ-nJ)	3.69	2.92	1.22	0.40	3.98	2.88

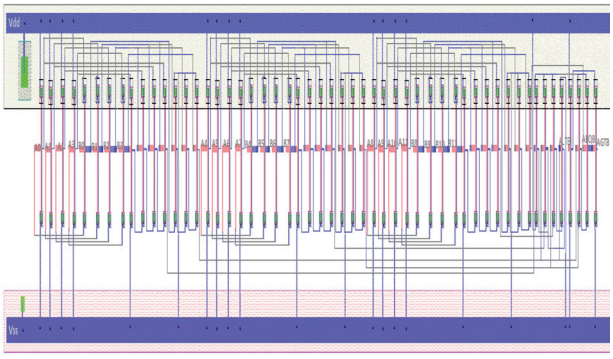

Figure 13: Layout of the novel technique-based 12-bit digital comparator.

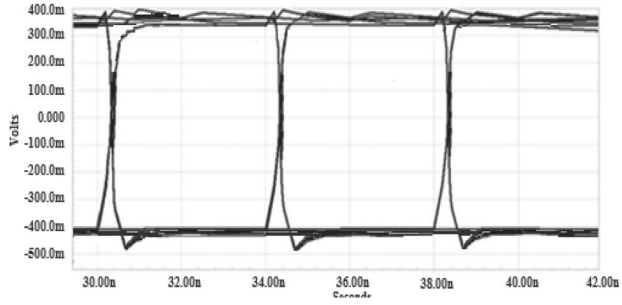

Figure 14: Eye diagram of the novel technique-based 12-bit digital comparator.

is 0.73 microwatt and 7.86 nanoseconds in the presence of the physical parasitic. The eye diagram of novel technique-based 12-bit comparator is shown in Figure 14. It has been found from the eye diagram that the output signal *A* is greater than signal *B* at a data rate of approximately 250 MBps. The simulation result is abridged in Table 1.

10. CONCLUSIONS

A novel technique has been applied by using the multiplexer to improve the speed of a comparator. Power consumption of the multiplexer-based 2-bit comparator is 0.09 μW which has been reduced to approximately 78% and delay has been reduced to approximately 37% from the existing transmission gate logic-based comparator [12]. It has been found that the transistor count is less in the proposed multiplexer-based 2-bit comparator circuit which is almost 75.67% less than existing transmission gate logic-based 2-bit digital comparator, subsequently that the overall area is minimized. A novel technique-based 12-bit digital comparator has been designed which consumes 0.56 microwatt power and the propagation delay is 5.15 nanosecond.

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