Class: Name: Number:

Computer Organization

Quiz(4.1~4.9) Date:2016/05/20

1. (4-1,2,3)(25%)Assuming the following latencies for logic blocks in the datapath:

I-Mem	Add	Mux	ALU	Regs	Mem	Sign-extend	Shift-left
400 ps	150 ps	50 ps	200 ps	200 ps	500 ps	80 ps	30 ps

(a) （5%）What is the clock cycle time if the only type of instruction we need to support are ALU instructions (**add**, **and**, etc.)?

Ans:

The longest-latency path for ALU operations is through I-Mem, Regs, Mux (to select ALU operand), ALU, Mux (to select value for register write) and Regs.

400+200+50+200+50+200 = 1100

(b) （5%）What is the clock cycle time if we only had to support **lw** instructions?

Ans:

The longest-latency path for lw is through I-Mem, Regs, Mux (to select ALU input), ALU, D-Dem, Mux (to select what is written to register) and Regs.

400+200+50+200+500+50+200 = 1600

(c) （10%）What is the clock cycle time if we must support **add**, **beq**, **lw** and **sw** instructions?

Ans:

lw clock cycle is the longest:1600

(d) （5%）If we can improve the latency of one of the given datapath components by 20%, which component should it be? What is the speed-up from this improvement?

Ans:

Mem:500->400

1600/1500

2. (4-2)(15%) When processor designers consider possible improvement to processor datapath, the decision usually depends on the cost/performance tradeoff.

	I-Mem	Add	Mux	ALU	Regs	D-Mem	Control
Latency	400ps	150ps	30ps	180ps	200ps	1000ps	100ps
Cost	1000	30	10	100	200	2000	500

Improvement	Latency	Cost	Benefit
Faster Add	-40ps for Add units	Cost +20 per Add unit	Replaces existing Add units with faster ones

Assume that we are starting with a datapath from Figure1.

(1) （5%）What is the clock cycle time with and without this improvement?

Ans: 400 + 200 + 30 + 180 + 1000 + 30 +200= 2040 ps

(2) （5%）What is the seed-up achieved by adding this improvement?

Ans: Speedup is 1. (No change in number of cycles, no change in clock cycle time.)

(3) （5%）Compare the cost/performance ratio with and without this improvement

Ans: Total cost = 1000+200+500+100+2000+2X30+3X10 = 3890

New cost = 3890+2X20 = 3930

Relative cost = 3930/3890 =1.01

Cost/performance = 1.01/1 = 1.01

3.(4-4) (20%)Refer to the following MIPS instructions :

(a) lw $3, 40($1)

(b) Label : bne $4, $2 Label

What is the value of these signals for instructions?

	RegDst	MemtoReg	RegWrite	MemRead	Branch
a.)					
b.)					

Ans:

	RegDst	MemtoReg	RegWrite	MemRead	Branch
a.)	0	1	1	1	0
b.)	X	X	0	0	1

4. (4-6)(20%)Assuming that following latencies for logic within each pipeline stage and for each register between two stages:

IF	ID	EX	MEM	WB	Pipeline register
100	120	90	130	60	10

Assuming there are no stalls, what is the speed-up achieved by pipelining a single-cycle datapath?

Ans:

The clock cycle time of a single-cycle is the sum of all latencies for the logic of all fi ve stages. The clock cycle time of a pipelined datapath is the maximum latency of the fi ve stage logic latencies, plus the latency of a pipeline register that keeps the results of each stage for the next stage. We have:

Single-cycle	Pipelined	Speed-up
500ps	140ps	3.57

5. (4-7)(20%)Find all data dependencies in the following instruction sequence.

I1: lw $1,40($2)
I2: add $2,$3,$3
I3: add $1,$1,$2
I4: sw $1,20($2)

Ans:

RAW:

($1) I1 to I3
($2) I2 to I3, I4
($1) I3 to I4

6. (10%)

Executing the following code on the pipelined datapath, what registers are being read and written at the end of the fifth cycle of the execution?

L1: add $2, $3, $1
L2: sub $4, $3, $5
L3: add $5, $3, $7
L4: add $7, $6, $1
L5: add $8, $2, $6

Ans:

At the end of the fifth cycle of execution, registers $6 and $1 (of S4) are being read and register $2 (of S1) will be written.

7. (4-5)(20%)Assuming that individual stages of the datapath have the following latencies:

IF	ID	EX	MEM	WB
200	300	250	400	150

(a) （5%）What is the clock cycle time in a pipelined and nonpipelined processor?

Ans:

Pipelined: 400

Nonpipelined: 200+300+250+400+150 = 1300

(b) （5%）What is the total latency of a lw instruction in a pipelined and nonpipelined processor?

Ans:

Pipelined: 400 * 5 = 2000

Nonpipelined: 1300

(c) （5%）Since the latency of lw in pipelined processor is more than in nonpipelined processor in (b), why we always use pipelined processor?

Ans:

多個指令可同時在不同 stage 執行

(d) （5%）If we can split two stage of the pipelined datapath into four stage(for each of these two was split into two stage), which stages would you split to get the lowest latency? What is the new clock cycle time of the processor?

Ans:

MEM&ID

MEM: 400/2 = 200, ID: 300/2 = 150

But EX is still 250.

The new clock cycle time is 250.

8.(4-5) (10%)Find the hazard in the following code:

```
lw    $t0,0($t1)
lw    $t2,4($t1)
sw    $t2,0($t1)
sw    $t0,4($t1)
```

Reorder the instructions to avoid pipeline hazard.

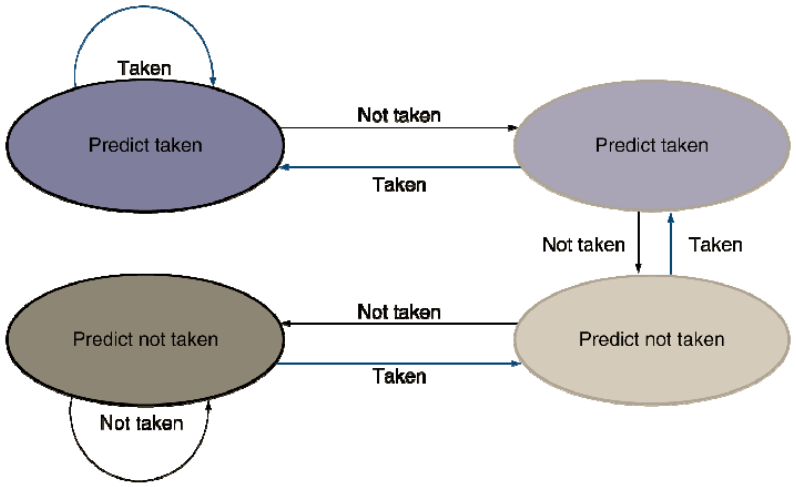
Ans:

對調這兩行 sw $t2,0($t1)

sw $t0,4($t1)

⇨ sw $t0,4($t1)
sw $t2,0($t1)

9.(4-8) (10%)



This question examines the accuracy of various branch predictors for the following repeating pattern (e.g. in a loop) of branch outcomes:

TNTNNTNT

(a) What is the accuracy of always-taken and always-not-taken predictors for this sequence of branch outcomes?

(b) What is the accuracy of the two-bit predictor for the first four branches in this pattern, assuming that the predictor starts off in the bottom left state from above figure (predict not taken)

(c) What is the accuracy of the two-bit predictor if this pattern is repeated forever.

Ans:

(a) always-taken: 4/8 = 1/2 = 50%

T	N	T	N	N	T	N	T
O	X	O	X	X	O	X	O

always-not-taken: 4/8 = 1/2 = 50%

T	N	T	N	N	T	N	T
X	O	X	O	O	X	O	X

(b) 2/4 = 1/2 = 50%

T	N	T	N
X	O	X	O

(c) 2/8 = 1/4 = 25%

T	N	T	N	N	T	N	T
X	X	X	X	O	X	O	X

10.(4-7) (5%) Refer to the following instruction sequences:

I1: add $1, $2, $3
I2: sw $2, 0($1)
I3: lw $1, 4($2)
I4: add $2, $2, $1
Find all data hazards in this instruction sequence for a five-stage pipeline and determine which can be **solved by forwarding** and which will **still cause a pipeline stall**.

Ans: data hazards are: ($1)I1 to I2
($1)I3 to I4
($1)I1 to I2 can be solved by forwarding and ($1)I3 to I4 will still cause a pipeline stall.

11.(4-9) (10%)

```
beg   $1, $0, Label
lw    $1, 0($1)
```

(5%)Assume that this branch is correctly predicted as taken, but then the instruction at "Label" is an undefined instruction. Describe what is done in each pipeline stage for each cycle, starting with the cycle in which the branch is fetched up to the cycle in which the first instruction of the exception handler is fetched.

題目口頭說明:畫出 pipeline diagram traditional form.

Ans:

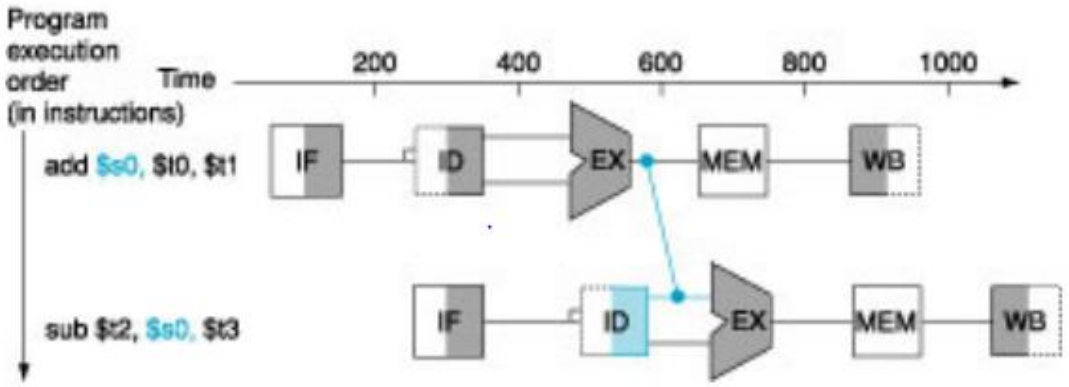
beq $1, $0, Label	IF ID EX MEM WB
lw $1, 0($1)	IF ID EX MEM
exception occurs	IF ID *EX
Something	IF *ID
Handler	IF

* = NOP

12.(5%) Using a drawing similar to the following figure, show the forwarding paths

needed to execute the following instructions in a pipeline architecture:

```
add  $3, $4, $16
sub  $5, $3, $2
lw   $7, 100($5)
add  $8, $7, $2
```



ANS:

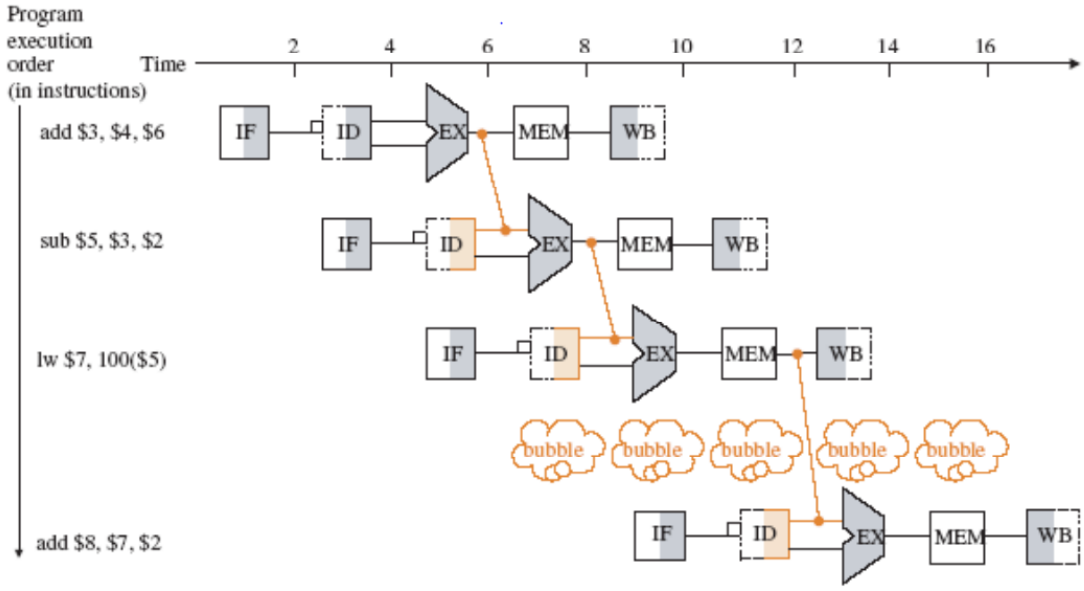
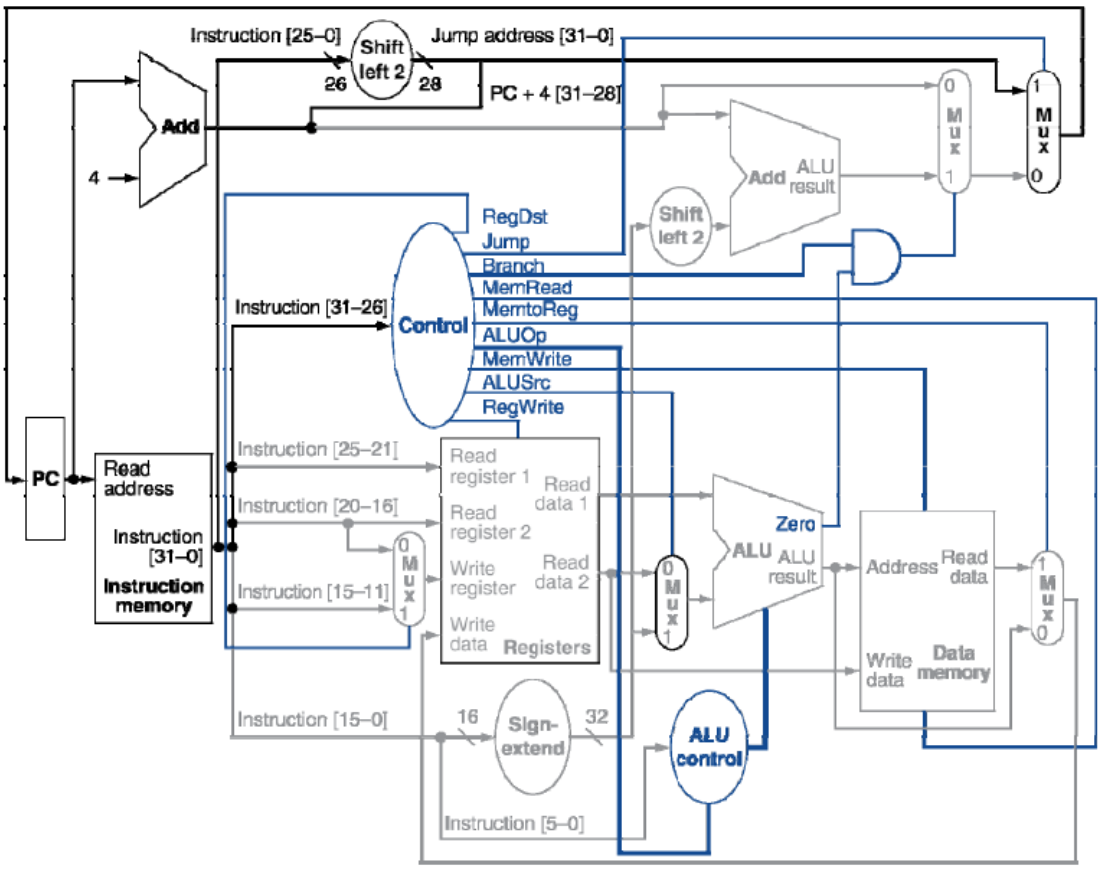


Fig1. Datapath with Jumps Added


Instruction [25–0]
Shift left 2
Jump address [31–0]
26
28
PC + 4 [31–28]
Add
4
M u x
0
1
Add
ALU result
Shift left 2
RegDst
Jump
Branch
MemRead
MemtoReg
ALUOp
MemWrite
ALUSrc
RegWrite
Instruction [31–26]
Control
PC
Read address
Instruction [31–0]
Instruction memory
Instruction [25–21]
Instruction [20–16]
Instruction [15–11]
Instruction [15–0]
Instruction [5–0]
Read register 1
Read register 2
Write register
Write data
Read data 1
Read data 2
Registers
Zero
ALU
ALU result
Address
Read data
Write data
Data memory
16
Sign-extend
32
ALU control