班級: 學號: 姓名:

Computer Organization

Final Exam

2008/06/10

(Total: 100%)

1. (20%) According to the single-cycle datapath in Figure 2, what are the values of a(1), a(2), …, d(5)in the following table of control signals?

Instruction	Reg-Dst	ALUSrc	Memto-Reg	Reg-Write	Mem-Read	Mem-Write	Branch	ALUOp1	ALUOp0
beq	a(1)	a(2)	a(3)	a(4)	0	0	a(5)	0	1
lw	b(1)	b(2)	b(3)	b(4)	1	0	b(5)	0	0
R-format	c(1)	c(2)	c(3)	c(4)	0	0	c(5)	1	0
sw	d(1)	d(2)	d(3)	d(4)	0	1	d(5)	0	0

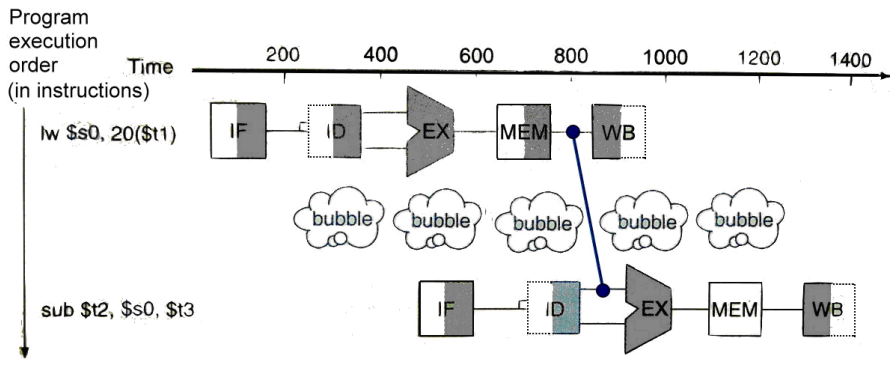
2. (10%) Execute the following **Copy** loop on a pipelined machine:

```
Copy :  lw      $10,    1000($20)
        sw      $10,    1000($20)
        addiu   $20,    $20,    -4
        bne     $20,    $0,     Copy
```

(a). Using a drawing similar to Figure 1, show the forwarding paths needed to execute the above **Copy** loop. You can use **forwarding** and **nop** instructions (stall) at the same time.

(b). Suppose that you are **not** allowed to use forwarding, please rewrite the code by inserting as few **nop** instructions (stall) as possible for proper execution.

Figure 1



3. (15%) Two important parameters control the performance of a processor: *cycle time* and *cycle per instruction*. There is an enduring trade-off between these two parameters in the design process of microprocessors. While some designers prefer to increase the processor frequency at the expense of large CPI, other designers follow a different school of thought in which reducing the CPI comes at the expense of lower processor frequency.
Consider the following machines, and compare their performance using the data below.

M1: The multicycle datapath of Chapter 5 with an **8.1GHz** clock

Instruction	Frequency
Loads	15%
Stores	15%
R-type	60%
Branch/jump	10%

M1

M2: A machine like the multicycle datapath of Chapter 5, except that register updates are done in the same clock cycle as a memory read or ALU operation. Thus in Figure 3, states 6 and 7 and states 3 and 4 are combined. This machine has a **7.2 GHz** clock, since the register update increases the length of the critical path.

Instruction	Frequency
Loads	30%
Stores	30%
R-type	25%
Branch/jump	15%

M2

M3: A machine like M2 except that effective address calculations are done in the same clock cycle as a memory access. Thus states 2, 3, and 4 can be combined, as can 2 and 5, as well as 6 and 7. This machine has a **6 GHz** clock because of the long cycle created by combining address calculation and memory access.

Instruction	Frequency
Loads	32%
Stores	28%
R-type	30%
Branch/jump	10%

M3

Find out which of the machines is fastest, Please write CPI and MIPS of M1, M2 and M3.

4. (10%) In the following C program fragment, which types of hazard might occur in a pipelined machine? Explain your answers. You must compile MIPS assembly code of the following C procedure. (Parameters a, b, x, y, z, w represent $a0, $a1, $s0, $s1, $s2, $s3 respectively)

```
If ( a = = b)
{     x = y + z;
      w = x – 1;}
r = w + x;
```

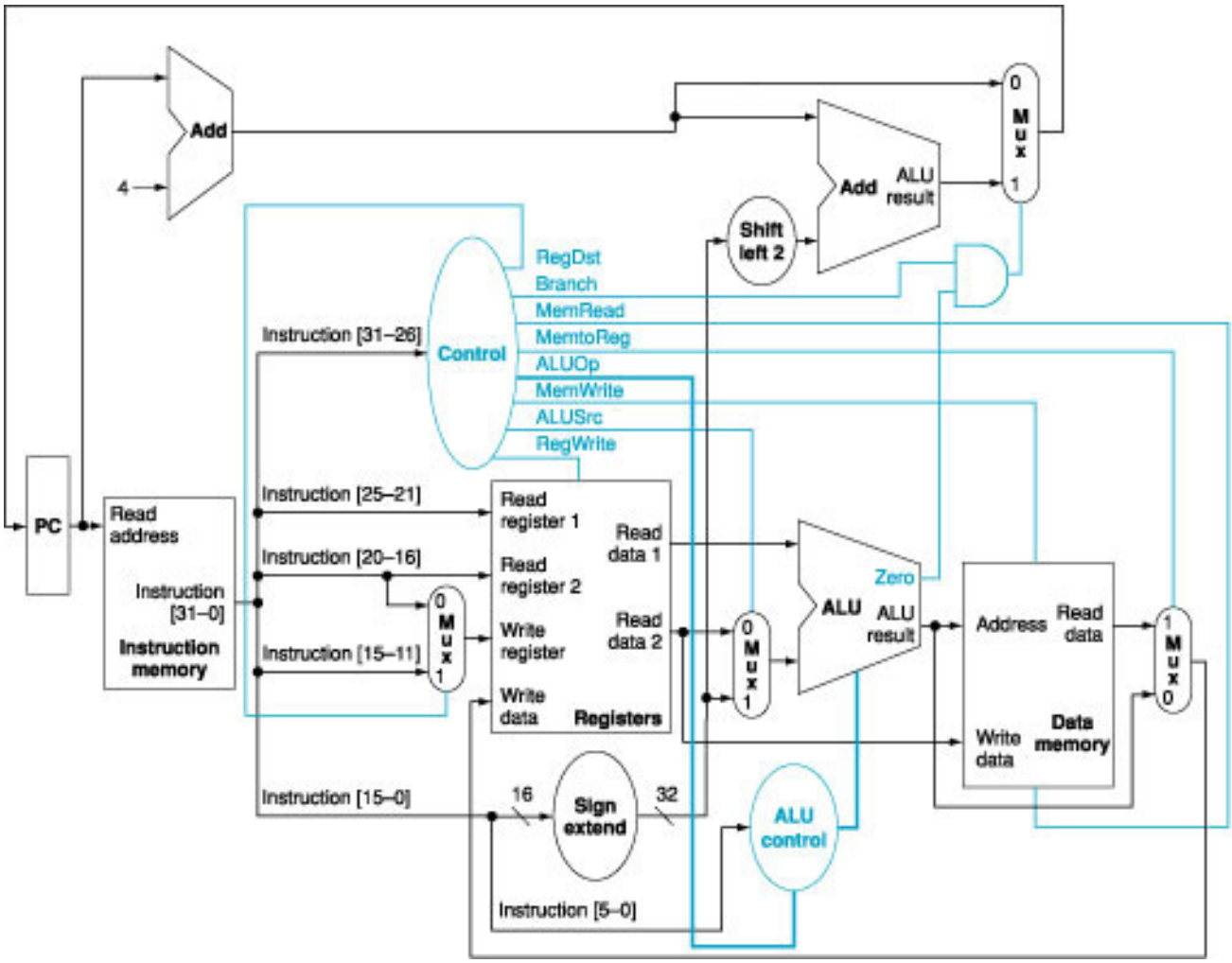
5. (10%) Consider a loop branch that branches nine times in a row, and then is not taken once. Assume that we are using a dynamic branch prediction scheme.
(a). What is the prediction accuracy for this branch if a simple 1-bit prediction scheme is used?
(b). What is the prediction accuracy for this branch if a 2-bit prediction scheme is used?
(c). Please draw the finite state machine for a 2-bit prediction scheme.

6. (15%) We wish to design a method to detect exceptions, including *undefined instructions* and *arithmetic overflow*, and to transfer control to the appropriate state in the exception states.
Add any necessary datapaths and control signals to the multicycle datapath of Figure 3, and any necessary states and control signals to the finite state machine of Figure 4. Note that the *exception address* = 8000 0180.

7. (20%) Note that some control signals are absent in the finite state machine of Figure 4. Please finish Figure 4 according to the multicycle datapath of Figure 3. In other words, please fill in the contents of **state 0**, **state 1**, **state 5**, **state 7**, **state 8**, and **state 9** in Figure 4.

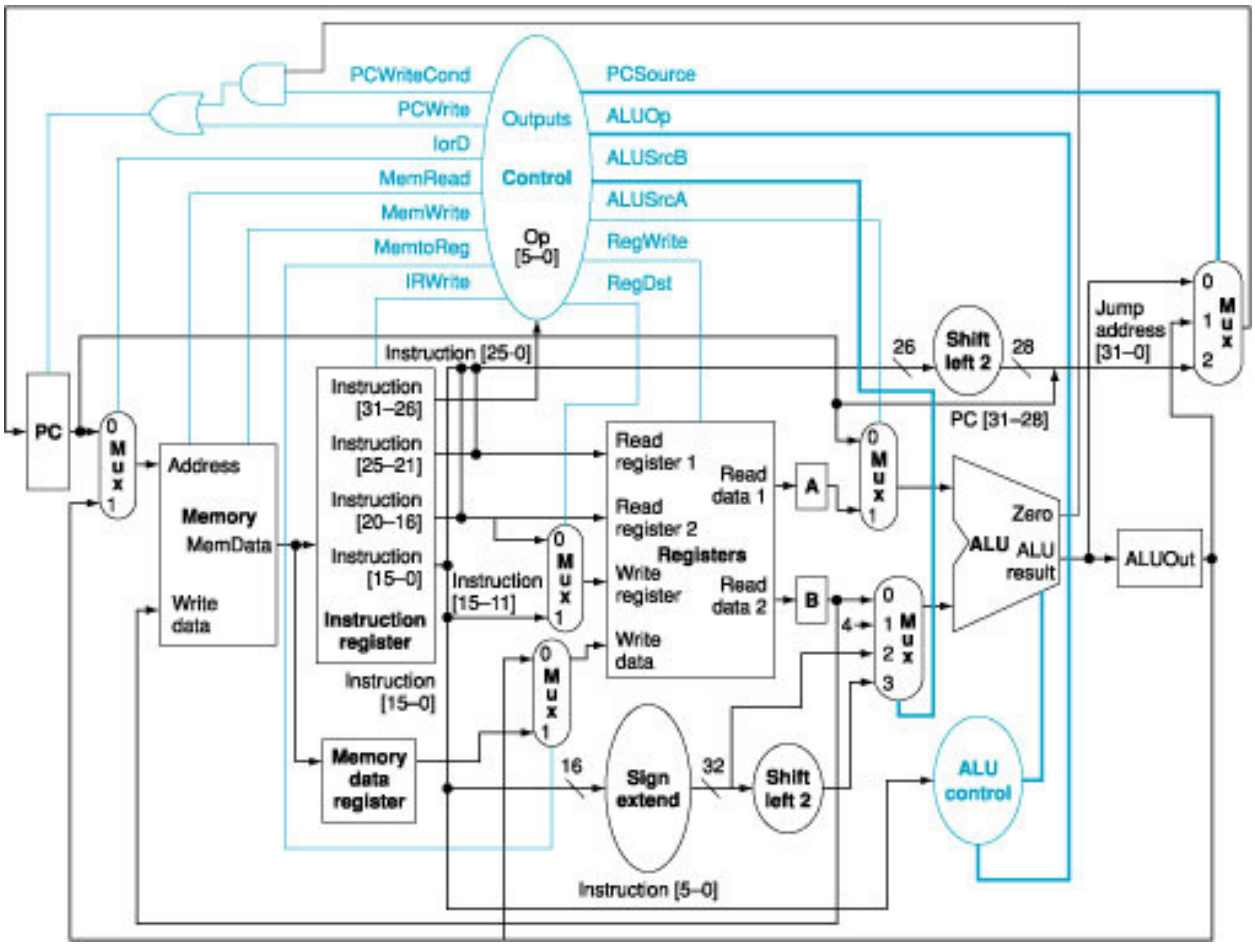
班級: 學號: 姓名:

Figure 2



班級: 學號: 姓名:

Figure 3



班級: 學號: 姓名:

Figure 4