ANEXO: REGISTRADORES

PORTA 1 (Similar para a Porta 2)

REG.	FUNÇÃO	VALOR do BIT			
P1DIR	Seleciona a direção de sinal (entrada/saída)	0	Entrada	1	Saída
P1OUT	Define o estado da(s) saída(s) digital(ais)	0	0 volt	1	Vdd
	2ª Função: quando o pino é uma entrada digital, define se o resistor será de pull-up ou pull-down	0	Pull-down	1	Pull-up
P1IN	Representa o estado da(s) entrada(s) digital(ais)	0	0 volt	1	Vdd
P1REN	Habilita resistor no pino configurado como entrada.	0	Desconectado	1	Conectado
P1IES	Seleciona borda de interrupção.	0	Subida	1	Descida
P1IE	Habilita geração de Requisição de Interrupção (IRQ)	0	Desabilitada	1	Habilitada
P1IFG*	Flag de Interrupção (indica evento de interrupção)	0	Não há evento	1	Há evento
P1SEL	Seleção de função digital alternativa do pino.	Ver tabela datasheet.			
P1SEL2	Seleção de função digital alternativa do pino.	Ver tabela datasheet.			

* As Flags de Interrupção devem ser limpas antes de habilitar a interrupção da(s) entrada(s).

BCS (Basic Clock System)

BCSCTL1, Basic Clock System Control Register 1

7	6	5	4	3	2	1	0
XT2OFF	XTS[1][2]	DIVAx		RSELx			
rw-(1)	rw-(0)	rw-(0)	rw-(0)	rw-0	rw-1	rw-1	rw-1

XT2OFF	XT2 off	0 XT2 is on	
XTS	LFXT1 mode select	0 Low-frequency mode	1 High-frequency mode
DIVAx	Divider for ACLK	00 /1 01 /2	10 /4 11 /8
RSELx	Range select		

BCSCTL2, Basic Clock System Control Register 2

7	6	5	4	3	2	1	0
SELMx		DIVMx		SELS	DIVSx		DCOR[1][2]
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

SELMx	Select MCLK source	00 DCOCLK 01 DCOCLK	10 XT2CLK when XT2 oscillator present on-chip. 11 LFXT1CLK or VLOCLK		
DIVMx	Divider for MCLK	00 /1 01 /2	10 /4 11 /8		
SELS	Select SMCLK source	0	DCOCLK	1	LFXT1CLK or VLOCLK when XT2 oscillator not present
DIVSx	Divider for SMCLK	00 /1 01 /2	10 /4 11 /8		
DCOR	DCO resistor select	0 Internal resistor		1 External resistor	

DCOCTL, DCO Control Register

7	6	5	4	3	2	1	0
DCOx			MODx				
rw-0	rw-1	rw-1	rw-0	rw-0	rw-0	rw-0	rw-0

DCOx	DCO frequency select.
MODx	Modulator selection.

BCSCTL3, Basic Clock System Control Register 3

7	6	5	4	3	2	1	0
XT2Sx		LFXT1Sx		XCAPx[1]		XT2OF[2]	LFXT1OF[1]
rw-0	rw-0	rw-0	rw-0	rw-0	rw-1	r0	r-(1)

XT2Sx	XT2 range select.	00 0.4- to 1-MHz crystal or resonator	01 1- to 3-MHz crystal or resonator
		10 3- to 16-MHz crystal or resonator	11 Digital external 0.4- to 16-MHz clock source
LFXT1Sx	Low-frequency clock select and LFXT1 range select.	00 32768-Hz crystal on LFXT1	01 Reserved
		10 VLOCLK	11 Digital external clock source
XCAPx	Oscillator capacitor selection.	00 ~1 pF	01 ~6 pF
		10 ~10 pF	11 ~12.5 pF
XT2OF	XT2 oscillator fault	0 No fault condition present	1 Fault condition present
LFXT1OF	LFXT1 oscillator fault	0 No fault condition present	1 Fault condition present

TIMER A

TAxCTL, Timer_A Control Register

15	14	13	12	11	10	9	8
Unused						TASSELx	
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)
7	6	5	4	3	2	1	0
IDx		MCx		Unused	TACLR	TAIE	TAIFG
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

TASSELx	Timer_A clock source select	00 TACLK	01 ACLK
		10 SMCLK	11 Não usar
MCx	Mode control	00 Stop mode	01 Up mode
		10 Cont. mode	11 Up/down
IDx	Input divider	00 /1	01 /2
		10 /4	11 /8
TACLR	Timer_A clear (Limpa bits IDx)	TAIFG	Timer_A interrupt flag
TAIE	Timer_A interrupt enable		

TAxCCTLx, Capture/Compare Control Register

15	14	13	12	11	10	9	8
CMx		CCISx		SCS	SCCI	Unused	CAP
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	r	r0	rw-(0)
7	6	5	4	3	2	1	0
OUTMODx			CCIE	CCI	OUT	COV	CCIFG
rw-(0)	rw-(0)	rw-(0)	rw-(0)	r	rw-(0)	rw-(0)	rw-(0)

CMx	Capture mode	00 Sem Captura	01 Cap. borda sub.
		10 Cap. borda desc.	11 Cap. bordas sub/desc
CCISx	Cap./Comp. input select	00 CCIxA	01 CCIxB
		10 GND	11 VCC
OUTMODx	Output Mode	000 OUT bit value	001 Set
		010 Toggle/reset	011 Set/reset
		100 Toggle	101 Reset
		110 Toggle/set	111 Reset/set
SCS	Synchronize capture source		
SCCI	Synchronized capture/compare input		
CAP	Capture mode: 0 Compare mode / 1 Capture mode		
CCIE	Capture/compare interrupt enable		
CCI	Capture/compare input		
OUT	Output: 0 Output low / 1 Output high		
COV	Capture overflow		
CCIFG	Capture/compare interrupt flag		

TAxCCR0 – Registrador de Captura/Comparação do Mod. 0.
TAxCCR1 – Registrador de Captura/Comparação do Mod. 1.
TAxCCR2 – Registrador de Captura/Comparação do Mod. 2.

TAxCCRx = (*tempo(F_{CLK}/F_{DIV})) – 1.**

PORTA 2

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]		
			P2DIR.x	P2SEL.6 P2SEL.7	P2SEL2.6 P2SEL2.7
XIN	6	XIN	0	1 1	0 0
P2.6		P2.x (I/O)	I: 0; O: 1	0 X	0 0
TA0.1		Timer0_A3.TA1	1	1 0	0 0
Pin Osc		Capacitive sensing	X	0 X	1 X
XOUT/	7	XOUT	1	1 1	0 0
P2.7/		P2.x (I/O)	I: 0; O: 1	0 X	0 0
Pin Osc		Capacitive sensing	X	0 X	1 X