8-bit Parallel-In/Serial-Out shift register

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I. Objectives

- Use Verilog to design and simulate an 8-bit Parallel-In/Serial-Out shift register using the IC 74HC165 specifications.
- Design a test bench for the circuit verification.

II. Introduction

III. Methodology

The 8-bit Parallel-In/Serial-Out shift register has been developed in two stages. In the first step the register has been designed based on the IC 74HC165 specifications available in the literature [**?**]. Using the truth table and the sequence diagram provided by the.

Listing 1: Codigo MATLAB para correlacionar señales de audio.

```
module PISO_REG_4B(
  input reg[7:0] D_in,
  input reg LOAD, SER,
  input reg clk, clken,
  output reg Q, QNEG
);

reg [7:0] D;

assign QNEG = ~Q;
assign Q = D[7];

always@(posedge clk or posedge clken)
begin
  if (~LOAD)
  begin
    D <= D_in;
  end
  else if (~clk | ~clken)
  begin
    D <= D << 1;
    D[0]<=SER;
  end

end

endmodule
```

IV. Conclusiones

In this document, an 8-bit Parallel-In/Serial-Out shift register was designed and tested. The register, based on the IC 74HC165 specifications, produced the same results under identical inputs during the test bench evaluation. The test bench results indicate, that the designed register can be used as a commercial Parallel-In/Serial-Out shift register.

[1] Texas Instruments, ”SNx4HC165 8-Bit Parallel-Load Shift Registers”. SN74HC165 datasheet, Dec. 1982[Revised Dec. 2015]