Danial Changez

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EDUCATION

Bachelor of Computer Engineering (Co-op) September 2022 – Present
University of Guelph, Guelph, ON

- **Relevant Courses: Computer Organization & Design, Embedded Reconfigurable Computing, Signal Processing, Data Structures, Large Scale Software Architecture**

TECHNICAL SKILLS

Languages: Verilog, VHDL, C\C++, PowerShell, Python, Shell, Java, JavaScript, SQL
Libraries: Selenium, WPF/XAML, Numpy, NLTK, Mocha, Chai, Unittest, Pynguin
Tools: Vivado, Vitis Unified, Linux, Docker, GitHub, Solidworks
Equipment: Multimeters, Oscilloscopes, Signal Generators, Soldering

WORK EXPERIENCE

Technical Support Analyst Intern Jan 2025 – Aug 2025
The Co-operators — Technical Platform Support, End-User Services

- **DONUT** — Created an app using **PowerShell** to parallelize driver updates with live device logs, increasing throughput by **3 times**, while being adopted by **30+** analysts.
- Standardized **CI/CD** to reduce release delivery time from **1 hour** to under **10 minutes**, while encrypting token storage into binaries using Windows DPAPI.
- **Dell BIOS Search** — Automated model-specific BIOS discovery and deployment for our fleet by using **Selenium** in a **PowerShell** script, eliminating Dell's **60-day** lag period.
- **Auto-PowerCycle** — **PowerShell** script tied to Kernel-Power and Dell TechHub logs in Event Viewer, used to reduce recurring black screen incidents at Calgary HQ by **70%**.
- Authored user and maintainer documentation (architecture, setup) for all scripts, while mentoring 5 co-ops to reduce onboarding time by **50%**.

PROJECTS

Tetris (RTL) | *Python, Verilog, Digital Design* Oct 2025 - Nov 2025

- Implemented a Tetris clone on the Nexys A7-100T FPGA in **Verilog**.
- Integrated a **VGA** timing module to output 640x480 pixels at 60Hz.
- Generated title ROMs and menu UI overlays while reducing the base **100 MHz** clock to **50 MHz** using an MMCM to ease timing constraints.

Matrix Multiplier AXI4 IP | *VHDL, C, Embedded Systems* Nov 2025

- Developed an **AXI4-Lite IP** in **VHDL** with a driver in **C** to communicate to the ARM processor through memory-mapped registers.
- Measured the latency of the embedded system at **52 ns**, averaged over **1000 runs** to reduce jitter from the software call overhead.
- Built a pure **VHDL** variant with ROM inputs, closing timing at **4.13 ns**, allowing a theoretical clock speed increase to **242 MHz** with an MMCM.

Schedule Exporter | *Python, JavaScript, Selenium* Nov 2024 - Sept 2024

- Built a cross-platform desktop app (**Python** with **Selenium**) and Chrome extension (**JavaScript**) for UofG students to export class schedules.
- Automated ICS and Google Calendar integration, reducing manual schedule build time by **90 – 120 minutes** per student.
- Processes a full term of **15 to 25 courses, labs, and seminars** to generate Google Calendar API imports in under **10 seconds**.