Assignment 2 CS 3339 – Fall 2017 Name Daniel Ortiz

Due: Friday, 9/22/17 @ 11:55pm netID deo15

(email not long Axxxxxx number)

40 points (no late grace period)

All submissions must be written in very neat handwriting and scanned (or typed) and submitted in PDF format to TRACS with the filename of A2_netID.pdf. You may submit as many times as you like prior to the deadline; only the most recent submittal will be graded. All assignments must be submitted individually and reflect your own work; however, I encourage you to work in groups and discuss the problems with your classmates.

1) [4 points] Despite its flaws, the x86 ISA has shown incredible resiliency, largely due to binary backwards compatibility. Why is binary backwards compatibility so important? Given this, what allowed the increase in popularity of the ARM ISA in the last decade?

Binary Backwards compatibility is important because you can run old Software on new hardware.

Mobile phones and low power consumption allowed the increase in Popularity of the ARM ISA.

2) [4 points] If I shop at Fry's, Digikey, Mouser, etc for electronic parts I can buy the latest i7 Intel processor chip but I cannot buy the latest ARM cortex processor chip – why not?

ARM Licences the ISA and not the processors. So basically no one is making them for basic consumer use other than for their own products.

3) [4 points] Divide the unsigned value 0x8eb5_743c by 4 using a bit-shift. Express the result in hexadecimal. (Hint: Don't use a calculator; you won't have one on the exam).

00 10|00 11|10 10|11 01|01 _ 01|11 01|00 00|11 11XX

2 3 A D _ 5 D 0 F

4) [4 points] An array of 4-byte ints begins in memory at address 0x1000_8000 and this address is stored in $s0. Provide the MIPS assembly instruction to store the 3rd element of the array into $s1.

lw $S1, 8($S0)

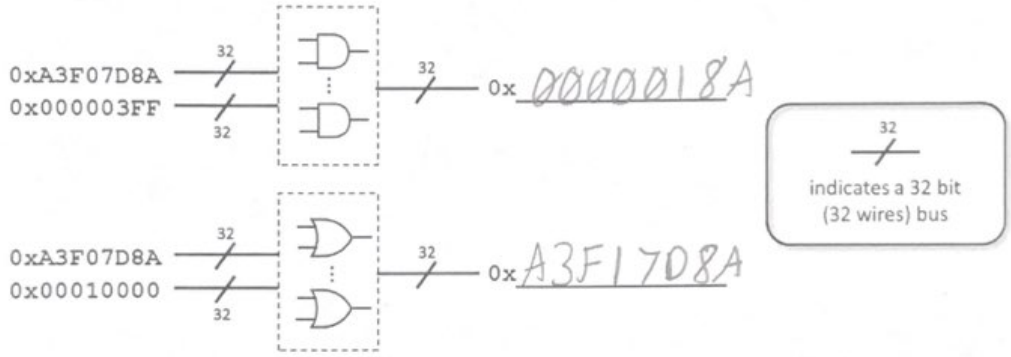
5) [4 points] Many x86 instructions require the destination register to also be one of the source registers. Why? (i.e., what is the benefit of requiring this?)

More room in bits for opcode/immediate/or addresses.

6) [4 points] If the MIPS designers wanted to increase the register set to 128 registers, what tradeoffs would be necessary for I-type instructions?

Smaller range for immediate, from 5 bits to 7 bits per register.

7) [4 points] The dashed boxes represent logic blocks that perform bitwise operations on 32 bit values per the symbol shown. Given the two 32 bit inputs what will be the output in hexadecimal format?



8) [4 points] Given the following truth table and circuit diagram complete the truth table with binary counting of the inputs and fill in the output values.

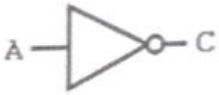
AND

Inputs		Output
A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

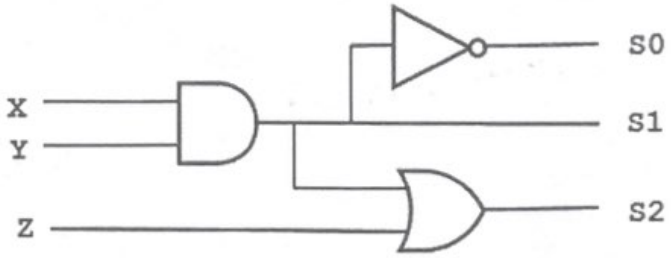
OR

Inputs		Output
A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

NOT



Input	Output
A	C
0	1
1	0



X	Y	Z	S0	S1	S2
0	0	0	1	0	0
0	0	1	1	0	1
0	1	0	1	0	0
0	1	1	1	0	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	0	1	1
1	1	1	0	1	1

9) [8 points] A MIPS binary has the following address and instruction data values. Write the assembly code for this instruction. Show your steps and put the answer in the same format as Project 1.

addr = 0x0040_0054 instr = 0x1360_0004

rs rt

=0001 0011 0110 0000 _ 0000 0000 0000 0100

4 27

addr = 0000 0000 0100 0000 _ 0000 0000 0101 0100

PC+4+CurrAddr

0000 0000 0000 0000 0000 0000 0001 0100

0000 0000 0100 0000 0000 0000 0110 1000

beq $k1, $zero, 0x00400068