Assignment 3 CS 3339 – Fall 2017 Name _____

Due: Wed, 10/11/17 @ 11:55pm netID _____

(email not long Axxxxx number)

40 points (no late grace period)

All submissions must be written in very neat handwriting and scanned (or typed) and submitted in PDF format to TRACS with the filename of A3_netID.pdf. You may submit as many times as you like prior to the deadline; only the most recent submittal will be graded. All assignments must be submitted individually and reflect your own work; however, I encourage you to work in groups and discuss the problems with your classmates.

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1) [2 points] A single cycle processor implementation can complete an entire instruction in 2.0nS. This processor is redesigned to implement pipelining with the same operation performed in 5 equal time length pipeline stages. What is the maximum operating frequency of the pipelined version in GHz?

2) [2 points] The *Intel® Math Kernel Library Developer Reference* Rev 15 Release 2018 contains the following cautionary statement: "Because the precision of floating point arithmetic is limited, it is not truly associative: (a + b) + c might not be the same as a + (b + c)." Describe why this happens and give an example of values for a, b, c where the output would differ.

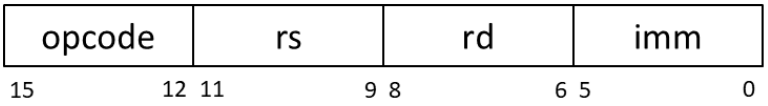
3) [4 points] Express the value -0.875 decimal in IEEE 754 single precision binary format and convert to hexadecimal.

4) [4 points] If a processor has implemented all forwarding paths but no hazard detection, under what cases could the processor produce erroneous results? Give a short sequence of instructions that would not give correct output if this were the case.

5) [3 points] Complete the following table with the steps necessary to multiply the 4-bit representation of 10 decimal by the 4-bit representation of 5 decimal and express the result in an 8-bit binary format.

10 X 5		= ?
Multiplier 4 bits ->	Multiplicand 8 bits <-	Product
_____	_____ _____	_____ _____
	+	_____ _____
_____	_____ _____	_____ _____
	+	_____ _____
_____	_____ _____	_____ _____
	+	_____ _____
_____	_____ _____	_____ _____
	+	_____ _____
		_____ _____

6) [5 points] A small 16-bit microcontroller has an R-type instruction with a 4-bit opcode, two 3-bit register fields, and a 6-bit immediate field.

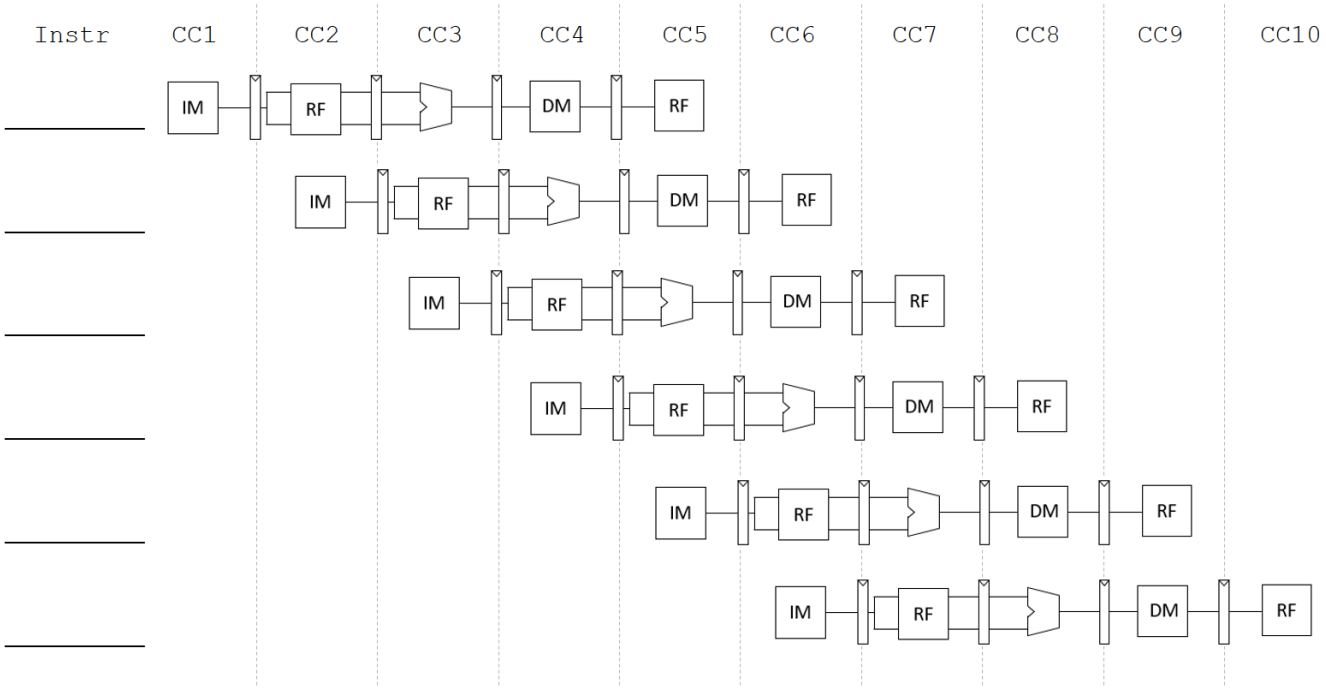


Complete the code below to properly parse the fields as in Projects 1 and 2:

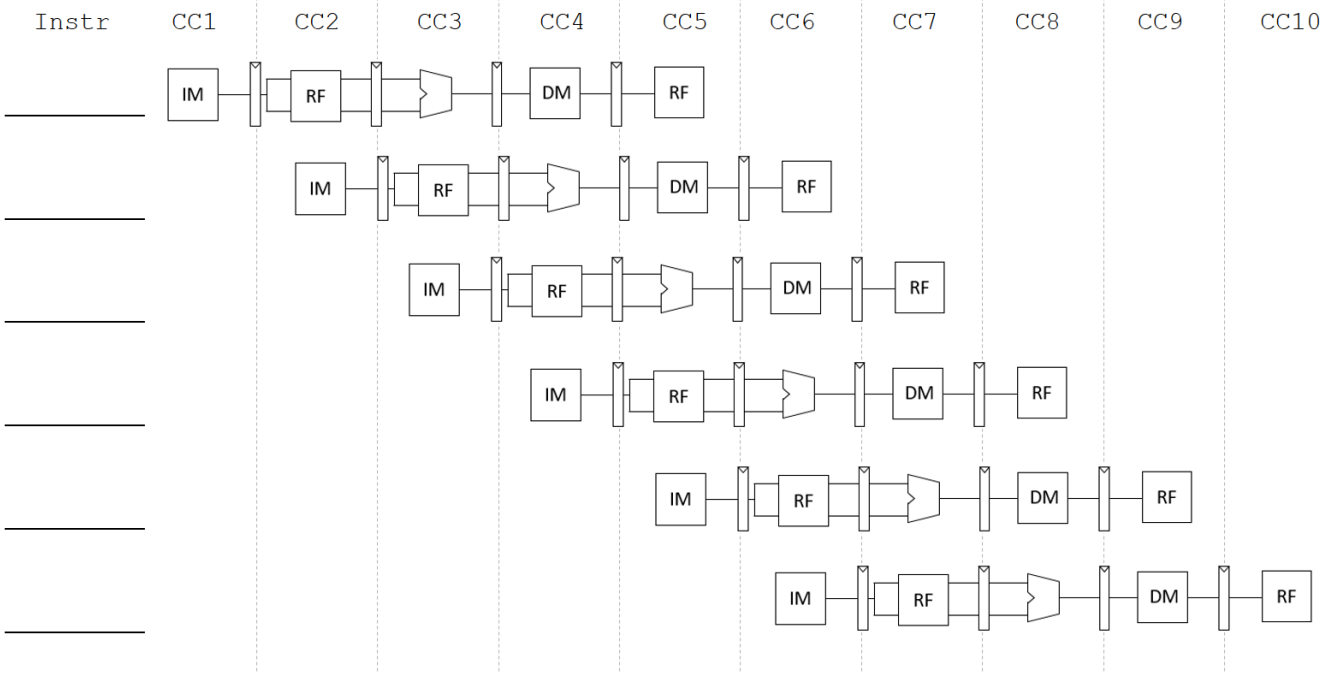
```
void disassembleInstr(uint16_t pc, uint16_t instr) {
  uint16_t opcode;      // opcode field
  uint16_t rs, rd;      // register specifiers
  uint16_t uimm;        // unsigned version of immediate (I-type)
  int16_t simm;         // signed version of immediate (I-type)

  opcode =

  rs =

  rd =

  uimm =

  simm =

// program continues from this point using values assigned.
```

7) [5 points] For the following instruction sequence show the bubbles required to ensure correct output without reordering and without forwarding paths. Draw arrows representing the flow of r3 and r4. [See figures 4.53 and 4.58]

```
and r3, r1, r2

lw r4, 10(r3)

sub r5, r4, r1
```



[5 points] Repeat the exercise, but this time use all possible forwarding paths to speed up execution.



8) [2 points] Correct the following emulation code for the MIPS *beq* instruction.

```
/* beq */ if (regFile[rs] = regFile[rd]) { pc = 4 + uimm;}
```

9) [6 points] List the 3 types of hazards pipelining introduces and for each one name the primary technique used to alleviate or eliminate it.

10) [2 points] Why is floating-point addition generally slower then integer addition?