7.9 1/2.74-inch 32Mpixel-Prototype CMOS Image Sensor with 0.64μm Unit Pixels Separated by Full-Depth Deep-Trench Isolation

JongEun Park, Sungbong Park, Kwansik Cho, Taehun Lee, Changkyu Lee, DongHyun Kim, Beomsuk Lee, SungIn Kim, Ho-Chul Ji, DongMo Im, Haeyong Park, Jinyoung Kim, JungHo Cha, Taehoon Kim, In-Sung Joe, Soojin Hong, Chongkwang Chang, Jingyun Kim, WooGwan Shim, Taehee Kim, Jamie Lee, Donghyuk Park, EuiYeol Kim, Howoo Park, Jaekyu Lee, Yitae Kim, JungChak Ahn, YoungKi Hong, ChungSam Jun, HyunChul Kim, Chang-Rok Moon, Ho-Kyu Kang

Samsung Electronics, Hwaseong, Korea

2021 IEEE International Solid- State Circuits Conference (ISSCC) | 978-1-7281-9549-0/20/$31.00 ©2021 IEEE | DOI: 10.1109/ISSCC42613.2021.9365751

For years, there has been a strong drive for sub-micron pixel development, in spite of reaching the visible light diffraction limit, because a smaller pixel pitch of CMOS image sensors (CISs) is inevitably required for ever-miniaturizing camera modules as mobile devices incorporate more cameras, few of which are dedicated to ultra-high-resolution zoomed images [1]. To that end, image sensor vendors have tried to find new ways to avoid reduction in sensitivity and more crosstalk in the sensor through pixel architecture change and/or fabrication process refinement [2-4]. For example, a 0.7μm pixel sensor was demonstrated with acceptable photodiode (PD) full-well capacity (FWC) of >6,000e- as well as signal-to-noise ratio (SNR) of ~32dB without optical/electrical crosstalk by employing state-of-the-art full-depth deep-trench isolations (FDTIs). [4] However, further scaling requires elaborate fabrication innovation and layout ideas. At the same time, meeting every aspect of pixel performance compared to the previous generation becomes even more difficult, e.g., with respect to dark or illuminated characteristics, fixed-pattern or temporal noises, etc. The latter, in particular, is associated with in-pixel source-follower (SF) amplifiers. Therefore, electrical performance of scaled in-pixel transistors cannot be overlooked. In this paper, a 32-megpixel (MP) CIS with 0.64μm unit pixels is demonstrated with FDTI design. Innovations in terms of fabrication and design to achieve this performance with scaling are discussed.

Cross-sectional schematics of the FDTI pixel structure are shown in Fig. 7.9.1 (a). To achieve the equivalent FWC, it is required to meet an effective PD area through the PD doping concentration and real PD area at the given scaling rate [3,4]. Even though the most advanced high-aspect-ratio contact (HARC) etching to our availability was used for this work, it was known that logic or memory processes based on similar design rule shrinks suffer from pattern leaning after the subsequent cleaning process. Therefore, to utilize the same cleaning facility as the previous generation, the aspect ratio of the DTI must remain the same as the previous generation. To overcome this restriction, the effective PD volume was enlarged by two ways: 1) increasing ion-implantation dose of n-type PD (NPD) doping by 30% and 2) lowering the shallow trench isolation (STI) depth by 20% as depicted in Fig. 7.9.1 (b). A key design consideration was not to create an abrupt p-n junction near the defective DTI interface. The reason is that high electric field aggravates both leakage current and white pixel defects, which are later discussed. NPD ion-implantation was carefully designed considering the following thermal steps so that p-n junction broadening can occur through isotropic surface-charge distribution at the deep PD junction. As a result, 6,000 e- of FWC in spite of 25% of PD volume reduction is achieved, which is comparable to that of the previous generation.

Another challenge with smaller pixels is node isolation. Figure 7.9.2 (a) illustrates a 4-transistor active pixel sensor (4-T APS) fabricated in this work. Any two nodes can be separated either by: 1) p-n junction barrier, or 2) STI, as seen in Fig. 7.9.2 (b). Node isolation between reset gates (RGs) and floating diffusions (FDs), in particular, is crucial in terms of pixel-to-pixel FWC non-uniformity. TCAD simulation was used to estimate the potential barrier height between the nodes. By using the same p-Si surface doping, the barrier for electrons at FDs is lowered from 0.37eV to 0.19eV. In other words, signal electrons can be lost by flowing to V_{DD} more easily as the pixel shrinks. The simulation also indicates that a 3-fold increase of p-Si doping is needed to ensure an equivalent barrier height to the previous generation, as shown in Fig. 7.9.2 (c).

However, such high blank ion-implantation may create electrical performance variation, not to mention additional fabrication cost. Therefore, STI was used instead for the RG-FD isolation in this work. However, this layout change increases STI interface area by 13%, which in turn might increase STI-induced leakage current. However, it was mitigated by STI depth reduction by 20%, and we were able to achieve an excellent leakage level without FWC non-uniformity.

The defective PD Si surface at the DTI interface caused by the DTI etching processes should be electrically passivated to suppress leakage generation. The suppression mechanism is electron-hole recombination by accumulated holes at the defective interface. It can be either in a passive way, i.e., using plasma doping (PLAD) around DTIs, which also serves as a p-type PD ground [5], or in an active way that can be done by applying a negative bias to DTIs (NDTI). Sufficient p-type doping concentration in the DTI polysilicon is critical to eliminate a spatial dark current gradient across the sensor, which can be induced by high sheet resistance of DTIs causing a voltage drop or RC delay. Initially, polysilicon gap-fill with an *in situ* deposition-etching-deposition process, followed by p-type doping with BF_3, was used. [2,4] In this work, fixed-pattern white pixel counts drastically increased over the previous generation. Usually, Fluorine (F) ion-implantation is used to cure the defective Si interface [6]. In our case, however, BF_3 concentration should be high enough to lower the DTI resistance and it may deteriorate the sidewall oxide quality as F-assisted boron concentration increases. Though in-depth analysis of such a phenomenon is under way, F-free boron-doping into DTI polysilicon was used. Figure 7.9.3 shows the fixed-pattern histograms in dark condition. Overall pixel counts with higher digital-number (DN) output are dramatically reduced. The reduction helped to improve not only the white pixel defects (in-pixel distribution), but also dark leakage current (average). Consequently, we were able to achieve acceptable white pixel defects below 20ppm and leakage current of 1.1e-/s, which is lower than the previous generation.

As pixel pitch shrinks, in-pixel transistors should be scaled as well. In particular, the size of SF is a key contributor to pixel linearity, and temporal pixel noises such as random telegraph signal (RTS). In this work, SF area was reduced by 38% from the previous generation due to the layout design rule constraints. As a result, there was an almost 6× increase of RTS noise from 3 to 18ppm. It is known that RTS current fluctuation is inversely proportional to SF area and gate oxide capacitance, i.e., $1/(W{\cdot}L{\cdot}C_{ox})$ [7]. Two experiments were carried out: 1) reduction of SF gate oxide (GOX) thickness, and 2) 20% reduction of spacer width. Figure 7.9.4 shows improvement of RTS counts with thinner GOX and narrower spacer, which corresponds to 17% reduction of effective SF area. Each step accounts for ~50% of RTS improvement. A caveat with using thinner GOX was reliability failures such as time-dependent dielectric breakdown (TDDB) accompanied with hot carrier injection (HCI). However, the pixel silicon with the reduced GOX was certified by our reliability team passing all the CIS reliability criteria, and it also meets the typical pixel RTS specification, i.e., below 10ppm. Figure 7.9.5 summarizes the measured pixel performances. Figures 7.9.6 and 7.9.7 show sample images taken with the 0.64μm pixels in comparison with the previous 0.7μm pixels, and a chip micrograph, respectively.

In summary, we demonstrate a 1/2.74-inch 32Mpixel prototype high-resolution CMOS image sensor with 0.64μm pixels fabricated by an advanced full-depth DTI process. Further scaling of submicron pixels by ~10% in pixel pitch and ~25% in PD volume poses many challenges in terms of fabrication, layout, and performance. To achieve comparable performance in terms of FWC, dark leakage current, white pixel defects, RTS, etc., we introduce higher NPD doping, shallower STI depth, new DTI p-doping species, STI-separated nodes, and SF transistor re-design. As a result, equivalent or even better pixel performance is obtained without any harsh process burdens or reliability failures. This work sheds many insights on pixel design and fabrication processes as submicron pixel scale continues.

References:

[1] S. Takahashi et al. "A 45 nm Stacked CMOS Image Sensor Process Technology for Submicron Pixel," *Sensors*, vol. 17, no. 2816, 2017.

[2] J. C. Ahn et al., "A 1/4-inch 8Mpixel CMOS Image Sensor with 3D Backside-Illuminated 1.12μm Pixel with Front-Side Deep-Trench Isolation and Vertical Transfer Gate," *ISSCC,* pp. 124-125, Feb. 2014.

[3] Y. Kim et al., "A 1/2.8-inch 24Mpixel CMOS Image Sensor with 0.9μm Unit Pixels Separated by Full-Depth Deep-Trench Isolation," *ISSCC,* pp. 84-85, Feb. 2018.

[4] H. Kim et al., "A 1/2.65in 44Mpixel CMOS Image Sensor with 0.7μm Pixels Fabricated in Advanced Full-Depth Deep-Trench Isolation Technology," *ISSCC,* pp. 18-19, Feb. 2018.

[5] C. R. Moon et al., "Application of Plasma-Doping (PLAD) Technique to Reduce Dark Current of CMOS Image Sensors," *IEEE Electron Device Letters*, pp. 114-116, Feb. 2007.

[6] P. Chowdhury et al., "Improvement of Ultrathin Gate Oxide and Oxynitride Integrity Using Fluorine Implantation Technique," *Appl. Phys. Lett*, vol. 70, p. 37, 1997.

[7] E. Simoen et al., "Explaining the Amplitude of RTS Noise in Submicrometer MOSFETs," *IEEE Trans. Electron. Devices*, vol. 39, p. 422, 1992.

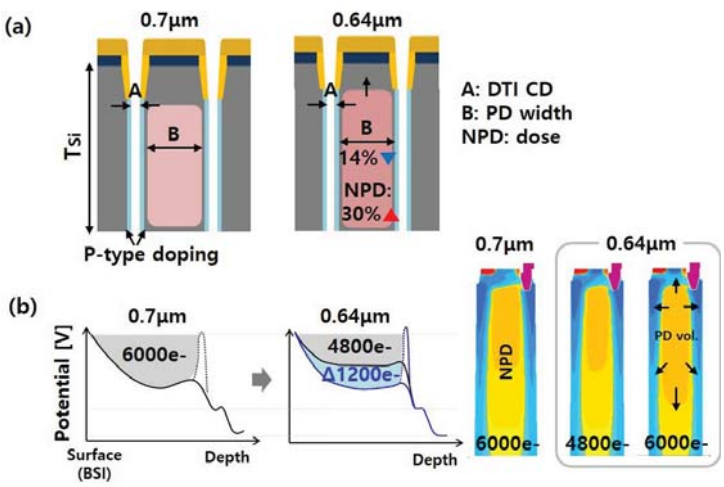

Figure 7.9.1: (a) Schematic diagrams of the full-depth DTI structures. (b) Potential curves of photodiode (PD) and TCAD-simulated doping profile of n-type PD doping.

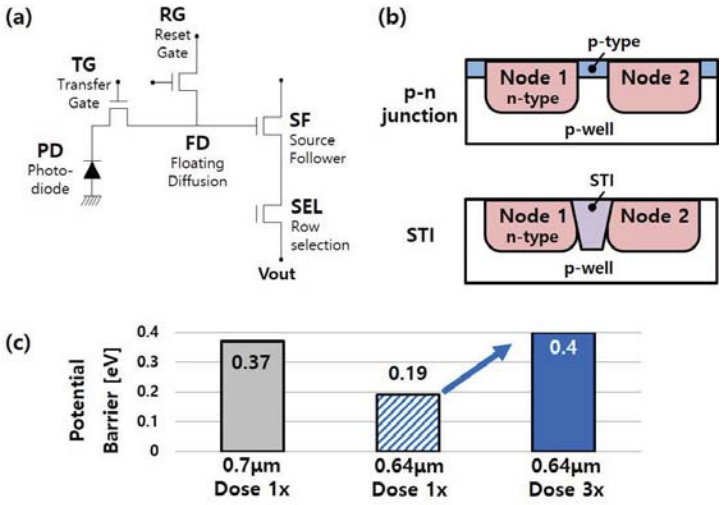

Figure 7.9.2: (a) Schematic of 4-T APS. (b) Cross-sectional view of node-isolation, p-n junction and STI isolation.

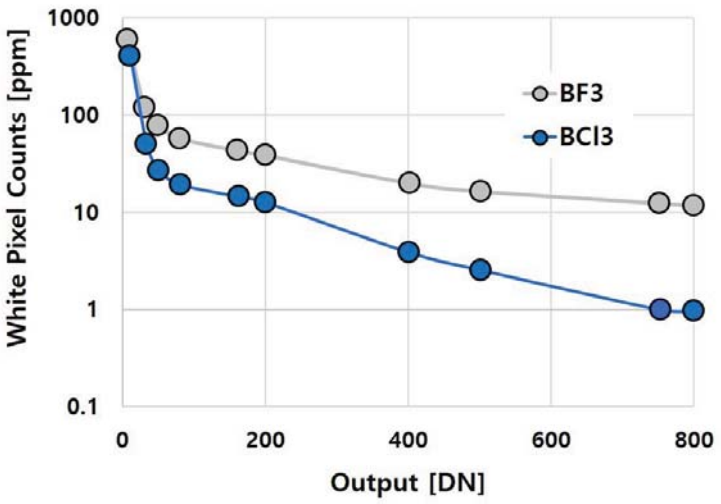

Figure 7.9.3: Fixed-pattern histogram in dark condition.

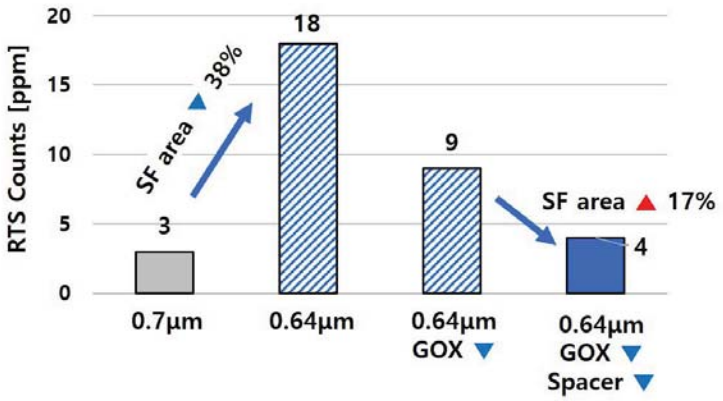

Figure 7.9.4: Random telegraph signal (RTS) noise in ppm.

Items	unit	0.7um	0.64um
Linear FWC	e-	6,000	6,000
Dark current	e-/s	1.3	1.1
White spot[1)]	ppm	10	15
Random noise	e-	1.4	1.4
RTS[2)]	ppm	3	4
YSNR [20lux][3)]	dB	31.7	30.7

1) White spot: # of pixels ≥160LSB @1-frame, gain X16, EIT 125msec, Tj=60℃
2) RTS: # of pixels ≥30LSB @difference between 2-frame, X16, EIT 0msec, Tj=60℃
3) YSNR [20lux]: 4-binning mode

Figure 7.9.5: Sensor performance comparison table.

Figure 7.9.6: Sample images.

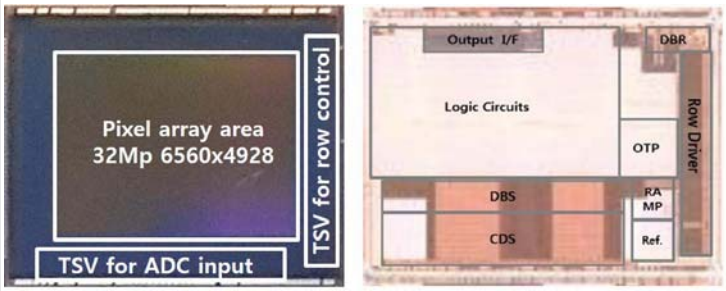

Figure 7.9.7: Chip micrograph.

978-1-7281-9549-0/21/$31.00 ©2021 IEEE