A 1/1.33-inch 108Mpixel CMOS Image Sensor with 0.8um unit NONACELL pixels

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***Abstract*— This paper presents a 1/1.33-inch 108Mp (mega-pixel) CMOS image sensor (CIS) for mobile applications. It is a 3D-stacked CIS designed with 0.8um unit pixels having dual conversion gain (DCG). This work in which the NONACELL technology is applied proves large-pixel effect which provides improved performance in low lux condition at submicron pixels. The number of photodiodes increases due to the NONACELL technology, the full well capacity (FWC) can be increased due to the proposed DCG technology as well. In addition, in the proposed high dynamic range (HDR) structure, image can be displayed with a frame rate that is 3 times higher than traditional 3D-HDR.**

Keywords—CIS, HDR, DCG, Nonacell

I. INTRODUCTION

CMOS image sensors have attracted much attention for the emerging mobile market, and the demand of high-resolution image sensors in mobile applications continues to increase [1-2]. Higher resolution needs reduction in pixel size to limit camera module size and consequently mobile phone thickness. In order to increase pixel resolution, the pixel size is reduced so that maximum FWC is limited. In order to further increase the effective FWC and signal-noise ratio pixel summation and dual conversion gain pixel [2-3] has been used. However, in the traditional DCG structure, the floating diffusion(FD) capacitance is limited to expansion, so only 2 summing can be supported. In this paper, proposes new DCG method that can be extended to 3 summing by sharing the FD node of adjacent rows. In addition, a wide dynamic range is used to selectively read pixels having the same integration time at the same time so that high frame rate can be used. In this work, a 0.8um 108 Mp CMOS image sensor is demonstrated for the first time, including four technologies: nonacell technology, advanced DCG, adaptive low power scheme and nona HDR. The chip consumes 600mW of total power at a frame rate of 90fps in nona mode achieving an FoM of 0.12e-nJ/DRU

II. NONACELL TECHNOLOTY

Combined pixels technique is used as Tetra or Nona, which attain high FWC by summing a couple of small size pixels, and HDR techniques. As depicted in Fig. 1, the tetra technology was used in product smaller than 1.0um pixel to secure the big pixel characteristics. To make more high resolution and high quality image, Nona pixel is applied to pixels of 0.8um or less as the next generation of tetra pixel [4]. Nonacell is an image sensor technology that enables nine adjacent pixels to operate like a single large pixel. By utilizing nonacell technology, small pixels of 0.8um size can be used as large pixels of 2.4um in a dark environment to photograph high sensitivity. Compared to tetracell that utilize four pixels, it can be more than twice as bright in the same light.

Compared to the Tetra in the view of pixel structure, the color filter pattern was changed from 2x2 to 3x3 and the pixel shared type was changed from 2x2 to 1x3. Like the tetra sensor, the remosaic conversion in the high illuminance and the nonacell technology in low illuminance can be used to improve the SNR.

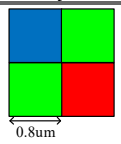
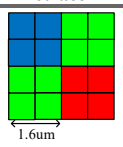
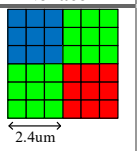
	Bayer	Tetracell	Nonacell
Structure			
Color filter pattern	1x1 CF	2x2 CF	3x3 CF
Pixel shared	2x2	2x2	1x3
SNR gain	SNR_{pix}	+ 6dB	+ 9.5dB
Max FWC @ Summing	FWC_{pix} e-	4x FWC_{pix} e-	9x FWC_{pix} e-

Fig. 1. Bayer, Tetracell and Nonacell technology

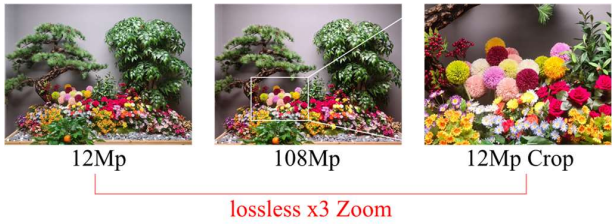


Fig. 2. Supporting lossless x3 Zoom

In general, the SNR improvement is improved by summing number M can be generally expressed as

$$SNR_{pix} = 20log_{10}\frac{Q}{\sqrt{Q+Dt+N}} \quad (1)$$

$$SNR_{sum} = 20log_{10}\frac{MQ}{\sqrt{MQ+MDt+N}} \approx SNR_{pix} + 10log_{10}M \quad (2)$$

where Q is the electron signal, t is the exposure time, D is the dark current constant and N is the read noise power. Thus, for full mode using one pixel, a nonacell that sums nine pixels gets 9.5dB of SNR gain, and a tetracell that sums four pixels gets 6dB of SNR gain.

108Mp resolution is best suited to create 12Mp resolution suitable for preview mode and capture with 9 sum effect when using nonacell. Using 108Mp Resolution, it crops 12Mp from 108Mp based on Preview 12Mp to support 12M capture image with x3 times zoom effect as shown in Fig. 2.

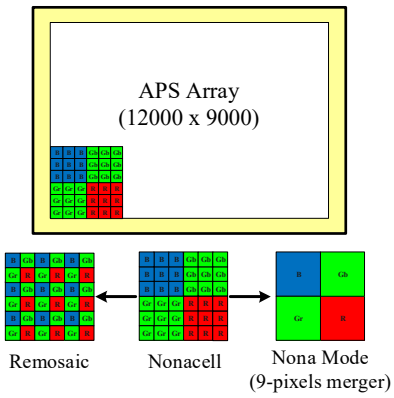


Fig. 3. Nonacell diagram which is transformed to the full mode and the Nona mode respectively

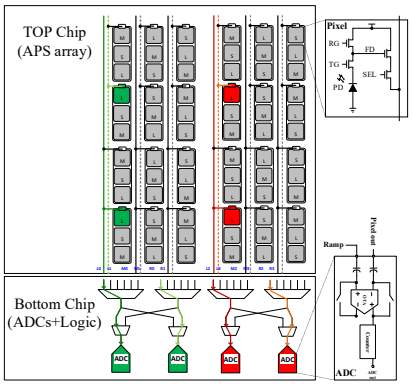


Fig. 4. Readout scheme for full resolution readout mode

III. IMAGE SENSOR ARCHITECTURE

The block diagram of the proposed sensor is as shown in Fig. 3. The top chip containing active pixel sensor (APS) array is fabricated in 65nm technology node and the readout circuitry, which is placed on the bottom chip, is in 28nm process. APS array is made up of 3x3 pixel clusters called nonacell. Each cluster consists of 1x3 arrays that share the FD node. In nona mode, 3 summing is performed vertically and then 3 averaging is performed horizontally to convert nine pixels into one pixel. Through this operation, the frame rate in the nona mode is 9 times higher than the full mode.

The new readout method was implemented according to the 1x3 shared APS structure. It is configured to share 2 column ADCs per 3 columns, reducing size and power in full mode, and allowing 2 row readout simultaneous readout (2RSR) operation in nona mode, enabling high frame rate.

Due to the 1x3 shared structure, the distance between different color pixel's Vout line (Vout_2) and the FD (FD_2) metal is close. When reading full resolution, nth column and n+3th column pixels were read at the same time as shown in Fig. 4 to minimize coupling effect by adjacent lines. In nona mode, which reads both pixels at the same time, it was necessary to review the level of different color coupling. And we optimized layout as much as possible through shielding with GND line and confirmed that the different color coupling was reduced from 3% to 0.8% in simulation result.

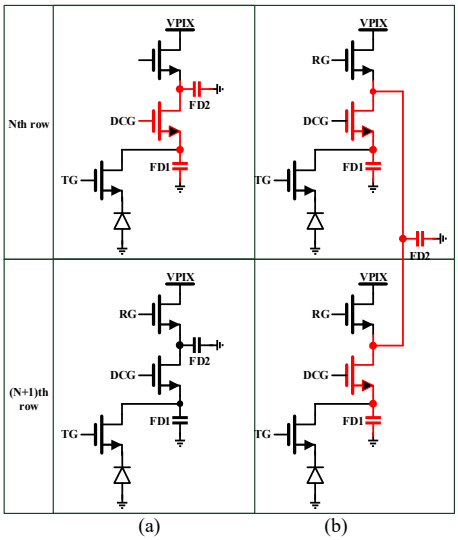


Fig. 5. Schematic of (a) Conventional DCG pixel and (b) Proposed DCG pixel

A. DUAL CONVERSION GAIN

The light that enters the pixel generates electrons in the photodiode, which is passed to the FD node and then converted to a voltage. At this time, the voltage generated by one electron is expressed as conversion gain (CG), and the unit is uV/e-. This CG is determined by the capacity of the FD node. It is inversely proportional to the size of the capacity as follows where e is the charge of the electron and C_{FD} is the capacity of the FD node.

$$C.G \propto \frac{e}{C_{FD}} \tag{3}$$

Therefore, when the capacity of the FD node is large, the CG becomes smaller, and on the contrary, when the capacity is small, the CG becomes larger. The large CG means that the signal voltage output is larger when the same amount of light enters and generates the same number of electrons. If the voltage signal is large, good SNR characteristics can be obtained, so it is better to make the capacity smaller to grow CG.

Although the nonacell technology can improve low light performance by increasing incident photons, it is difficult to realize a triple FWC due to the limitation of FD dynamic range and ADC saturation range. To overcome this, the adaptive DCG pixel that has two types of CG in the nona mode, high conversion gain (HCG) and low conversion gain (LCG). As shown in Fig. 5, additional FD capacitance can be obtained by adding DCG tr. between RG and VDD in the existing DCG structure. However, as the pixel size becomes smaller, there is a limit to the FD capacitance that can be additionally obtained. To overcome this, the FD2 and FD1 nodes of the adjacent row were used in DCG mode to secure 3 times the FD capacitance. By using this, the ratio of HCG to LCG ratio can be secured up to 1:3.

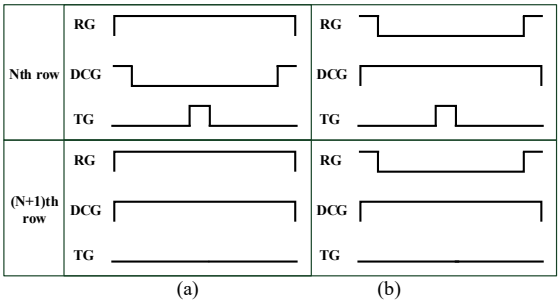


Fig. 6. DCG timing diagram of (a) HCG and (b) LCG

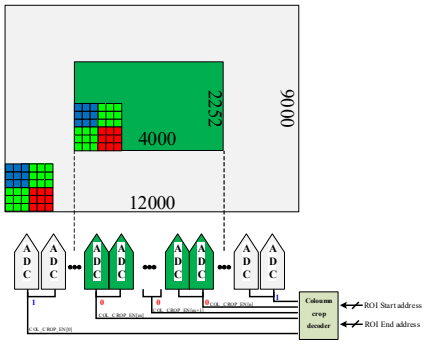


Fig. 7. Adaptive low power scheme

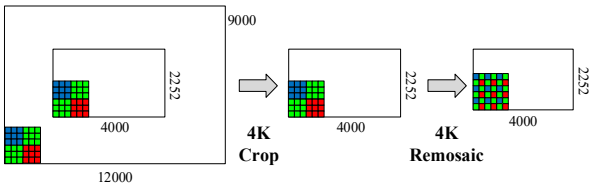


Fig. 8. ROI remosaic example

As shown in Fig. 6, when reading nth row in HCG mode, only DCG of nth row is tuned off, so FD1 node is used only. In LCG mode, on the other hand, both RG of nth and n+1th row are turned off, and both DCG of nth and n+1th row are turned on and used as FD is used with the sum of FD2, FD1nth and FD1n+1th.

Using this DCG technology that changes the FD capacitance according to the situation, it always has better performance by increasing CG in the dark scenes and reducing CG in the bright scenes.

In addition, if the selection transistor of neighboring pixels are operated together, the number of source follower can be used twice, and the noise improvement effect can be obtained in DCG mode. Especially in pixels below 0.7um, it is impossible to implement the DCG mode cap due to small size. Therefore, the neighboring FD cap sharing method must be applied.

B. ADAPTIVE LOW-POWER SCHEME

In the case of high-pixel products, it is often used in crop mode in actual products. In order to reduce power in crop mode, column ADCs can be turned on or off according to crop size. Transferring the image start and end positions in the timing generator block is a way to provide a COL_CROP_EN[N] signal to turn off the selected ADC in the column crop decoder. When crop mode is activated, the ADC can be selectively turned off to reduce the analog power.

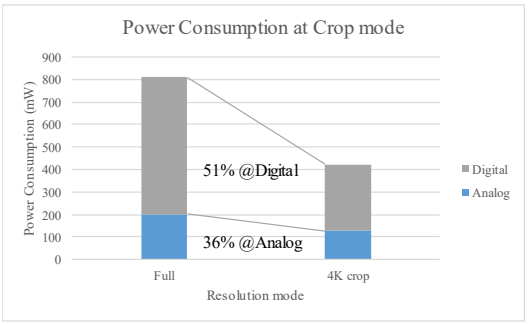


Fig. 9. ROI remosaic example

Adaptive low-power scheme is applied to the column-parallel ADCs especially for the smaller random region of interest (ROI) than full resolution. As shown in Fig. 7, the column crop decoder receive the ROI start address and the end address. The entered address is used to generate a COL_CROP_EN[N] signal for power down according to the preset table value. For example, if the start address of ROI is 4000d, all from COL_CROP_EN[0] to COL_CROP_EN[3] becomes high, and the ADCs connected to the signals becomes power down. Another example, if the end address is 8000d, all from COL_CROP_EN[10] to COL_CROP_EN[13] become high and the ADCs connected to the signals turn off the power. In this way, no matter what area of ROI comes in, only the ADC that is actually needed can operate to reduce the analog power. Fig. 9 shows the power dissipation of the 4K 30fps movie mode. The analog power is reduced by 36% when column ADCs outside of the ROI region are turned off.

There is a big problem in power consumption during remosaic operation to change the nona pattern to the bayer pattern. Corp mode is used when the Digital zoom function is activated, and efforts are required to reduce the power of the remosaic block. In order to reduce power in crop mode, ROI remosaic function that can be removable after a specific area crop was applied as shown in Fig.8. When operating with 4k crop, digital power is improved by about 51%. As shown in Fig. 9, the total power reduction was 48% combined with the analog power reduction plan.

C. NONA HDR MODE

To contain information about a wider range of luminance, HDR images require a mixture of pixels with different exposures. The long-exposure pixels hold better information in darker areas, but in lighter areas the exposure is exceeded and the signal is saturated. Conversely, short exposure pixels have better information in bright areas and use this information in areas saturated by long exposure. In each region of the image we decide to use information from short pixels, medium pixels, long pixels, or mix of both for transition areas.

For better HDR quality, CIS contains tetracell or nonacell up to 3 exposures. After HDR operation every quartet of pixels is merged into one pixel. In general, in tetracell structure, frame rate is dependent on full frame because all pixels must be read individually during 3D HDR. However, the proposed 3x3 nonacell has 3 FD nodes in the same color, so it is possible to implement the 3D HDR mode in the

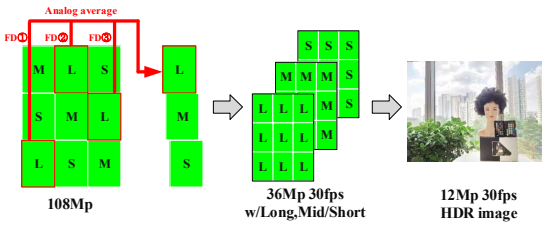


Fig. 10. Proposed Nona HDR structure

Fig. 11. Nona HDR sample image

binning mode. As shown in Fig. 10, the nona HDR is implemented in the binning mode by selectively averaging pixels with the same exposures in 3x3 nonacell based on each 1x3 unit pixel. As a result, in the proposed HDR structure, data can be displayed with a frame rate that is 3 times higher than traditional 3D HDR. A sample image with a dynamic range of 80 dB or more using nona HDR is shown in Fig. 11.

IV. RESULTS AND DISCUSSIONS

The chip was fabricated with 65nm 1-poly 6-metal NMOS process for the top chip and 28nm 1-poly 8-metal CMOS process for the bottom chip. The full resolution of the sensor is 108Mp with 0.8um pixel pitch and nona-patterned color filter array, as shown in Fig. 12. The power consumption is 810mW at the 108Mp 10fps and 600mW at the 12Mp 90fps.

The CIS in which the nonacell technology is applied shows a large-pixel effect which provides improved performance in low lux condition at submicron pixels. Even if the number of photodiodes increases due to the NONACELL technology, the FWC cannot be increased due to the limitation of FD dynamic range and ADC saturation. However, with a privilege of the DCG technology, it is possible to increase FWC in high lux condition.

In order to reduce power in crop mode, adaptive low-power scheme is applied to the column-parallel ADCs especially for the smaller ROI than full resolution and ROI remosaic function that can be removable after a specific area crop was applied.

In the 3x3 pixel cluster, the pixels having the same integration time are selectively read out at the same time, and the frame rate is more than three times higher than the previous method in the 3D-HDR function.

Table 1 lists a performance summary of nonacell. Compared to the tetracell of the same pixel size, it was confirmed that the low lux SNR obtained more than 3.3dB and the high lux SNR obtained more than 2.2dB.

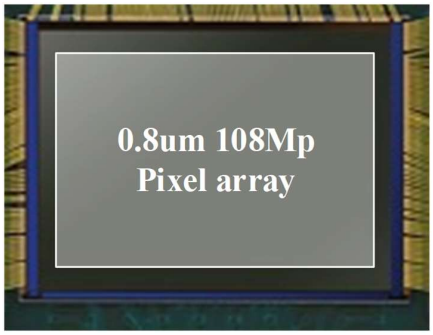


Fig. 12. Die micrograph of 108megapixels CMOS Image Sensor

Table 2 lists a performance summary of the 108Mp CIS. The chip consumes 600mW of total power at a frame rate of 90fps in nona mode achieving an FoM of 0.12e-nJ/DRU.

TABLE I. FWC AND SNR CHARACTERISTICS

	This work		[3]	
Pixel	0.8um Nonacell		0.8um Tetracell	
Mode	Full	Nona	Full	Tetra
Full well capacity(e-)	6,000	54,000	6,000	24,000
20 Lux SNR (dB)	26.0	35.6	25.9	32.3
High Lux SNR (dB)	44.2	51.3	44.2	49.1

TABLE II. PERFORMANCE COMPARISON

	This work		[5]
Pixel count(H)	12,000	4,000	2,560
Pixel count(V)	9,000	3,000	1,536
Full well capacity(e-)	6,000	54,000	7,800
Frame rate(fps)	10	90	60
Analog gain	16	48	8
Random noise(e-)	1.4	3.4	4.3
Power(mW)	810	600	95
FoM=(Power*Noise/(fps*#pixel*DRU$^+$)	0.23	0.12	0.17

DRU^+ = FWC(e-)/Noise(e-)

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