A 0.8 μm Smart Dual Conversion Gain Pixel for 64 Megapixels CMOS Image Sensor with 12k e- Full-Well Capacitance and Low Dark Noise

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***Abstract*—** A 0.8 μm-pitch 64 megapixels ultrahigh-resolution CMOS image sensor has been demonstrated for mobile applications for the first time. Full-well capacity (FWC) of 6k e- was achieved in 0.8 μm pixels as the best in the world, and the advanced color filter (CF) isolation technology was introduced to overcome sensitivity degradation. Dual conversion gain (CG) technology was also first applied to mobile applications to improve the FWC performance of Tetracell up to 12k e-. In addition, highly refined deep trench isolation (DTI) and photodiode design significantly improved dark noise characteristics.

I. INTRODUCTION

A pixel pitch has been constantly reduced for high-resolution image sensors, and has scaled down to 0.9 μm [1]. On the current mobile market, it has strong demands for higher resolution of image sensors. In order to meet this demand, pixels should be reduced to a smaller pitch considering a limitation such as size of the chip. As is well known, however, reducing a pixel pitch degrades the significant characteristics of image sensor such as sensitivity, crosstalk, and full-well capacity (FWC) of photodiode (PD) which affect the signal-to-noise ratio (SNR) in a camera image. In particular, deep trench isolation (DTI), a key technology to reduce crosstalk, is a core process for reducing pixel pitch because it has a great influence on the volume and fill factor of the light receiving unit. Therefore, it is essential that the DTI of 0.8 μm pixels should be narrower and highly refined than that of 0.9 μm pixels, in order to mitigate degradation caused by reducing pixel pitch. As an alternative to improve sensitivity, from the optical structure viewpoint, low refractive index (*n*) material is applied to the grid which decreases optical crosstalk by isolating color filter (CF). This low-*n* material grid technology, named ISOCELL Plus, reduces the surface absorption of light on the grid and yields the total internal reflection easily [2].

Tetracell is one of the most important technology trends for improving sensitivity of submicron pixels. It improves sensitivity by merging four PDs only in low illuminance conditions, whereas it does not provide any FWC gain in high illuminance conditions due to to a limitation in floating diffusion (FD) dynamic range. In order to overcome this, the dual conversion gain (CG) technology has been introduced to improve FWC and SNR by using low CG in high illuminance conditions [3]. In this work, a 0.8 μm 64 megapixels (MP) CMOS image sensor is demonstrated for the first time, including three technologies: Advanced DTI, ISOCELL Plus, and Dual CG.

II. TECHNOLOGY

A. Advanced Deep-Trench Isolation and Photodiodes

For the reduction of pixel pitch from 0.9 μm to 0.8 μm, the DTI process should be highly refined from the previous generation. The main reason for this refinement is to maximize quantum efficiency by extending light incident surface area. With this background, the narrower DTI was implemented in 0.8 μm pixels compared to 0.9 μm pixels. In order to overcome the increased aspect-ratio, the DTI sidewall (SW) oxidation process was also optimized for the complete gap-fill process. Since DTI SW oxidation is particularly sensitive to dark current and white spot characteristics in full-depth DTI structure, it is difficult to change the DTI process. However, the well-refined DTI SW oxidation can reduce dark current and white spots. The main process features between 0.8 μm pixels and previous generation are compared and summarized in Table 1.

To overcome FWC degradation according to the pixel pitch reduction, the ion-implantation process for PD was optimized without any image lags. Based on the advantages of full-depth DTI such as blooming free and complete isolation, the PD volume was expanded by enhancing implant doses to improve potential and adding implant steps to create deeper PD as shown in Fig. 1. In addition, they were elaborately optimized, focusing on lowering electric field between DTI and PD to reduce white spot.

B. ISOCELL Plus

The grid technology for CF isolation is used in 0.8 μm pixels in order to decrease crosstalk, as shown in Fig. 2. These grids were designed to prevent the light from travelling into an adjacent pixel. However, the conventional grids made of metals tended to absorb some of the incident light, which results in optical loss. Thus, by substituting the grids with a low-*n* material, it can reduce the surface absorption, increasing sensitivity by total internal reflection.

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C. Dual Conversion Gain

As shown in Fig. 3, Tetracell is a well-known technology for improving low sensitivity and SNR of the small pixel by combining and outputting four PDs in low illuminance conditions. However, in high illuminance conditions, even if four PDs are merged, there is no FWC enhancement due to the limitation of FD dynamic range, resulting in no SNR gain. The dual CG technology was introduced as a solution to overcome this FWC limit of Tetracell. The basic circuitry of 4-shared pixel consists of four photodiodes (PD), four transfer gates (TG), a selection gate (SEL), a reset gate (RG), a FD, and a source follower (SF). Herein, the circuit of the dual CG pixels is configured by adding another reset gate named DCG, as shown in Fig. 4. Dual CG pixels can switch CG cleverly depending on the illumination environment; they operate with high CG in low illuminance conditions requiring low dark noise, and operate with low CG in high illuminance conditions requiring high FWC. As shown in Fig. 5 (a), the high CG is operated by toggling the RG as a reset while the DCG is always turned on. On the other hand, the low CG is achieved by toggling the DCG as a reset, which enlarges FD capacitance as depicted in Fig. 5 (b). In this work, the low CG value was designed to be half of the high CG value through the adjustment of FD junction and metal parasitic capacitance. This indicates that FWC is doubled in high illuminance conditions as shown in Fig. 6. Consequently, dynamic range is enhanced and the sensor is capable of expressing more detailed image accordingly.

III. Results and Discussion

With the advanced DTI and optimized PD, the FWC performance of 0.8 μm pixels were maintained at the same level, 6k e-, as that of 0.9 μm pixels even though Si volume was reduced by 20 %, as shown in Fig. 7. In addition, the sensitivity is improved by 15 % without noticeable crosstalk increase with ISOCELL Plus technique, as shown in Fig. 8. It was confirmed that optical loss is improved by the substituted grid material. This is because the low-*n* material grid collects much more light into PD with total internal reflection on the surface. Consequently, SNR loss under low illuminance condition due to pixel pitch reduction is significantly decreased by above-described techniques, as shown in Fig. 9.

The measured electrical characteristics of 0.8 μm pixels are compared with those of the conventional 0.9 μm pixels under dark condition. Fig. 10 (a) shows the fixed pattern noise histogram, indicating that the standard deviation is extremely decreased. In particular, the white spots are suppressed dramatically and reduced down to 11 % of the conventional pixels, as shown in Fig. 10 (b). Low electric field PD can be designed in ISOCELL due to the advantages of blooming free and 3-dimensional PD structure. Remarkable white spot improvement was achieved in 0.8 μm pixels compared to 0.9 μm pixels through electric field minimization of PD and high-tech DTI module processes. Dark current is also significantly decreased to 1.5 e-/s, corresponding to 75 % of the conventional pixels, as shown in Fig. 10 (c). In addition to the fixed pattern noise, the temporal noise is considerably improved to 1.2 e-, as shown in Fig. 11. The overall electric characteristics under dark conditions, which are the key factors in CMOS image sensor, are successfully improved.

With the low CG mode, the increased FD capacitance enhances linear FWC. As shown in Fig. 12, FWC of 0.8 μm pixels is twice that of 0.9 μm pixels in the Tetra mode merging four PDs. It was also confirmed that low CG value adjusted through the FD capacitance engineering is the half of high CG value. Consequently, 64 MP CMOS image sensor achieved the performance with 12k e- of FWC in the Tetra mode. In addition, SNR is enhanced by 2.2 dB with high FWC in high illuminance conditions, as shown in Fig. 13. The image is fully saturated due to the low FWC, so that the yellow color is not expressed; whereas it is well represented thanks to high FWC, as shown in Fig. 14. In other words, the color reproducibility becomes superior by increasing dynamic range with high FWC. Pixel characteristics of 0.8 μm pixels are summarized and compared with those of 0.9 μm pixels in Table 2. They show better performances even with smaller pixel pitch. Well-designed layout architecture, optimized ion-implantation for photodiode and transistors with well-tuned anneal process, ISOCELL Plus, and advanced DTI module process lead the enhancement of performances.

IV. Conclusion

A 0.8 μm 64 MP ultrahigh-resolution CMOS image sensor has been demonstrated and launched for mobile application, as shown in Fig. 15. The performances of 0.8 μm pixels mostly showed better results than those of the conventional 0.9 μm pixels, in terms of electrical and optical characteristics. Using dual CG technology, FWC is increased up to 12k e-, which is twice as that of 0.9 μm pixels in the Tetra mode. Accordingly, SNR under high illuminance condition was enhanced by 2.2 dB. In addition, the key dark noise characteristics such as white spot, dark current and temporal noise, were significantly suppressed by the advanced DTI module and the optimization of photodiode. Moreover, 0.4 dB improvement of SNR according to 15 % enhancement of sensitivity was obtained with ISOCELL Plus technology. We certainly expect this 0.8 μm 64 MP CMOS image sensor to meet market demands for high-resolution mobile cameras as well as accelerate submicron pixel trends.

Acknowledgment

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Process	0.9 µm	0.8 µm
Critical dimension of DTI (a. u.)	1.00	0.94
Aspect ratio	38:1	45:1
DTI sidewall oxidation	Ref.	New
Photodiode	Ref.	Deeper N-well
Grid for CF isolation	Metal	Low-*n* material

Table 1. Comparison of process technology.

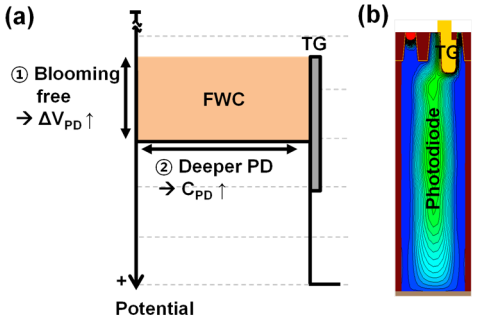

Fig. 1. (a) Schematic diagram of achieving high FWC. (b) TCAD potential profile of 0.8 µm unit pixel.

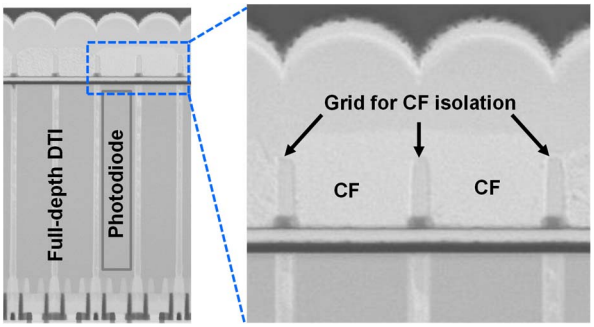

Fig. 2. Cross-sectional TEM image of 0.8 µm pixels with low-*n* material grid.

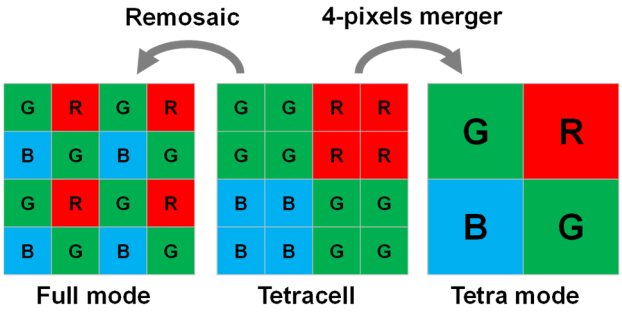

Fig. 3. Tetracell diagram which is transformed to the Full mode and the Tetra mode respectively.

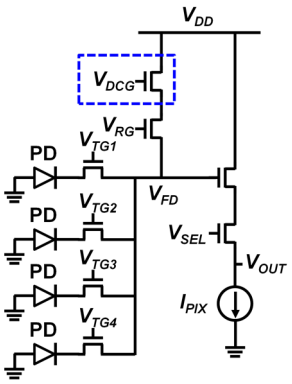

Fig. 4. Schematics of 4-shared pixels with dual CG which DCG transistor (blue box) is added.

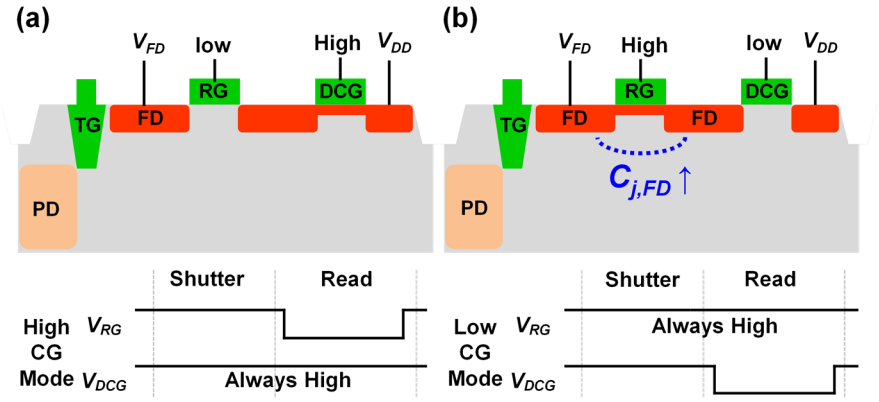

Fig. 5. Pixel device schematics at the read time and timing diagram of (a) high CG and (b) low CG.

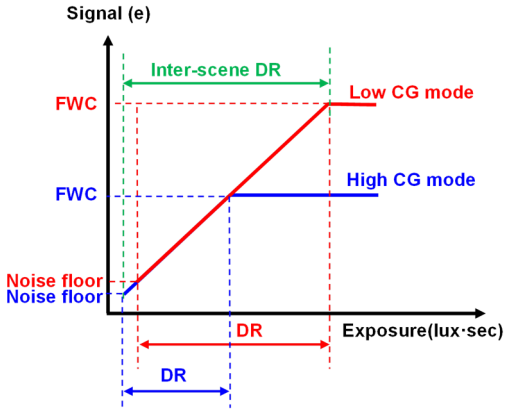

Fig. 6. Photoelectric conversion characteristics in a high CG mode (blue) and a low CG mode (red).

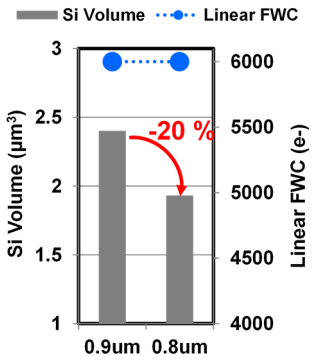

Fig. 7. Si physical volumes (bar) and unit pixel FWC (circle).

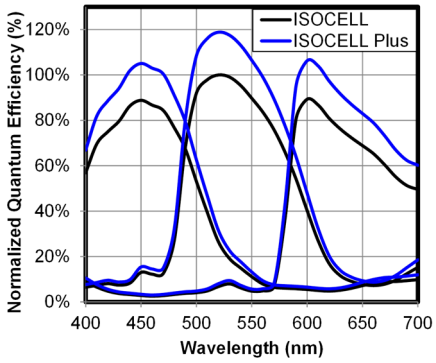

Fig. 8. The normalized quantum efficiency of ISOCELL and ISOCELL Plus [2].

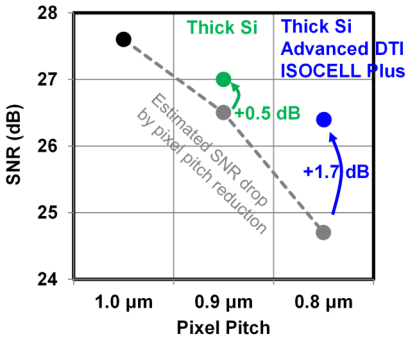

Fig. 9. SNR improvement in 0.8 µm pixel under low illuminance condition.

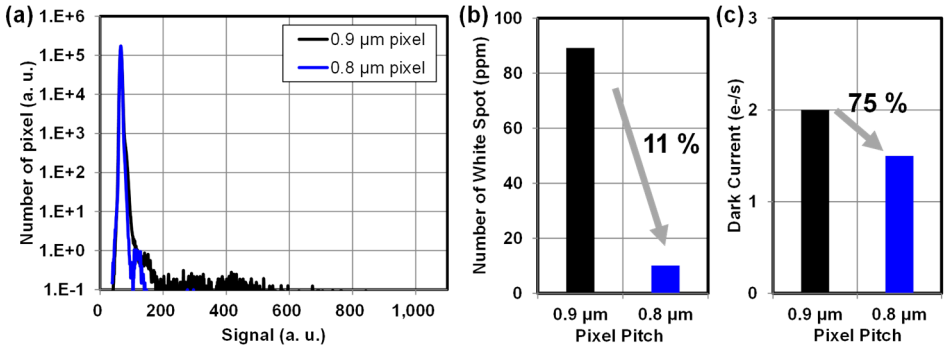

Fig. 10. (a) The histograms of dark fixed pattern noise at T_a = 60 ºC. (b) The decreased number of white spot and (c) the reduced dark current at T_j = 60 ºC in 0.8 µm pixel.

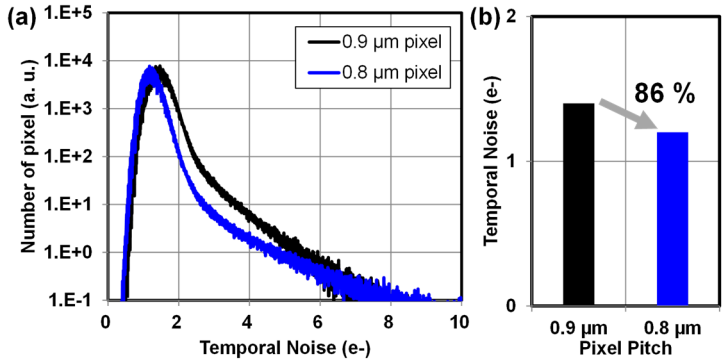

Fig. 11. (a) The histograms of dark temporal noise and (b) the decreased averaged value in 0.8 µm pixels.

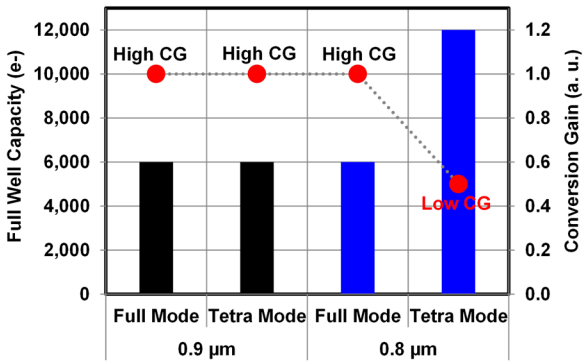

Fig. 12. The relation between FWC (bar) and CG (circle) at the Full mode and the Tetra mode.

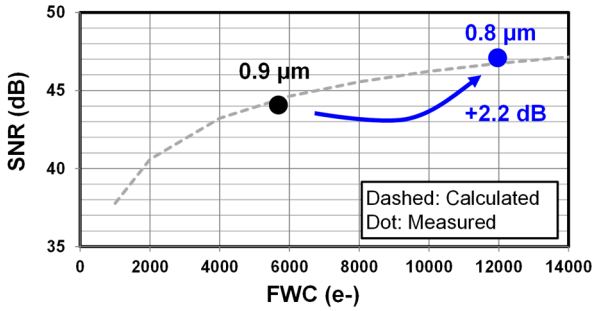

Fig. 13. SNR trend in the Tetra mode according to FWC of PD under high illuminance condition.

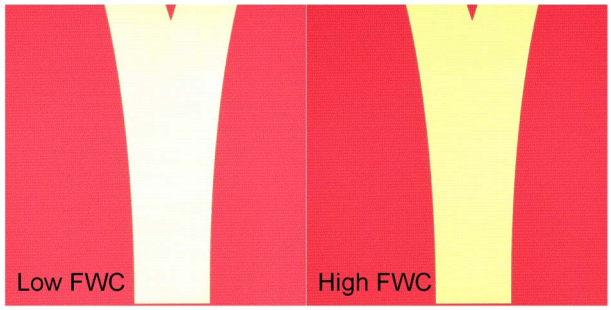

Fig. 14. The images comparing the color reproducibility of low FWC and high FWC in high illuminance conditions.

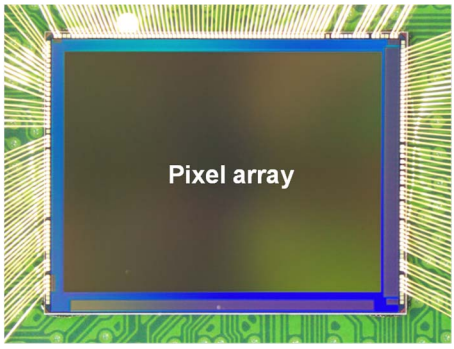

Fig. 15. Die micrograph of 64 megapixels CMOS Image Sensor.

Characteristics		Unit	0.9µm ISOCELL	0.8µm ISOCELL PLUS
Linear full-well capacity	at Full mode	e-	6,000	6,000
	at Tetra mode	e-	6,000	12,000
G-sensitivity		e/lux.sec	2,600	2,300
Image lag		e-	<1.0	<1.0
Crosstalk		%	14.2	14.5
Temporal noise		e-	1.4	1.2
RTS (>30LSB)		ppm	1	1
White spot (T_j 60 °C)		ppm	90	10
Dark current (T_j 60 °C)		e-/s	2.0	1.5

Table 2. Comparison of pixel characteristics.