Core8	Core7	Core6	Core5	Core4	Core3	Core2	Core1		
								Registers	2-4 KB, ~1 Cycle
								L1 instruct / L1 data	32-64KB (each), ~3-5 cycls
								L2 Cache	512KB - 2MB, ~10-18 Cycles

L3 Cache

64MB - 256MB, ~35-60 cycles, shared