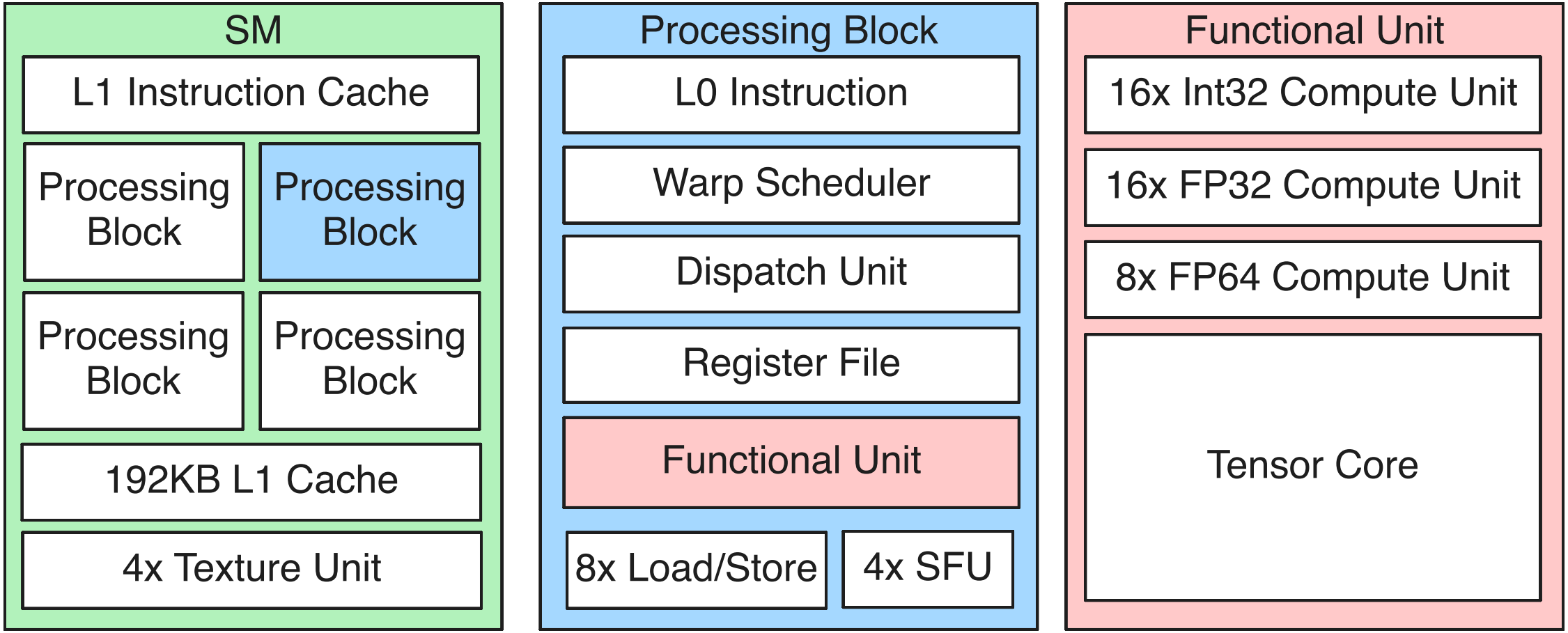
SM
L1 Instruction Cache
Processing Block
Processing Block
Processing Block
Processing Block
192KB L1 Cache
4x Texture Unit
Processing Block
L0 Instruction
Warp Scheduler
Dispatch Unit
Register File
Functional Unit
8x Load/Store
4x SFU
Functional Unit
16x Int32 Compute Unit
16x FP32 Compute Unit
8x FP64 Compute Unit
Tensor Core