

RWTH Aachen University  
Department of Computer Science

# Design and Performance Engineering of GPU-Accelerated Tensor Network Algorithms for Large-Scale Scientific Simulations

Master Thesis

submitted by

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# Abstract

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# Listings



# List of Symbols

$\mathcal{T}$	Tensor
$\mathbf{A}, \mathbf{B}$	Matrices
$\mathbf{v}$	Vector
$\chi$	Bond dimension
$d$	Local (physical) dimension
$N$	Matrix/problem size
$\mathcal{O}(\cdot)$	Asymptotic upper bound





# List of Abbreviations

BLAS	Basic Linear Algebra Subprograms
DFT	Density Functional Theory
GEMM	General Matrix Multiply
GPU	Graphics Processing Unit
HBM	High Bandwidth Memory
HPC	High Performance Computing
MPI	Message Passing Interface
MPS	Matrix Product State
SM	Streaming Multiprocessor
TN	Tensor Network



# **1. Introduction**

## **1.1. Motivation**

## **1.2. Problem Statement**

## **1.3. Contributions**

## **1.4. Outline**

The remainder of this thesis is structured as follows. Chapter 2 introduces ...Chapter 3 presents ...Chapter 4 details ...Chapter 5 evaluates ...Chapter 6 summarises ...



## **2. Background**

### **2.1. Tensor Networks**

#### **2.1.1. Tensor Notation and Diagrams**

#### **2.1.2. Tensor Contraction**

#### **2.1.3. Tensor Network Structures**

### **2.2. GPU Architecture**

#### **2.2.1. Streaming Multiprocessor and Warp Execution**

#### **2.2.2. Memory Hierarchy**

#### **2.2.3. NVIDIA A100 Ampere Architecture**

### **2.3. CUDA Programming Model**

#### **2.3.1. Thread Hierarchy and Kernel Launch**

#### **2.3.2. Shared Memory and Synchronisation**

#### **2.3.3. Memory Coalescing and Bank Conflicts**

#### **2.3.4. Performance Profiling with Nsight Compute**

### **2.4. Related Work**

#### **2.4.1. cuBLAS and cuTENSOR**

#### **2.4.2. ChASE Eigensolver**

#### **2.4.3. Existing GPU Tensor Network Implementations**



## **3. Design and Methodology**

**3.1. Target Kernels**

**3.2. Algorithmic Approach**

**3.3. Data Layout and Memory Strategy**

**3.4. Baseline Selection**





## **4. Implementation**

### **4.1. Kernel Design**

### **4.2. Shared Memory Tiling**

### **4.3. Occupancy and Launch Configuration**

### **4.4. Integration and Build System**



## **5. Results**

### **5.1. Experimental Setup**

### **5.2. Single-GPU Performance**

### **5.3. Profiling Analysis**

### **5.4. Comparison with cuBLAS and cuTENSOR**

### **5.5. Scaling Behaviour**

### **5.6. Discussion**



## **6. Conclusion**

### **6.1. Summary**

### **6.2. Limitations**

### **6.3. Future Work**



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## A. Supplementary Benchmarks

TODO



# Declaration of Authorship

I hereby declare that I have created this work completely on my own and used no other sources or tools than the ones listed, and that I have marked any quotes accordingly.

Aachen, February 17, 2026

Daniel Sinkin