Report for E-design 344

by

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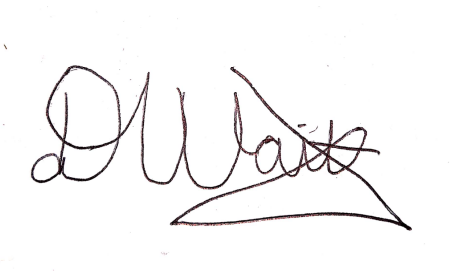
E-Design report # 1

August 2019

Declaration

By submitting this report electronically, I declare that the entirety of the work contained therein is my own, original work, that I am the sole author thereof (save to the extent explicitly otherwise stated), that reproduction and publication thereof by Stellenbosch University will not infringe any third party rights and that I have not previously in its entirety or in part submitted it for obtaining any qualifcation.



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D.B. Wait

Date: 09/08/2019 .....

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Chapter 1

Power supply system design

1.1 System overview

The system discussed is designed to convert an AC signal from the wall-socket into 5 VDC and −5 VDC rails. A transformer steps down the 240 VAC signal to a 18 VAC signal which is rectified with a small ripple. The rectified signal is input to a switch-mode regulator which produces a 14 VDC signal. This signal is used fed to both a 5 VDC linear voltage regulator and an inverting charge-pump circuit. Figure 1.1 represents the system on the PCB.

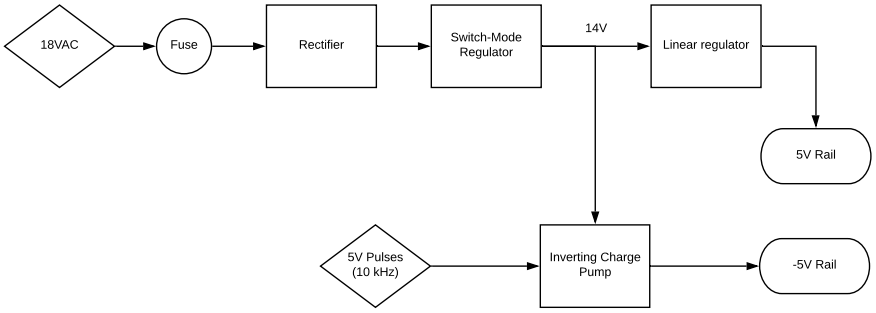


Figure 1.1: System diagram

1.2 Rationale

It was decided to use a switch mode regulator as an intermediate to step-down the rectified voltage for two reasons. Firstly, the elements in the inverting charge-pump result in a considerable voltage drop - so a larger input than 5 VDC is required. Secondly, if the rectified output was used as an input to the linear regulator, it may overheat.

Chapter 2

Rectifier

2.1 Theory and related work

Figure 2.1 demonstrates the generic setup of a half-wave rectifier [1, p.75]. Considering that the switch-mode regulator is connected to the output, the design was intended for the requirements specified in the switch-mode's datasheet [2]

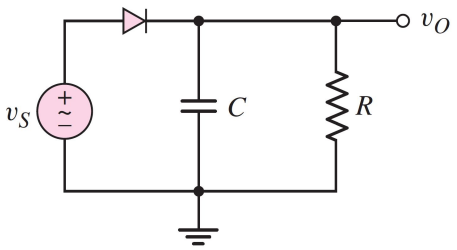


Figure 2.1: Half-Wave Rectifier

2.2 Design

The input voltage to the rectifier is 18 VAC, an 1N4007 diode with a voltage drop of 1.1 VDC [3, p.2] rejects negative voltage. The capacitance was chosen to be 220 µF as recommended [2, p.25]. The following calculation was used to check that, for a load that draws 100 mA, the capacitor is large enough to deliver current:

$$i = C\frac{\Delta V}{\Delta t}. \tag{2.1}$$

Assuming a linear ripple voltage from the capacitor, one can solve for the rate of change of voltage with a straight line from the peak voltage to the minimum

desired voltage over the capacitor. The minimum voltage was selected to be 8 V.

$\Delta V = (V_{peak} - V_{diode}) - V_{min} = (18\sqrt{2} - 1.1) - 8$

$t_{period} = \frac{1}{f} = \frac{1}{50} = 20\,\text{ms}$

$t_{min} = \frac{\arccos \frac{V_{min}}{V_{peak} - V_{diode}}}{2\pi f} = 4\,\text{ms}$

$\Delta t = t_{period} - t_{min} = 16\,\text{ms}$

Solving for the minimum capacitance: $C = \frac{i\Delta t}{\Delta V} = 98\,\mu\text{F}$

Therefore, 220 µF should meet the requirements - with a smaller ripple.

2.3 Simulation

Figure 2.2 is the LTSpice result of my design measured at the switch-mode regulator.

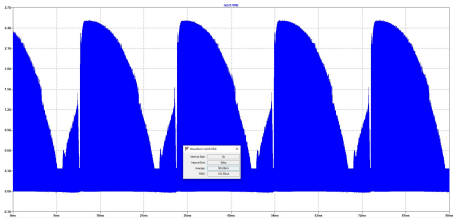


Figure 2.2: Rectifier Output Current (RMS = 103.55mA)

2.4 Measurements

Figure 2.3 is the oscilloscope reading of the rectifier with the bulky 100 Ω load.

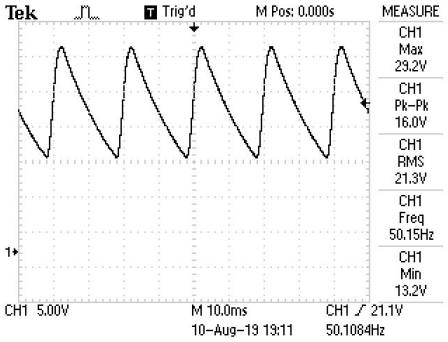


Figure 2.3: Rectifier output (DC Coupled)

Chapter 3

Switchmode regulation

3.1 Theory and related work

This particular switch-mode regulator uses a charge-pump styled design to step-down the voltage. Also called a buck-converter, switching transistors control the flow of current through capacitors and/or inductors to output a smaller voltage [4]. This buck-converter switches at 150 kHz [2, p.1] which generates noise of the same frequency throughout the system, however it is useful as a pre-regulator due to the high input voltage to the system.

3.2 Design

The switch-mode was connected in an adjustable output implementation so that possible design changes could be facilitated. Figure 3.1 is the diagram taken directly from [2, p.26].

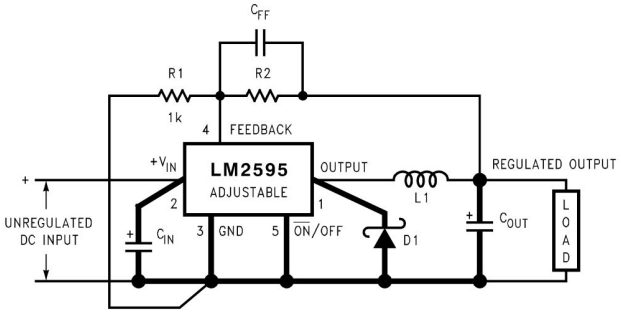


Figure 3.1: Adjustable Output Switch-Mode Regulator

[2, p.15] recommends that the input capacitance be 1.25 times greater than the peak input voltage. Therefore, the capacitor in the rectifier circuit is rated at 50 V.

The given formula allows one to select resistors for a desired voltage.

$$V_{out} = V_{ref}(1 + \frac{R_2}{R_1}) \tag{3.1}$$

An output of 13 V is needed to power the inverting charge-pump discussed later, therefore, for $V_{ref} = 1.23\,\text{V}$ and $R_1 = 1\,\text{k}\Omega$, the nearest E-12 resistor value for R_2 is $10\,\text{k}\Omega$.

The feed-forward capacitor was chosen according to 3.2 to be 4.7 nF

$$C_{FF} = \frac{1}{31 \times 10^3 \times R_2} \tag{3.2}$$

The recommended inductor for L_1 is 100 µH. However, the largest available inductor was 68 µH.

Lastly, the output capacitor was selected to be 100 µF.

3.3 Simulation

According to the LTSpice simulation, as seen in Figure 3.2, the regulator delivers the expected voltage across a $100\,\Omega$ load albeit quite noisy.

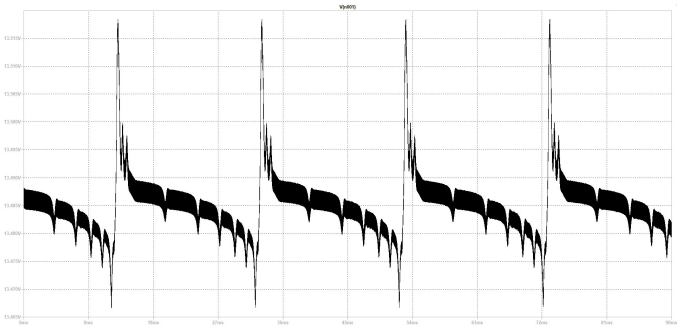


Figure 3.2: SPICE output of switch-mode regulator

3.4 Measurements

Figure 3.3 is an oscilloscope reading of the output of the built circuit with a 100 Ω load.

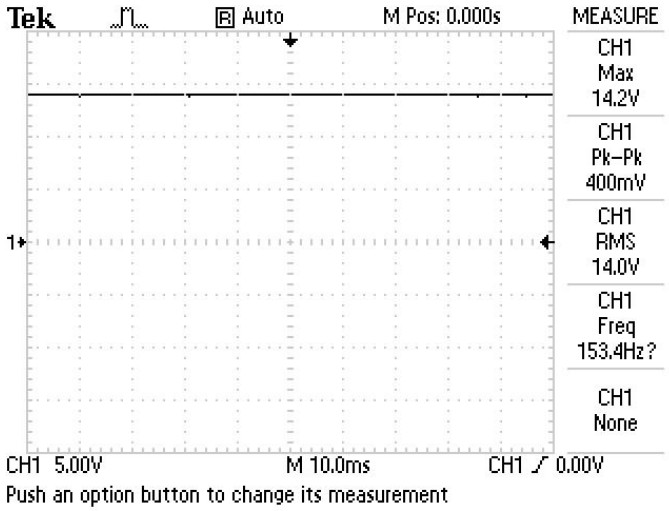


Figure 3.3: Switch-mode regulator output

Chapter 4

Linear regulation

4.1 Theory and related work

Linear regulators have proven to be reliable from experience and cause less noise than a switch-mode regulator. High frequency noise can be filtered well with bypass capacitors. Thus, in order to deliver a smooth 5 VDC rail, the linear regulator was used.

4.2 Design

The switch-mode's output capacitor smooths the input to the linear regulator ($C_I = 100\,\mu F$).

A 0.1 µF bypass capacitor (C_O) is on the output of the linear regulator as recommended [5, p.8].

4.3 Simulation

According to Figure 4.1 this setup is suffice for a 50 Ω load with negligible noise.

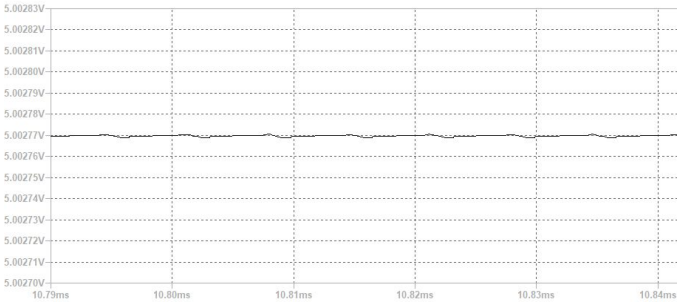


Figure 4.1: SPICE output of switch-mode regulator

4.4 Measurements

Due to the 150 kHz noise coming from the switch-mode, a capacitance of 0.1 µF places a pole too far from the frequency which needs to be attenuated. As a matter of fact, the practical results work better without that capacitor. By Equation 4.1, it is possible to determine the ideal capacitance for this circuit [1, p.492].

$$f_c = \frac{1}{2\pi RC} \tag{4.1}$$

Choosing a corner frequency of 15 kHz and a resistance of 50 Ω, it would seem that a capacitor of at least 220 nF is required.

Figure 4.2 shows the linear regulator's current output.

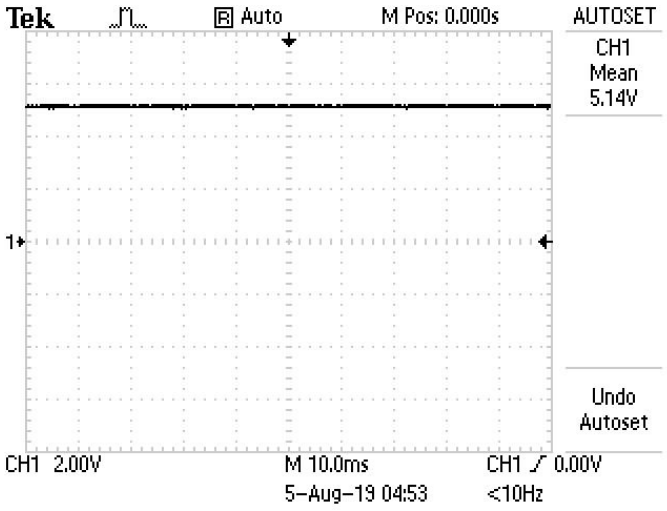


Figure 4.2: 5V rail from linear regulator

Chapter 5

Charge pump regulation

5.1 Theory and related work

The fundamental design was inspired by [6] as shown in Figure 5.1. During the design of the charge-pump, it seemed that I somehow needed to improve the circuit so that it could deliver more current to a load. After seeing a few designs which used push-pull amplifiers, I found a schematic using three NPN transistors as shown in Figure 5.2 [7].

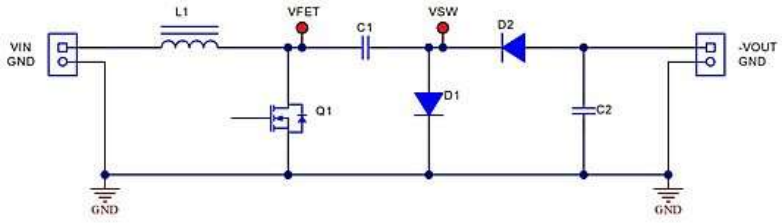


Figure 5.1: Transistor controlled inverting charge pump

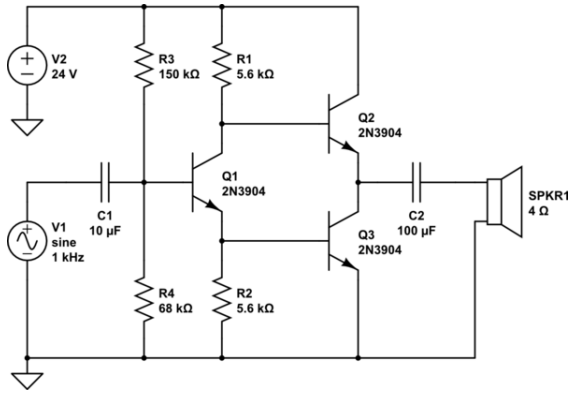


Figure 5.2: Push-pull amplifier using 3 NPN BJTs

5.2 Design

By using a BJT as a 'NOT gate', the pulse train delivered to each BJT in the Class B amplifier is out of phase. Thus, the amplifier's BJTs act as switches to control the inverting charge-pump.

In order to keep the RMS current through the transistors below 200 mA [8, p.1], resistors were placed at the collectors of the phase-shifter and first transistor of the push-pull configuration.

Due to the losses in the diodes, there needs to be an oscillating 7.2 V output from the amplifier.

A low impedance resistor and a zener diode are used to clamp the inverted voltage to −5 V similar to the design at [1, p.85].

There were many iterations of the design due to the difference between simulated circuits versus practical circuits. Figure 5.3 is the LTSpice model of the final working design.

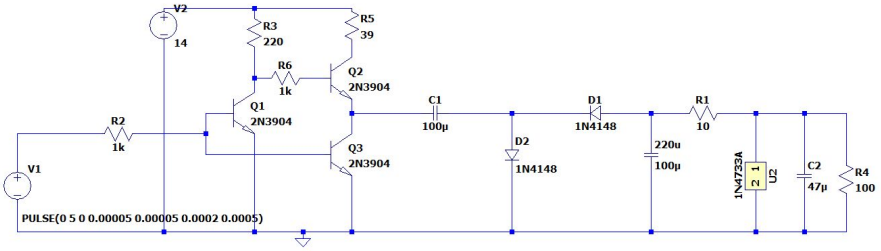


Figure 5.3

5.3 Simulation

Figure 5.4 shows the output from the charge pump and the clamped output from the zener regulator.

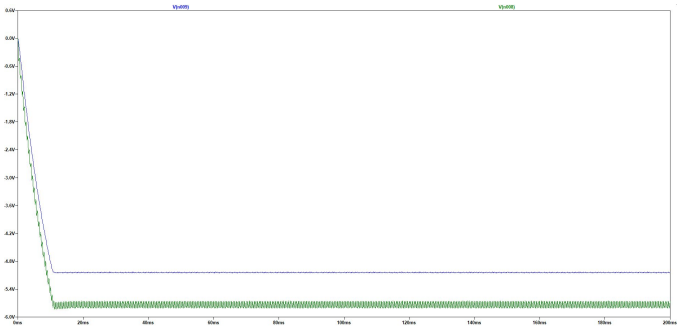


Figure 5.4: Green - Inverter output. Blue - Clamper output

5.4 Measurements

The charge-pump's zener-regulated output is shown in Figure 5.5

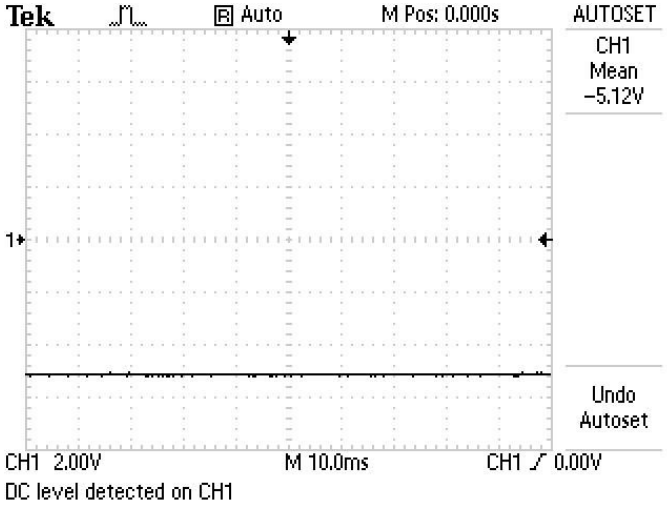


Figure 5.5: -5V rail from charge-pump

Chapter 6

System test results

Certainly, integrating each sub-system described in the previous chapters called for adjustments to the original design. However, the design was as modular and easily adjustable as could be managed - so few changes were needed.

The system fulfills the minimum requirements and none of the components are at risk of exceeding their power-ratings according to my calculations - which have been excluded from the report due to length constraints.

Objectively, the noise caused by the switch-mode regulator is less than ideal for the ADCs which will be implemented later. Therefore, further measures will be implemented for noise rejection.

References

[1] Neamen, D.A.: *Microelectronics*. McGraw Hill, 2010.

[2] *LM2595 SIMPLE SWITCHER Power Converter 150-kHz 1-A Step-Down Voltage Regulator*. Texas Instruments, May 2016.

[3] *1N4001-1N4007 General-Purpose Rectifiers*. Fairchild Semiconductor, 2014.

[4] Tech Web: Switching regulator basics: Step-down operation principles. 2016.
Available at: `https://micro.rohm.com/en/techweb/knowledge/dcdc/dcdc`$_s r/dcdc_s r$01/696

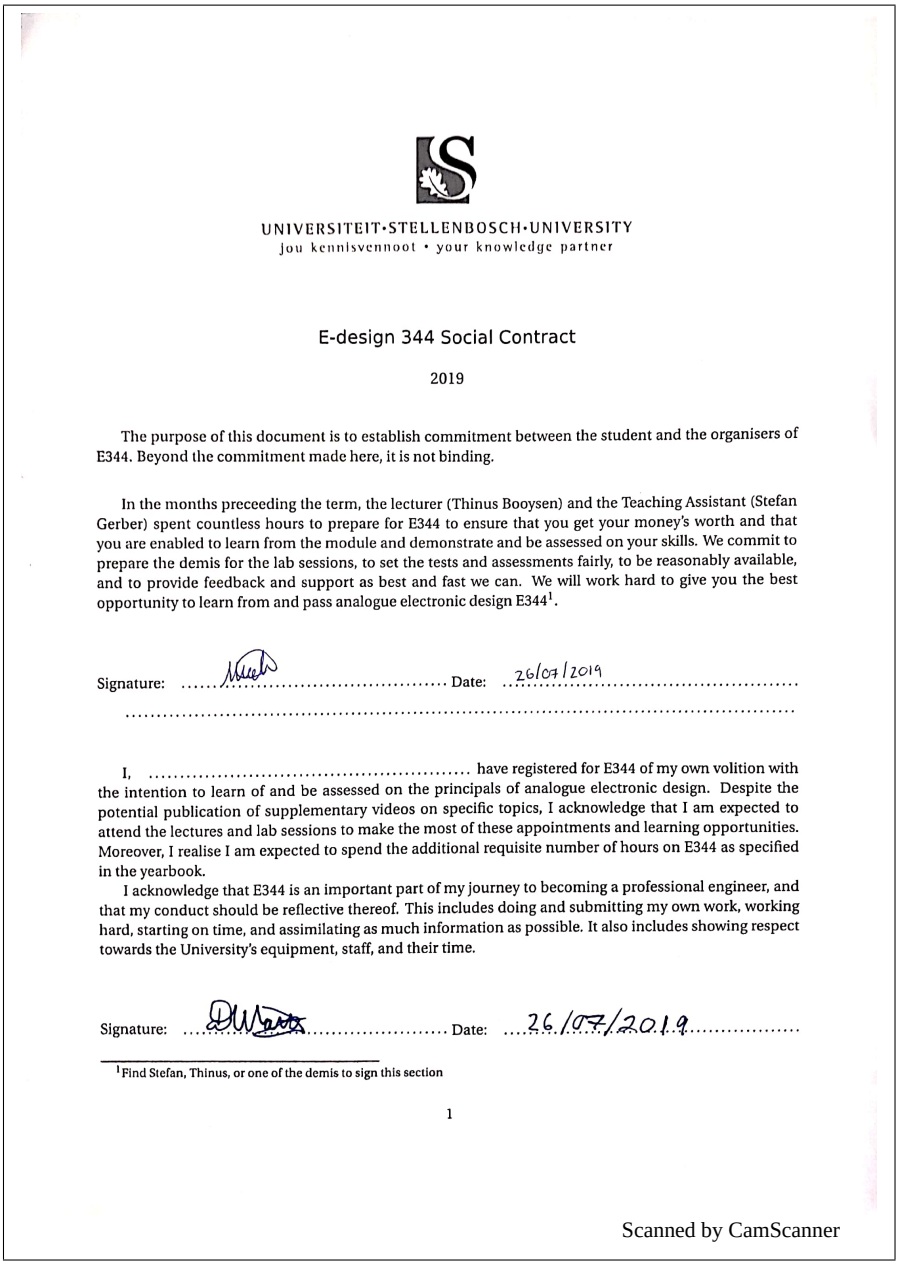
[5] *MC78LXXA / LM78LXXA 3-Terminal 0.1 A Positive Voltage Regulator*. Fairchild Semiconductor, 2013.

[6] EDN Asia: How to design a high voltage dcm inverting charge pump converter. 2019.
Available at: `https://www.ednasia.com/news/article/How-to-design-a-high-voltage-DCM-inverti`

[7] Stack Exchange: How to keep current from draining out the bottom of this push-pull amplifier? 2018.
Available at: `https://electronics.stackexchange.com/questions/374108/how-to-keep-current-fr`

[8] *2N3904 SMALL SIGNAL NPN TRANSISTOR*. ST, 2003.

Appendix A: Social contract



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E-design 344 Social Contract

2019

The purpose of this document is to establish commitment between the student and the organisers of E344. Beyond the commitment made here, it is not binding.

In the months preceeding the term, the lecturer (Thinus Booysen) and the Teaching Assistant (Stefan Gerber) spent countless hours to prepare for E344 to ensure that you get your money's worth and that you are enabled to learn from the module and demonstrate and be assessed on your skills. We commit to prepare the demis for the lab sessions, to set the tests and assessments fairly, to be reasonably available, and to provide feedback and support as best and fast we can. We will work hard to give you the best opportunity to learn from and pass analogue electronic design E344[1].

Signature: ..... Date: 26/07/2019

I, ... have registered for E344 of my own volition with the intention to learn of and be assessed on the principals of analogue electronic design. Despite the potential publication of supplementary videos on specific topics, I acknowledge that I am expected to attend the lectures and lab sessions to make the most of these appointments and learning opportunities. Moreover, I realise I am expected to spend the additional requisite number of hours on E344 as specified in the yearbook.

I acknowledge that E344 is an important part of my journey to becoming a professional engineer, and that my conduct should be reflective thereof. This includes doing and submitting my own work, working hard, starting on time, and assimilating as much information as possible. It also includes showing respect towards the University's equipment, staff, and their time.

Signature: ..... Date: 26/07/2019

[1] Find Stefan, Thinus, or one of the demis to sign this section

1

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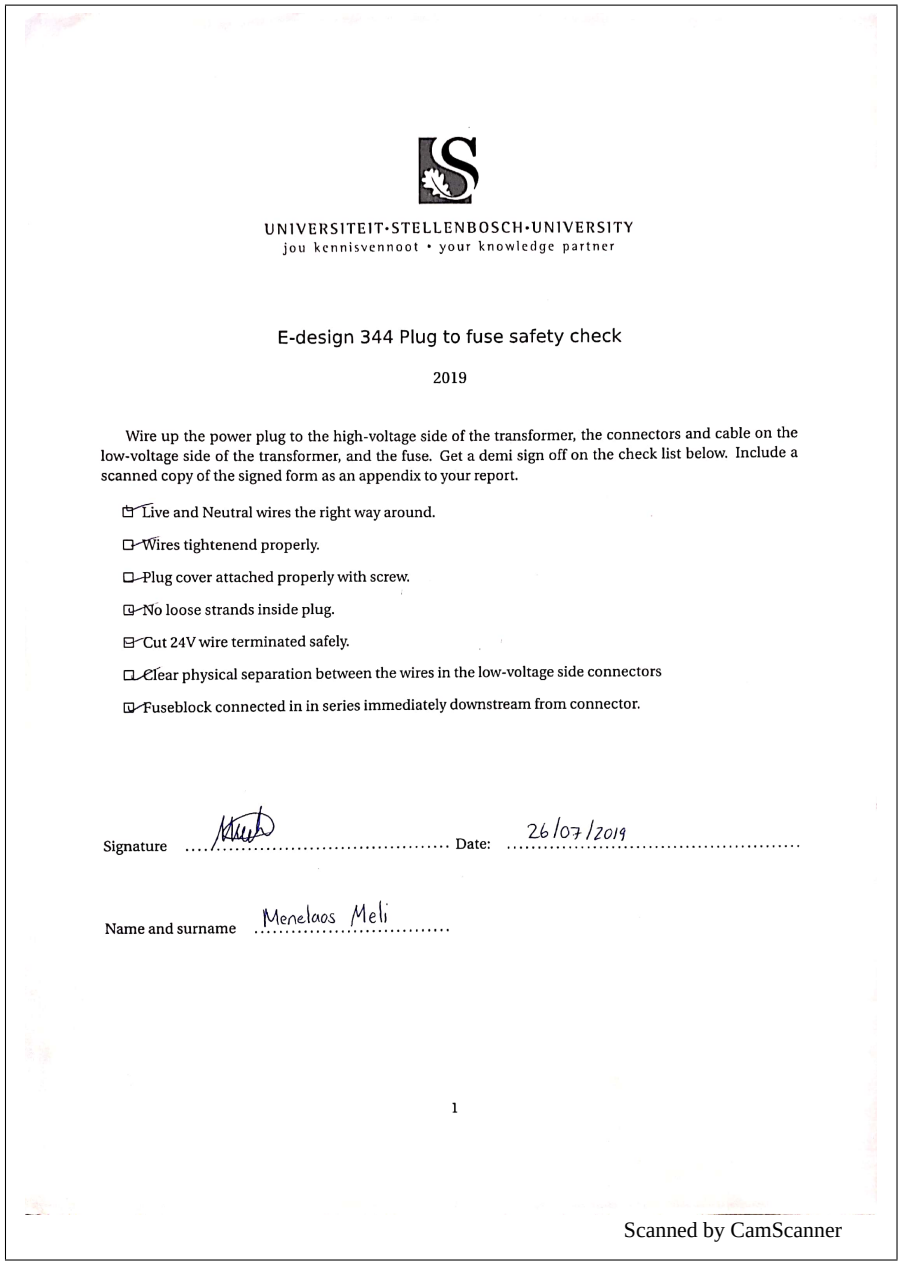
Appendix B: Wiring safety check



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E-design 344 Plug to fuse safety check

2019

Wire up the power plug to the high-voltage side of the transformer, the connectors and cable on the low-voltage side of the transformer, and the fuse. Get a demi sign off on the check list below. Include a scanned copy of the signed form as an appendix to your report.

- ☑ Live and Neutral wires the right way around.
- ☑ Wires tightenend properly.
- ☑ Plug cover attached properly with screw.
- ☑ No loose strands inside plug.
- ☑ Cut 24V wire terminated safely.
- ☑ Clear physical separation between the wires in the low-voltage side connectors
- ☑ Fuseblock connected in in series immediately downstream from connector.

Signature ..... Date: 26/07/2019

Name and surname Menelaos Meli

1

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Appendix C: Screengrab of GitHub repo