Report for E-design 344

by

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E-Design report # 2

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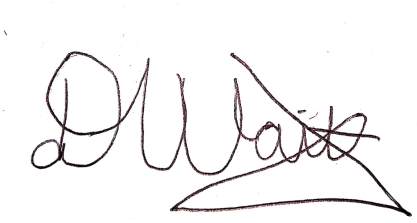

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D.B. Wait

Date: 23/09/2019

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Chapter 1

Signal conditioning system design

The colour-coded block diagram as shown in Figure 1.1 represents the design of the system to transduce the peak voltage (blue) and peak current (yellow) through a load, as well as the absolute phase-shift between them (green). The design is required to measure: an input voltage between 12 VAC to 20 VAC; a current through the load of 0 mA to 285 mA; and an absolute phase-shift of 0° to 45°. Each transducer's output shall be represented on a 0 V to 5 V, 10-bit ADC.

The 5 V and −5 V rails from Assignment 1 are designed to output at least 50 mA. The system uses 7 TLC2272 op-amps and a TL081 op-amp resulting in a maximum current consumption of 23.8 mA. Therefore, the rails should work.

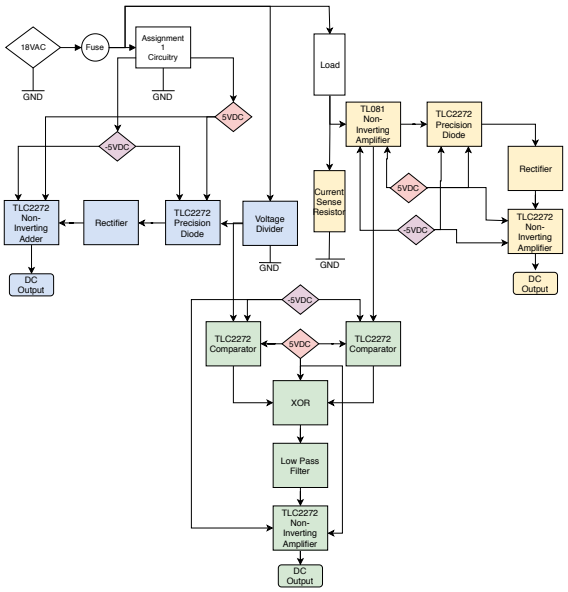


Figure 1.1: System diagram

Chapter 2

Voltage peak transducer

2.1 Theory and related work

In order to transform an AC voltage into a DC voltage output, rectification will be necessary. A simple half-wave rectifier would use a 1N4007 rectifying diode which has a forward-voltage of 1.1 V [1, p.2]. In order to induce a negligible voltage drop over the diode, a 'precision-diode' configuration is used. The precision-diode functions by using the diode's cathode as feedback to the op-amp such that the output of the precision-diode matches the positive cycle of the input voltage [2, p. 654] and $V_{in+} = V_{in-} = V_{out}$.

For a half-wave rectifier, the Equation 2.1 can be used to calculate the RC constant (τ) for given parameters [2, p.76]. It is important to note that multiplication of V_L and V_M by the same factor has no affect on τ.

$$V_L = V_M e^{-t/\tau} \tag{2.1}$$

This project also implements a non-inverting summing amplifier with two inputs. The output of such a configuration is to be calculated with the following equation [3]:

$$V_{out} = (1 + \frac{R_f}{R_g})(V_1 \frac{R_{in2}}{R_{in1} + R_{in2}} + V_1 \frac{R_{in1}}{R_{in1} + R_{in2}}) \tag{2.2}$$

The supply voltage from the transformer regularly exceeds 18 VAC and may be up to 22 VAC for the no-load condition. Hence, the design parameters have been adjusted for a range of 12 VAC to 23 VAC.

2.2 Design

Figure 2.1 is the product of the design choices below.

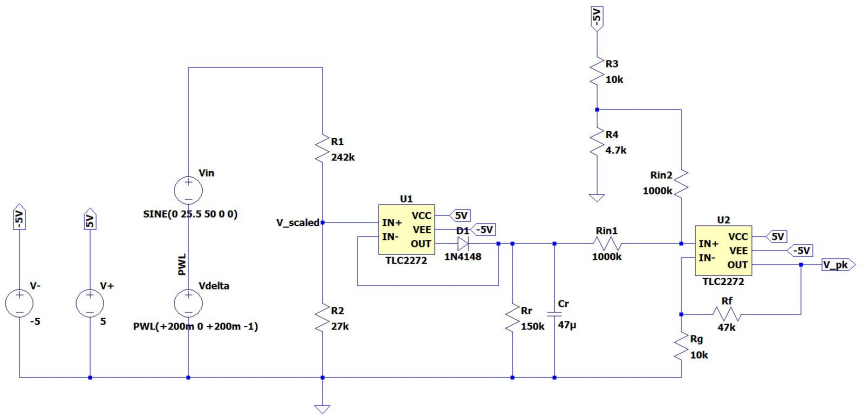


Figure 2.1: Voltage Transducer circuit

Firstly, the input AC voltage is divided with high-impedance resistors. This scaled voltage is input to the precision diode. To account for the maximum common-mode voltage of the TLC2272, the scaled voltage may be no more than 3.5 V. The transformer output may be as large as 31 Vpk, hence I chose to scale down the input voltage by a factor of 10 so that the common-mode limit will not be exceeded.

$$\frac{1}{10} = \frac{R2}{R1+R2}$$

Choosing R2 = 27 kΩ to ensure a high series impedance, R1 = 243 kΩ which can be approximated with a series combination of 220 kΩ and 22 kΩ resistors.

Secondly, the scaled voltage is half-wave rectified. The rectified signal ripple must meet the 150 mV accuracy requirement while preserving the ability to detect a 1 V change at the input within one second. Using the given Equation 2.1, the minimum value of τ can be determined such that a 23 VAC drops by 150 mV over a 20 ms period:

$$\tau_{min} = \frac{-0.02}{\ln(\frac{23\sqrt{2}-0.15}{23\sqrt{2}})} = 4.33$$

Similarly, for a minimum voltage of 16 VAC, to detect a 1 V decrease within 1 s, the maximum value of τ can be calculated:

$$\tau_{max} = \frac{-1}{\ln(\frac{16\sqrt{2}-1}{16\sqrt{2}})} = 22.12$$

Therefore, a resistor of 150 kΩ and a capacitor of 47 µF results in an acceptable $\tau = RC = 7.05$.

Finally, the rectified signal is passed to a non-inverting summing amplifier [3] which scales the voltage such that the original input of 12 VAC to 23 VAC lies within a range of 0 VDC to 5 VDC.
The amplifier takes the rectified signal and a DC offset as the inputs - both input resistances are 1 MΩ for simplicity. The negative rail is used to create an offset at the second input of the amplifier such that 12 VAC translates to 0 V. Thus, the negative rail divided with resistors (R3 and R4) to match an input of 12 VAC (divided and rectified to 1.7 V).
The gain of the non-inverting adder is designed so that 23 VAC represents at most 4.85 V in compliance with the minimum high-level output voltage of the TLC2272 for low currents [4, p.7]. Therefore, a gain of 5.7 is chosen with $R_f = 47\,\text{k}\Omega$ and $R_g = 10\,\text{k}\Omega$

2.3 Simulation

The design was validated with an LTSpice simulation to ensure that the design requirements are met. Figure 2.2 is the result of the simulation of the circuit in Figure 2.1. The graphic depicts the scaled voltage, input voltage decrements, and DC voltage output of the voltage transducer for an 18 VAC input.

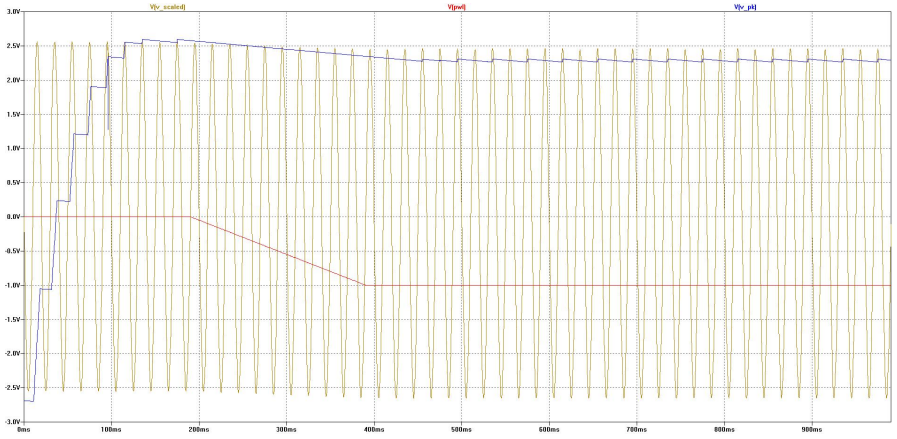


Figure 2.2: Voltage Transducer Circuit

2.4 Measurements

The design was rigorously tested with emulated input voltages in order to determine the accuracy of the deduced input from the analogue output. The deduced input

column is calculated from the circuit design to demonstrate the deviation from the expected output.

Emulated Input (Vpk)	Signal Generator Selected (Vpk-pk)	Signal generator Measured (V+pk)	Analogue output (Vdc)	Deduced input (Vpk)	Difference (mV)
16	1.577885693	1.6	-0.19	16.2635983	263.598304
21	2.070974972	2.12	1.25	21.30595278	305.952784
21.15	2.08576765	2.14	1.3	21.48103454	331.0345368
21.3	2.100560329	2.16	1.34	21.62109994	321.0999391
26	2.564064251	2.62	2.68	26.31329091	313.2909135

Figure 2.3: Emulated Voltage Transducer tests

Table 2.3 was used to generate an accurate linear model as shown in Figure 2.4. This model is to be used in the integrated test's calculation.

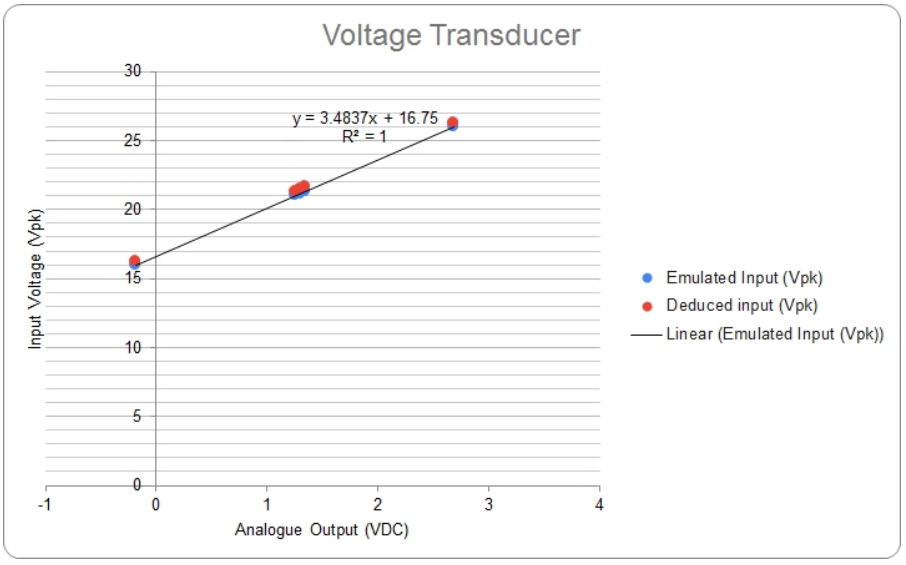
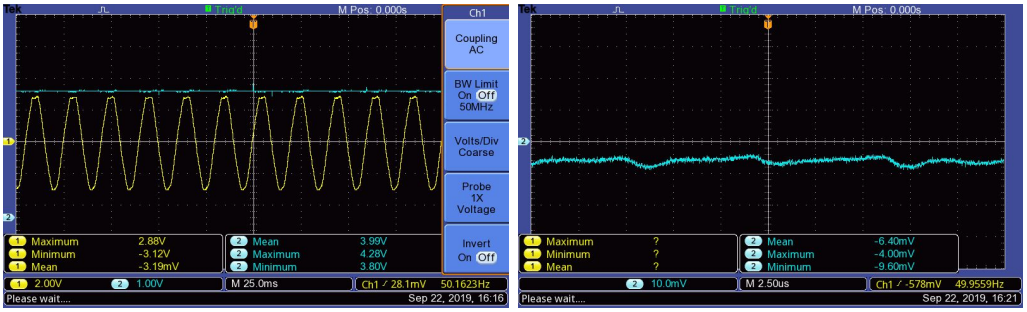


Figure 2.4: Voltage Transducer: Linear function of analogue output vs input voltage

The integrated test in Figure 2.5 verifies that inaccuracies in the output can be compensated for with the above linear equation.

Measurement	Load R	Scaled input (Vpk)	Input (Vpk)	Analogue output (Vd	Deduced input (Vpk)	Difference (mV)
No Load	open	3.08	31.23166667	4.17	31.277029	45.36233333
Full Load	100	2.96	30.01484848	3.79	29.953223	-61.62548485
Mid Range	1k	3.06	31.02886364	4.12	31.102844	73.98036364

Figure 2.5: Integrated test of voltage transducer



(a) VAC Input and DC output (b) Voltage transducer AC output

Figure 2.6: Oscilloscope measurement of analogue DC output and AC characteristics of the Voltage Transducer for the Mid-range load

Chapter 3

Current peak transducer

3.1 Theory and related work

The current transducer design is quite similar to that of the voltage transducer, due to the nature of transforming an AC signal into a DC representation. Once again, the precision rectifier, equation 2.1, and a precision diode will be used.

A simple, non-inverting amplifier configuration, the gain is calculated as follows:

$$A_v = (1 + \frac{Rf}{Rg}) \tag{3.1}$$

For such configurations, the maximum common-mode voltage is unlikely to be exceeded due to the fact that $V_{in-max} = V_{OH} \frac{Rg}{Rf+Rg}$.

TL081 op-amps have a better Common-Mode Rejection Ratio (CMRR) than that of a TLC2272 [5, p.7] [4, p.7]. Therefore, the TL081 makes for a better small-signal amplifier [6].

3.2 Design

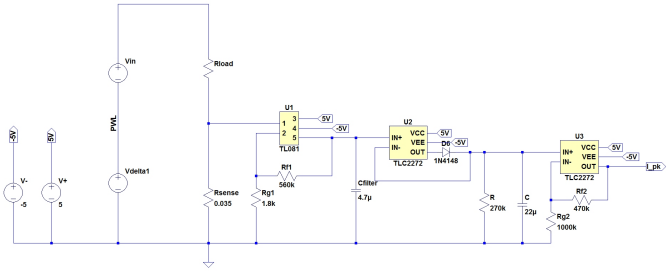


Figure 3.1: Current Transducer circuit

30 mΩ and 5 mΩ current-sense resistors are connected in series to maximize the small voltage which is pre-amplified by the TL081 op-amp. For a maximum current of 285 mA ($V_{Rsense} = 9.975\,\text{mV}$), the voltage gain is required to comply with the TL081 minimum high-level output voltage of 3.5 V [5, p.9]. A gain of 312 is set by choosing Rf1 = 560 kΩ and Rg1 = 560 kΩ.

The pre-amplified voltage is half-wave rectified. The precision diode ensures negligible voltage drop. The rectified signal ripple must meet the 1 mA accuracy requirement and be able to detect a 10 mA change in current for currents over 100 mA within one second.

The maximum value of τ can be determined such that a 285 mA drops by 1 mA over a 20 ms period:

$\tau_{min} = \frac{-0.02}{\ln(\frac{285-1}{285})} = 5.69$

Similarly, for a minimum current of 100 mA, to detect a 10 mA decrease within 1 s, the maximum value of τ can be calculated:

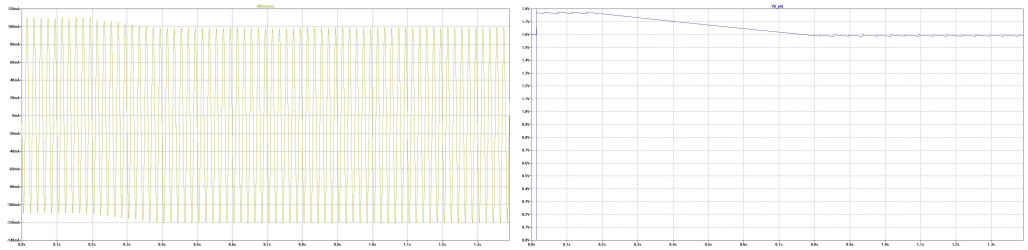
$$\tau_{max} = \frac{-1}{\ln(\frac{100-10}{100})} = 9.49$$

Therefore, a resistor of 270 kΩ and a capacitor of 22 µF results in an acceptable $\tau = RC = 5.94$.

The rectified signal is post-amplified by a non-inverting amplifier such that 285 mA through the sensing resistor will output closer to the 5 V limit. Hence, for a configuration of Rf2 = 470 kΩ and Rg2 = 1 MΩ, the gain is 1.47 and an input of 285 mA should be converted to 4.58 V.

3.3 Simulation

An LTSpice simulation of the circuit in Figure 3.1 indicates that the current transducer satisfies the specifications. The input voltage is chosen to demonstrate that the chosen RC constant allows a 10 mA change to be detected for currents above 100 mA.



(a) Decreasing load current (b) Current transducer DC output

Figure 3.2: Current transducer LTSpice results

3.4 Measurements

As with the voltage transducer, emulated tests where performed to determine the functionality of the design and compensate for inaccuracies. Resistors were used to divide the voltage applied to the system. The selected and measured function generator outputs differed considerably due to noise.

Emulated Input (mApk)	Signal Generator Selected (mVpk)	Signal Generator Selected (mVpk-pk)	Signal generator Measured (V+pk)	Analogue output (Vdc)	Deduced input (mApk)	Difference (mA)
0	0	0	0.264	-0.089	-5.507270835	-5.507270835
50	1.75	3.5	0.009	0.833	51.54557984	1.545579839
100	3.5	7	0.012	1.64	101.482294	1.48229404
101	3.535	7.07	0.012	1.65	102.1010885	1.101088516
102	3.57	7.14	0.012	1.67	103.3386775	1.338677467
200	7	14	0.0152	3.2	198.0142323	-1.985767727
285	9.975	19.95	0.0184	4.56	282.170281	-2.829719011

Figure 3.3: Emulated Voltage Transducer tests

Due to the difficulties of emulating the load current, the linear function of the deduced input is more reliable for calculations. The linear function is given in Figure 3.4.

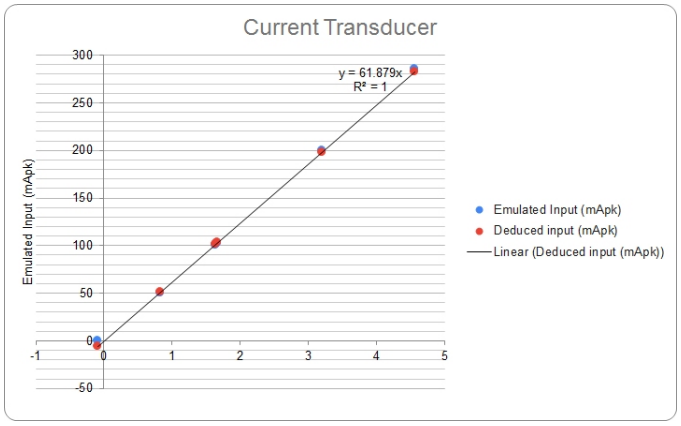
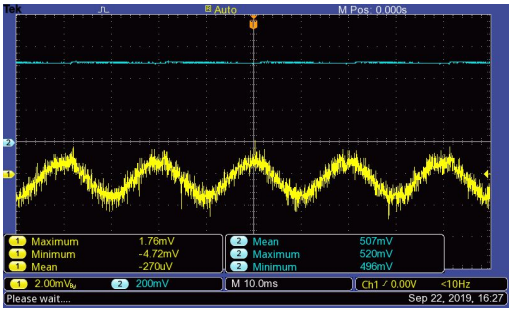


Figure 3.4: Current Transducer: Linear function of analogue output vs. load current

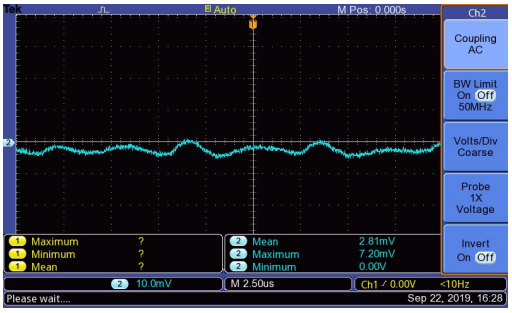
By applying the linear function in Figure 3.4 for the integrated tests, a marginally accurate calculation of the load current is achievable. The voltage drop over the sense resistors is indeterminate so the best I could do to determine the actual current in the system was to divide the measured input voltage by the load impedance.

Measurement	Load R1	Load R2	Measured input (Vpk)	Actual input (mApk)	Analogue output (Vdc)	Deduced input (mApk)	Difference (mA)
No Load	open	-	0.02	0	0.003	0.185637	0.185637
Full Load	100	-	0.011	281.9	4.57	282.78703	0.88703
Mid Range	1k	-	0.0013	31.2	0.506	31.310774	0.110774
Mid + δ	1k	24k	0.0016	32.3	0.519	32.115201	-0.184799
Mid + 2δ	1k	12k	0.0019	33.6	0.555	34.342845	0.742845

Figure 3.5: Integrated test of the current transducer



(a) AC coupled current Input and DC output



(b) Current transducer AC output

Figure 3.6: Oscilloscope measurement of analogue DC output and AC characteristics of the Current Transducer for the Mid-range load

Chapter 4

Phase shift transducer

4.1 Theory and related work

This design converts a PWM signal into a DC signal using a first-order low-pass passive filter. A PWM signal can be described as a Fourier series of sinusoidal signals. Essentially, a very small corner frequency is selected so that only the 0 Hz portion remains.

A series capacitor and parallel resistor which acts as a high-pass filter uses the inverse method to enable accurate phase detection.

The corner frequency of these filters can be determined with Equation 4.1.

$$f_c = \frac{1}{2\pi RC} \tag{4.1}$$

4.2 Design

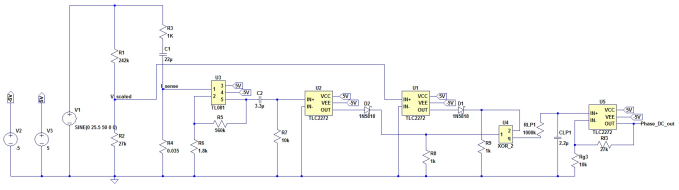


Figure 4.1: Phase Transducer circuit

The transducer converts the voltage and amplified current sinusoidal signals into square waves using a comparator configuration referenced to ground such that it

acts as a 'zero-crossing detector'. The TLC2272 op-amp was used for the comparators due to its high maximum common-mode voltage and large minimum high-level output voltage.

Due to intrinsic offsets in the amplified current signal, a high pass filter is used before the current comparator such that the corner frequency is much smaller than 50 Hz. Hence, for R = 10 kΩ and C = 3.3 µF: $f_c = 4.8Hz$.

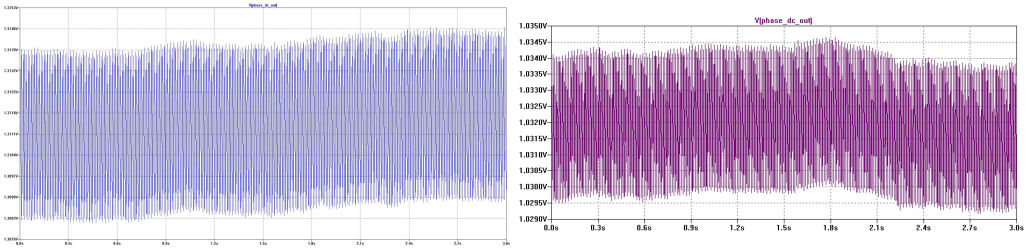
The comparator outputs are passed through an XOR gate to obtain a PWM which represents the phase shift between the voltage and current. due to the fact that XOR gate minimum input voltage is −0.5 V [7, p.4], the negative portion of the comparator outputs is blocked by diodes. Schottky diodes are used for the benefit of a low forward-voltage.

The PWM signal is filtered by the low-pass filter such that the lowest frequency components remain. For R = 1 MΩ and C = 2.2 µF: $f_c = 0.07Hz$

For a PWM of 0 V to 5 V, the maximum phase shift of 45° results in a DC value of 1.25 V. For better resolution, a gain of 4 is desired. The DC voltage is amplified by a non-inverting TLC2272 amplifier. According to Equation 3.1, by selecting resistors Rf3 = 27 kΩ and Rg3 = 10 kΩ a gain of 3.7 is induced.

4.3 Simulation

LTSpice simulations of the deigned circuit produce a satisfactory output, albeit noisy. The cause of the noise could not be determined and does not appear in the practical implementation.



(a) Mid: 1 kΩ and 22 µF load

(b) Mid + δ: 1 kΩ and 33 µF load

Figure 4.2: LTSpice simulations results

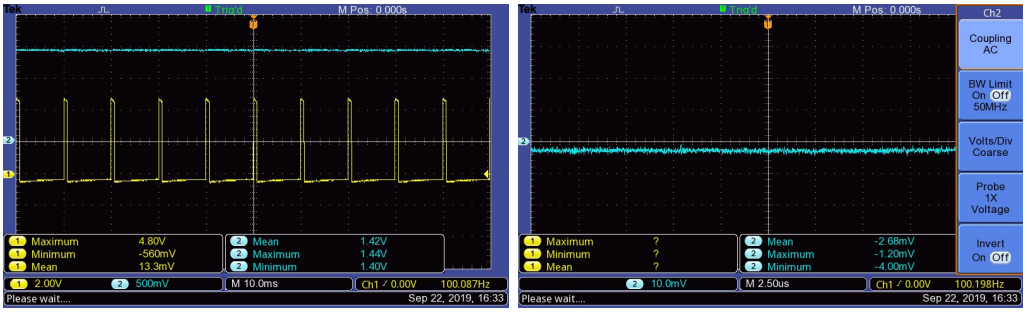
4.4 Measurements

For 1° accuracy, the difference between deduced the deduced and actual input may be no more than $\frac{1^\circ}{360^\circ} 20\,\text{ms} = 55.56\,\mu\text{s}$. Therefore, calculating the input phase shift

based on the circuit design proves sufficient for the integrated tests.

Measurement	Load R	Load C	Measured Shift (ms)	Analogue output (Vd	Deduced input ms	Difference (ms)
No Load	1k	-	0.312	0.508	0.274594595	-0.037405405
Full Load	1k	3.3	1.82	3.32	1.794594595	-0.025405405
Mid Range	1k	22	0.76	1.41	0.762162162	0.002162162
Mid + δ	1k	33	0.61	1.08	0.583783784	-0.026216216
Mid + 2δ	1k	47	0.496	0.937	0.506486486	0.010486486

Figure 4.3: Integrated test of the phase shift transducer



(a) PWM and DC output (b) Phase transducer AC output

Figure 4.4: Oscilloscope measurement of analogue DC output and AC characteristics of the Phase Transducer for the Mid-range load

Chapter 5

System tests

The circuit in Figure 5.1 is testament to the arduous task of building, testing, and tweaking to meet the requirements.

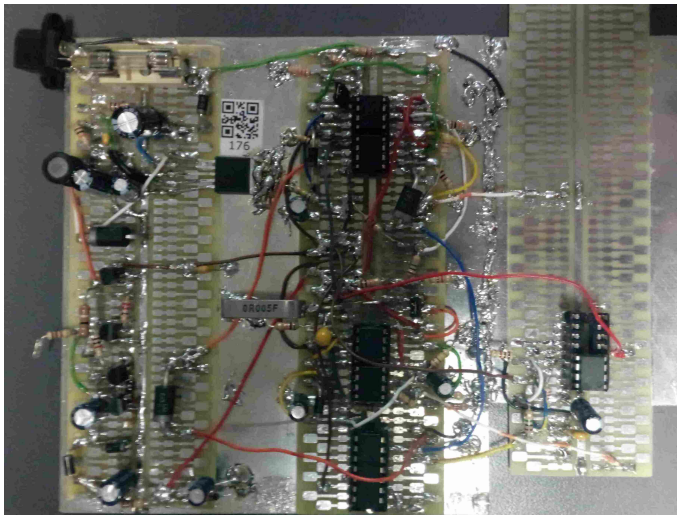
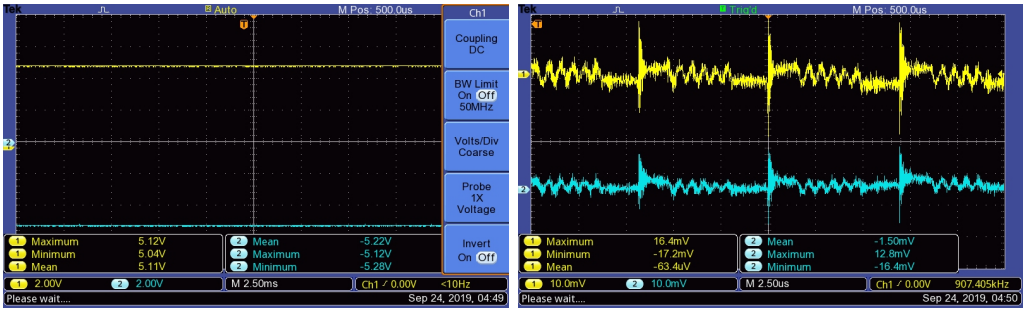


Figure 5.1: Integrated test of the current transducer



(a) DC rails (b) AC rails

Figure 5.2: Oscilloscope measurements of rails at Full Load Condition

References

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[6] Gerard Fonte: How to choose an operational amplifier. 2008.
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Appendix A: GitHub Activity Heatmap