NCTU-EE IC LAB – Fall 2023

Final Project check list

Self-verify APR result

Download your tar file by 02_check to the workstation.
Create a new directory, enter the directory and decompress the tar file.
Enter the decompressed directory.
Rename the following files (you can use ***mv*** comment):
CHIP_iclabXXX.inn → CHIP.inn
CHIP_iclabXXX.io → CHIP.io
CHIP_iclabXXX.sdc → CHIP.sdc
CHIP_iclabXXX.sdf → CHIP.sdf
CHIP_iclabXXX.v → CHIP.v
CHIP_iclabXXX.inn.dat → CHIP.inn.dat

If you did not tar you file on workstation, and any error occured during decompression or restoring you innovus files you will fail the demo!

1. Make sure your CHIP.sdc is written correctly: **period**, **waveform** parameter, **input delay** and **output delay**. **Waveform** parameter, **input delay** and **output delay** should be half of the **period**.
2. Invoke innonus and restore CHIP.inn
3. Explore the core size and die size, also verify if the core to IO boundary should be larger than 100.
4. Verify the floorplan and powerplan constraints:
   a. Power ring: wire group, interleaving, and at least 4 pairs, width 9.
   b. Stripes: distance between 2 sets should be less than 200, and width 4.
5. SI Timing analysis with non-negative slacks, 0 DRVs, core filler added.
6. Verifying Geometry and Connectivity after adding core filler cells.
7. Latency cycles in post simulation should be the same as gate level simulation.
8. SRAMs must be inside core region.