CHALMERS
Department of Computer Science and Engineering

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DAT094
Introduction to Electronic System Design
Files in Lab4 MAC_gen_min_12_101

Lab 4

MAC_gen_min_12_101

A FIR filter using GENERATE to create the design. 12 bits signal, 12 bits coefficients, 101 taps

Files

`FIR_tap.vhdl` – project component (from lab 2)

`MAC_gen_min_12_101.vhdl` – the filter design

`MAC_gen_min_12_101_tb3.vhdl` – do file for the design

`MAC_gen_min_12_101_tb3_do` – do file to run the test bench

`MAC_gen_min_12_101_package.vhdl` – gives coefficients for the filter and input signals and expected results for the simulation (from packages)

`vec2str_package.vhdl` – converts STD_LOGIC and STD_LOGIC_VECTOR to text for printing (from packages)