CHALMERS
Department of Computer Science and Engineering

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DAT094
Introduction to Electronic System Design
Files in Lab4
total_system_MAC_loop_min_12_17

Lab 4

Total_system_MAC_loop_min_12_17

A total filter system with ADC and DAC using MAC_gen_min_12_17 FIR filter with 12 bits signal, 12 bits coefficients, 17 taps. A lowpass pass filter with a cutoff frequency of 12 kHz

Files

`MAC_loop_min_full_12_17.vhdl` – the total design including ADC and DAC

`MAC_loop_min_12_17.vhdl` – the filter design (from lab 4/MAC_loop_min_12_17)

`convert_data_format` – converts between signed and unsigned vectors (from lab 1)

`sample_clock` – generats the sampling clock signal (from Common files)

`SPI_clock` – sets the clock frequency for the SPI communication (from Common files)

`SPI_AD` – reads data from the ADC using SPI interface (from Common files)

`SPI_DA` – sends output data to the DAC (from Common files)

`MAC_loop_min_12_17_package.vhdl` – gives coefficients for the filter and input signals and expected results for the simulation (from packages)

`vec2str_package.vhdl` – converts STD_LOGIC and STD_LOGIC_VECTOR to text for printing (from packages)

`system_frequencies_package.vhdl` – sets the system frequency, the sample frequency and the SPI clock frequency (from packages)