CHALMERS
Department of Computer Science and Engineering

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DAT094
Introduction to Electronic System Design
Files in Lab4 MAC_loop_min_12_17

Lab 4

MAC_loop_min_12_17

A FIR filter using FOR…LOOP to create the design. 12 bits signal, 12 bits coefficients, 17 taps

Files

`MAC_loop_min_12_17.vhdl` – the filter design

`MAC_loop_min_12_17.do`– do file for the filter design

`MAC_loop_min_12_17_tb3.vhdl` - test bench for the design

`MAC_loop_min_12_17_tb3_do` – do file to run the test bench

`MAC_loop_min_12_17_package.vhdl` – gives coefficients for the filter and input signals and expected results for the simulation (from packeges)

`vec2str_package.vhdl` – converts STD_LOGIC and STD_LOGIC_VECTOR to text for printing (from packages)