8.6 Register Maps

This section describes the control registers for the device in detail. All registers are eight bits in width and are allocated to the device configuration and programmable coefficients settings. These registers are mapped internally using a page scheme that can be controlled using either I^2C or SPI communication to the device. Each page contains 128 bytes of registers. All device configuration registers are stored in page 0, which is the default page setting at power up (and after a software reset). Page 1 consists of the live status registers and input diagnostic SAR data for advanced diagnostic purposes. All programmable coefficient registers are located in page 2, page 3, and page 4. The device current page can be switched to a new desired page by using the PAGE[7:0] bits located in register 0 of every page.

Do not read from or write to reserved pages or reserved registers. Write only default values for the reserved bits in the valid registers.

The procedure for register access across pages is:

- Select page N (write data *N* to register 0 regardless of the current page number)
- Read or write data from or to valid registers in page N
- Select the new page M (write data *M* to register 0 regardless of the current page number)
- Read or write data from or to valid registers in page M
- Repeat as needed

8.6.1 Device Configuration Registers

This section describes the device configuration registers for page 0 and page 1.

8.6.1.1 Register Summary Table Page=0x00

ADDRESS	REGISTER	DESCRIPTION	SECTION
0x00	PAGE_CFG	Device page register	PAGE_CFG Register (P0_R0)
0x01	SW_RESET	Software reset register	SW_RESET Register (P0_R1)
0x02	SLEEP_CFG	Sleep mode register	SLEEP_CFG Register (P0_R2)
0x05	SHDN_CFG	Shutdown configuration register	SHDN_CFG Register (P0_R5)
0x07	ASI_CFG0	ASI configuration register 0	ASI_CFG0 Register (P0_R7)
0x08	ASI_CFG1	ASI configuration register 1	ASI_CFG1 Register (P0_R8)
0x09	ASI_CFG2	ASI configuration register 2	ASI_CFG2 Register (P0_R9)
0x0B	ASI_CH1	Channel 1 ASI slot configuration register	ASI_CH1 Register (P0_R11)
0x0C	ASI_CH2	Channel 2 ASI slot configuration register	ASI_CH2 Register (P0_R12)
0x0D	ASI_CH3	Channel 3 ASI slot configuration register	ASI_CH3 Register (P0_R13)
0x0E	ASI_CH4	Channel 4 ASI slot configuration register	ASI_CH4 Register (P0_R14)
0x0F	ASI_CH5	Channel 5 ASI slot configuration register	ASI_CH5 Register (P0_R15)
0x10	ASI_CH6	Channel 6 ASI slot configuration register	ASI_CH6 Register (P0_R16)
0x13	MST_CFG0	ASI master mode configuration register 0	MST_CFG0 Register (P0_R19)
0x14	MST_CFG1	ASI master mode configuration register 1	MST_CFG1 Register (P0_R20)
0x15	ASI_STS	ASI bus clock monitor status register	ASI_STS Register (P0_R21)
0x16	CLK_SRC	Clock source configuration register	CLK_SRC Register (P0_R22)
0x21	GPIO_CFG0	GPIO configuration register 0	GPIO_CFG0 Register (P0_R33)
0x22	GPIO_CFG1	GPIO configuration register 1	GPIO_CFG1 Register (P0_R34)
0x23	GPIO_CFG2	GPIO configuration register 2	GPIO_CFG2 Register (P0_R35)
0x24	GPI_CFG0	GPI configuration register 0	GPI_CFG0 Register (P0_R36)
0x25	GPI_CFG1	GPI configuration register 1	GPI_CFG1 Register (P0_R37)
0x26	GPIO_VAL	GPIO output value register	GPIO_VAL Register (P0_R38)
0x27	GPIO_MON	GPIO monitor value register	GPIO_MON Register (P0_R39)
0x28	INT_CFG	Interrupt configuration register	INT_CFG Register (P0_R40)
0x29	INT_MASK0	Interrupt mask register 0	INT_MASK0 Register (P0_R41)
0x2A	INT_MASK1	Interrupt mask register 1	INT_MASK1 Register (P0_R42)
0x2B	INT_MASK2	Interrupt mask register 2	INT_MASK2 Register (P0_R43)
0x2C	INT_LTCH0	Latched interrupt readback register 0	INT_LTCH0 Register (P0_R44)

Register Maps (continued)

0x2D	CHx_LTCH	Channel diagnostic summary latched status register	CHx_LTCH Register (P0_R45)
0x2E	CH1_LTCH	Channel 1 diagnostic latched status register	CH1_LTCH Register (P0_R46)
0x2F	CH2_LTCH	Channel 2 diagnostic latched status register	CH2_LTCH Register (P0_R47)
0x30	CH3_LTCH	Channel 3 diagnostic latched status register	CH3_LTCH Register (P0_R48)
0x31	CH4_LTCH	Channel 4 diagnostic latched status register	CH4_LTCH Register (P0_R49)
0x32	CH5_LTCH	Channel 5 diagnostic latched status register	CH5_LTCH Register (P0_R50)
0x33	CH6_LTCH	Channel 6 diagnostic latched status register	CH6_LTCH Register (P0_R51)
0x34	INT_MASK3	Interrupt mask register 3	INT_MASK3 Register (P0_R52)
0x35	INT_LTCH1	Latched interrupt readback register 1	INT_LTCH1 Register (P0_R53)
0x36	INT_LTCH2	Latched interrupt readback register 2	INT_LTCH2 Register (P0_R54)
0x37	INT_LTCH3	Latched interrupt readback register 3	INT_LTCH3 Register (P0_R55)
0x38	MBDIAG_CFG0	MICBIAS diagnostic register 0	MBDIAG_CFG0 Register (P0_R56)
0x39	MBDIAG_CFG1	MICBIAS diagnostic register 1	MBDIAG_CFG1 Register (P0_R57)
0x3A	MBDIAG_CFG2	MICBIAS diagnostic register 2	MBDIAG_CFG2 Register (P0_R58)
0x3B	BIAS_CFG	Bias configuration register	BIAS_CFG Register (P0_R59)
0x3C	CH1_CFG0	Channel 1 configuration register 0	CH1_CFG0 Register (P0_R60)
0x3D	CH1_CFG1	Channel 1 configuration register 1	CH1_CFG1 Register (P0_R61)
0x3E	CH1_CFG2	Channel 1 configuration register 2	CH1_CFG2 Register (P0_R62)
0x3F	CH1_CFG3	Channel 1 configuration register 3	CH1_CFG3 Register (P0_R63)
0x40	CH1_CFG4	Channel 1 configuration register 4	CH1_CFG4 Register (P0_R64)
0x41	CH2_CFG0	Channel 2 configuration register 0	CH2_CFG0 Register (P0_R65)
0x42	CH2_CFG1	Channel 2 configuration register 1	CH2_CFG1 Register (P0_R66)
0x43	CH2_CFG2	Channel 2 configuration register 2	CH2_CFG2 Register (P0_R67)
0x44	CH2_CFG3	Channel 2 configuration register 3	CH2_CFG3 Register (P0_R68)
0x45	CH2_CFG4	Channel 2 configuration register 4	CH2_CFG4 Register (P0_R69)
0x46	CH3_CFG0	Channel 3 configuration register 0	CH3_CFG0 Register (P0_R70)
0x47	CH3_CFG1	Channel 3 configuration register 1	CH3_CFG1 Register (P0_R71)
0x48	CH3_CFG2	Channel 3 configuration register 2	CH3_CFG2 Register (P0_R72)
0x49	CH3_CFG3	Channel 3 configuration register 3	CH3_CFG3 Register (P0_R73)
0x4A	CH3_CFG4	Channel 3 configuration register 4	CH3_CFG4 Register (P0_R74)
0x4B	CH4_CFG0	Channel 4 configuration register 0	CH4_CFG0 Register (P0_R75)
0x4C	CH4_CFG1	Channel 4 configuration register 1	CH4_CFG1 Register (P0_R76)
0x4D	CH4_CFG2	Channel 4 configuration register 2	CH4_CFG2 Register (P0_R77)
0x4E	CH4_CFG3	Channel 4 configuration register 3	CH4_CFG3 Register (P0_R78)
0x4F	CH4_CFG4	Channel 4 configuration register 4	CH4_CFG4 Register (P0_R79)
0x50	CH5_CFG0	Channel 5 configuration register 0	CH5_CFG0 Register (P0_R80)
0x51	CH5_CFG1	Channel 5 configuration register 1	CH5_CFG1 Register (P0_R81)
0x52	CH5_CFG2	Channel 5 configuration register 2	CH5_CFG2 Register (P0_R82)
0x53	CH5_CFG3	Channel 5 configuration register 3	CH5_CFG3 Register (P0_R83)
0x54	CH5_CFG4	Channel 5 configuration register 4	CH5_CFG4 Register (P0_R84)
0x55	CH6_CFG0	Channel 6 configuration register 0	CH6_CFG0 Register (P0_R85)
0x56	CH6_CFG1	Channel 6 configuration register 1	CH6_CFG1 Register (P0_R86)
0x57	CH6_CFG2	Channel 6 configuration register 2	CH6_CFG2 Register (P0_R87)
0x58	CH6_CFG3	Channel 6 configuration register 3	CH6_CFG3 Register (P0_R88)
0x59	CH6_CFG4	Channel 6 configuration register 4	CH6_CFG4 Register (P0_R89)
0x64	DIAG_CFG0	Input diagnostic configuration register 0	DIAG_CFG0 Register (P0_R100)
0x65	DIAG_CFG1	Input diagnostic configuration register 1	DIAG_CFG1 Register (P0_R101)
0x66	DIAG_CFG2	Input diagnostic configuration register 2	DIAG_CFG2 Register (P0_R102)
0x67	DIAG_CFG3	Input diagnostic configuration register 3	DIAG_CFG3 Register (P0_R103)
0x68	DIAG_CFG4	Input diagnostic configuration register 4	DIAG_CFG4 Register (P0_R104)
0x6B	DSP_CFG0	DSP configuration register 0	DSP_CFG0 Register (P0_R107)
0x6C	DSP_CFG1	DSP configuration register 1	DSP_CFG1 Register (P0_R108)

Register Maps (continued)

0x70	AGC_CFG0	AGC configuration register 0	AGC_CFG0 Register (P0_R112)
0x73	IN_CH_EN	Input channel enable configuration register	IN_CH_EN Register (P0_R115)
0x74	ASI_OUT_CH_EN	ASI output channel enable configuration register	ASI_OUT_CH_EN Register (P0_R116)
0x75	PWR_CFG	Power up configuration register	PWR_CFG Register (P0_R117)
0x76	DEV_STS0	Device status value register 0	DEV_STS0 Register (P0_R118)
0x77	DEV_STS1	Device status value register 1	DEV_STS1 Register (P0_R119)
0x7E	I2C_CKSUM	I^2C checksum register	I2C_CKSUM Register (P0_R126)

8.6.1.2 Register Summary Table Page=0x01

ADDRESS	REGISTER	DESCRIPTION	SECTION
0x00	PAGE_CFG	Device page register	PAGE_CFG Register (P1_R0)
0x16	MBIAS_LOAD	MICBIAS internal load sink configuration register	MBIAS_LOAD Register (P1_R22)
0x2C	INT_LIVE0	Live interrupt readback register 0	INT_LIVE0 Register (P1_R44)
0x2D	CHx_LIVE	Channel diagnostic summary live status register	CHx_LIVE Register (P1_R45)
0x2E	CH1_LIVE	Channel 1 diagnostic live status register	CH1_LIVE Register (P1_R46)
0x2F	CH2_LIVE	Channel 2 diagnostic live status register	CH2_LIVE Register (P1_R47)
0x30	CH3_LIVE	Channel 3 diagnostic live status register	CH3_LIVE Register (P1_R48)
0x31	CH4_LIVE	Channel 4 diagnostic live status register	CH4_LIVE Register (P1_R49)
0x32	CH5_LIVE	Channel 5 diagnostic live status register	CH5_LIVE Register (P1_R50)
0x33	CH6_LIVE	Channel 6 diagnostic live status register	CH6_LIVE Register (P1_R51)
0x35	INT_LIVE1	Live interrupt readback register 1	INT_LIVE1 Register (P1_R53)
0x37	INT_LIVE3	Live interrupt readback register 3	INT_LIVE3 Register (P1_R55)
0x55	MBIAS_OV_CFG	MICBIAS overvoltage threshold register	MBIAS_OV_CFG Register (P1_R85)
0x59	DIAGDATA_CFG	Diagnostic data configuration register	DIAGDATA_CFG Register (P1_R89)
0x5A	DIAG_MON_MSB_VBAT	Diagnostic VBAT_IN data MSB byte register	DIAG_MON_MSB_VBAT Register (P1_R90)
0x5B	DIAG_MON_LSB_VBAT	Diagnostic VBAT_IN data LSB nibble register	DIAG_MON_LSB_VBAT Register (P1_R91)
0x5C	DIAG_MON_MSB_MBIAS	Diagnostic MICBIAS data MSB byte register	DIAG_MON_MSB_MBIAS Register (P1_R92)
0x5D	DIAG_MON_LSB_MBIAS	Diagnostic MICBIAS data LSB nibble register	DIAG_MON_LSB_MBIAS Register (P1_R93)
0x5E	DIAG_MON_MSB_IN1P	Diagnostic IN1P data MSB byte register	DIAG_MON_MSB_IN1P Register (P1_R94)
0x5F	DIAG_MON_LSB_IN1P	Diagnostic IN1P data LSB nibble register	DIAG_MON_LSB_IN1P Register (P1_R95)
0x60	DIAG_MON_MSB_IN1M	Diagnostic IN1M data MSB byte register	DIAG_MON_MSB_IN1M Register (P1_R96)
0x61	DIAG_MON_LSB_IN1M	Diagnostic IN1M data LSB nibble register	DIAG_MON_LSB_IN1M Register (P1_R97)
0x62	DIAG_MON_MSB_IN2P	Diagnostic IN2P data MSB byte register	DIAG_MON_MSB_IN2P Register (P1_R98)
0x63	DIAG_MON_LSB_IN2P	Diagnostic IN2P data LSB nibble register	DIAG_MON_LSB_IN2P Register (P1_R99)
0x64	DIAG_MON_MSB_IN2M	Diagnostic IN2M data MSB byte register	DIAG_MON_MSB_IN2M Register (P1_R100)
0x65	DIAG_MON_LSB_IN2M	Diagnostic IN2M data LSB nibble register	DIAG_MON_LSB_IN2M Register (P1_R101)
0x66	DIAG_MON_MSB_IN3P	Diagnostic IN3P data MSB byte register	DIAG_MON_MSB_IN3P Register (P1_R102)
0x67	DIAG_MON_LSB_IN3P	Diagnostic IN3P data LSB nibble register	DIAG_MON_LSB_IN3P Register (P1_R103)
0x68	DIAG_MON_MSB_IN3M	Diagnostic IN3M data MSB byte register	DIAG_MON_MSB_IN3M Register (P1_R104)
0x69	DIAG_MON_LSB_IN3M	Diagnostic IN3M data LSB nibble register	DIAG_MON_LSB_IN3M Register (P1_R105)
0x6A	DIAG_MON_MSB_IN4P	Diagnostic IN4P data MSB byte register	DIAG_MON_MSB_IN4P Register (P1_R106)
0x6B	DIAG_MON_LSB_IN4P	Diagnostic IN4P data LSB nibble register	DIAG_MON_LSB_IN4P Register (P1_R107)
0x6C	DIAG_MON_MSB_IN4M	Diagnostic IN4M data MSB byte register	DIAG_MON_MSB_IN4M Register (P1_R108)
0x6D	DIAG_MON_LSB_IN4M	Diagnostic IN4M data LSB nibble register	DIAG_MON_LSB_IN4M Register (P1_R109)
0x6E	DIAG_MON_MSB_IN5P	Diagnostic IN5P data MSB byte register	DIAG_MON_MSB_IN5P Register (P1_R110)
0x6F	DIAG_MON_LSB_IN5P	Diagnostic IN5P data LSB nibble register	DIAG_MON_LSB_IN5P Register (P1_R111)
0x70	DIAG_MON_MSB_IN5M	Diagnostic IN5M data MSB byte register	DIAG_MON_MSB_IN5M Register (P1_R112)
0x71	DIAG_MON_LSB_IN5M	Diagnostic IN5M data LSB nibble register	DIAG_MON_LSB_IN5M Register (P1_R113)
0x72	DIAG_MON_MSB_IN6P	Diagnostic IN6P data MSB byte register	DIAG_MON_MSB_IN6P Register (P1_R114)
0x73	DIAG_MON_LSB_IN6P	Diagnostic IN6P data LSB nibble register	DIAG_MON_LSB_IN6P Register (P1_R115)
0x74	DIAG_MON_MSB_IN6M	Diagnostic IN6M data MSB byte register	DIAG_MON_MSB_IN6M Register (P1_R116)

0x75	DIAG_MON_LSB_IN6M	Diagnostic IN6M data LSB nibble register	DIAG_MON_LSB_IN6M Register (P1_R117)
0x76	DIAG_MON_MSB_TEMP	Diagnostic temperature data MSB byte register	DIAG_MON_MSB_TEMP Register (P1_R118)
0x77	DIAG_MON_LSB_TEMP	Diagnostic temperature data LSB nibble register	DIAG_MON_LSB_TEMP Register (P1_R119)
0x78	DIAG_MON_MSB_LOAD	Diagnostic MICBIAS load current data MSB byte register	DIAG_MON_MSB_LOAD Register (P1_R120)
0x79	DIAG_MON_LSB_LOAD	Diagnostic MICBIAS load current data LSB nibble register	DIAG_MON_LSB_LOAD Register (P1_R121)

Table 51 lists the access codes used for the PCM6xx0-Q1 registers.

Table 51. PCM6xx0-Q1 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-W	R/W	Read or write
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.6.1.3 Register Description: Page = 0x00

8.6.1.3.1 PAGE_CFG Register (page = 0x00, address = 0x00) [reset = 0h]

The device memory map is divided into pages. This register sets the page.

Figure 96. PAGE_CFG Register

7	6	5	4	3	2	1	0
PAGE[7:0]							
R/W-0h							

Table 52. PAGE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PAGE[7:0]	R/W	0h	These bits set the device page. 0d = Page 0 1d = Page 1 ... 255d = Page 255

8.6.1.3.2 SW_RESET Register (page = 0x00, address = 0x01) [reset = 0h]

This register is the software reset register. Asserting a software reset places all register values in their default power-on-reset (POR) state.

Figure 97. SW_RESET Register

7	6	5	4	3	2	1	0
Reserved							SW_RESET
R-0h							R/W-0h

Table 53. SW_RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Reserved	R	0h	Reserved
0	SW_RESET	R/W	0h	Software reset. This bit is self-clearing. 0d = Do not reset 1d = Reset

8.6.1.3.3 SLEEP_CFG Register (page = 0x00, address = 0x02) [reset = 0h]

This register configures the regulator, VREF quick charge, I²C broadcast and sleep mode.

Figure 98. SLEEP_CFG Register

7	6	5	4	3	2	1	0
Reserved	Reserved		VREF_QCHG[1:0]		I2C_BRDCAST_EN	Reserved	SLEEP_ENZ
RW-0h	RW-0h		RW-0h		RW-0h	R-0h	RW-0h

Table 54. SLEEP_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	RW	0h	Reserved
6-5	Reserved	RW	0h	Reserved
4-3	VREF_QCHG[1:0]	RW	0h	The duration of the quick-charge for the VREF external capacitor is set using an internal series impedance of 200 Ω. 0d = VREF quick-charge duration of 3.5 ms (typical) 1d = VREF quick-charge duration of 10 ms (typical) 2d = VREF quick-charge duration of 50 ms (typical) 3d = VREF quick-charge duration of 100 ms (typical)
2	I2C_BRDCAST_EN	RW	0h	I²C broadcast addressing setting. 0d = I²C broadcast mode disabled; the I²C slave address is determined based on the ADDR pins 1d = I²C broadcast mode enabled; the I²C slave address is fixed at 1001 100
1	Reserved	R	0h	Reserved
0	SLEEP_ENZ	RW	0h	Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode

8.6.1.3.4 SHDN_CFG Register (page = 0x00, address = 0x05) [reset = 5h]

This register configures the device shutdown

Figure 99. SHDN_CFG Register

7	6	5	4	3	2	1	0
Reserved				SHDNZ_CFG[1:0]		DREG_KA_TIME[1:0]	
R-0h				RW-1h		RW-1h	

Table 55. SHDN_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	R	0h	Reserved
3-2	SHDNZ_CFG[1:0]	RW	1h	Shutdown configuration. 0d = DREG is powered down immediately after SHDNZ asserts 1d = DREG remains active to enable a clean shut down until a time-out is reached; after the time-out period, DREG is forced to power off 2d = DREG remains active until the device cleanly shuts down 3d = Reserved
1-0	DREG_KA_TIME[1:0]	RW	1h	These bits set how long DREG remains active after SHDNZ asserts. 0d = DREG remains active for 30 ms (typical) 1d = DREG remains active for 25 ms (typical) 2d = DREG remains active for 10 ms (typical) 3d = DREG remains active for 5 ms (typical)

8.6.1.3.5 ASI_CFG0 Register (page = 0x00, address = 0x07) [reset = 30h]

This register is the ASI configuration register 0.

Figure 100. ASI_CFG0 Register

7	6	5	4	3	2	1	0
ASI_FORMAT[1:0]		ASI_WLEN[1:0]		FSYNC_POL	BCLK_POL	TX_EDGE	TX_FILL
RW-0h		RW-3h		RW-0h	RW-0h	RW-0h	RW-0h

Table 56. ASI_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	ASI_FORMAT[1:0]	RW	0h	ASI protocol format. 0d = TDM mode 1d = I^2S mode 2d = LJ (left-justified) mode 3d = Reserved
5-4	ASI_WLEN[1:0]	RW	3h	ASI word or slot length. 0d = 16 bits 1d = 20 bits 2d = 24 bits 3d = 32 bits
3	FSYNC_POL	RW	0h	ASI FSYNC polarity. 0d = Default polarity as per standard protocol 1d = Inverted polarity with respect to standard protocol
2	BCLK_POL	RW	0h	ASI BCLK polarity. 0d = Default polarity as per standard protocol 1d = Inverted polarity with respect to standard protocol
1	TX_EDGE	RW	0h	ASI data output (on the primary and secondary data pin) transmit edge. 0d = Default edge as per the protocol configuration setting in bit 2 (BCLK_POL) 1d = Inverted following edge (half cycle delay) with respect to the default edge setting
0	TX_FILL	RW	0h	ASI data output (on the primary and secondary data pin) for any unused cycles 0d = Always transmit 0 for unused cycles 1d = Always use Hi-Z for unused cycles

8.6.1.3.6 ASI_CFG1 Register (page = 0x00, address = 0x08) [reset = 0h]

This register is the ASI configuration register 1.

Figure 101. ASI_CFG1 Register

7	6	5	4	3	2	1	0
TX_LSB	TX_KEEPER[1:0]		TX_OFFSET[4:0]				
RW-0h	RW-0h		RW-0h				

Table 57. ASI_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TX_LSB	RW	0h	ASI data output (on the primary and secondary data pin) for LSB transmissions. 0d = Transmit the LSB for a full cycle 1d = Transmit the LSB for the first half cycle and Hi-Z for the second half cycle
6-5	TX_KEEPER[1:0]	RW	0h	ASI data output (on the primary and secondary data pin) bus keeper. 0d = Bus keeper is always disabled 1d = Bus keeper is always enabled 2d = Bus keeper is enabled during LSB transmissions only for one cycle 3d = Bus keeper is enabled during LSB transmissions only for one and half cycles

Table 57. ASI_CFG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	TX_OFFSET[4:0]	RW	0h	ASI data MSB slot 0 offset (on the primary and secondary data pin). 0d = ASI data MSB location has no offset and is as per standard protocol 1d = ASI data MSB location (TDM mode is slot 0 or I^2S, LJ mode is the left and right slot 0) offset of one BCLK cycle with respect to standard protocol 2d = ASI data MSB location (TDM mode is slot 0 or I^2S, LJ mode is the left and right slot 0) offset of two BCLK cycles with respect to standard protocol 3d to 30d = ASI data MSB location (TDM mode is slot 0 or I^2S, LJ mode is the left and right slot 0) offset assigned as per configuration 31d = ASI data MSB location (TDM mode is slot 0 or I^2S, LJ mode is the left and right slot 0) offset of 31 BCLK cycles with respect to standard protocol

8.6.1.3.7 ASI_CFG2 Register (page = 0x00, address = 0x09) [reset = 0h]

This register is the ASI configuration register 2.

Figure 102. ASI_CFG2 Register

7	6	5	4	3	2	1	0
ASI_DAISY	Reserved	ASI_ERR	ASI_ERR_RCOV	Reserved			
RW-0h	R-0h	RW-0h	RW-0h	R-0h			

Table 58. ASI_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ASI_DAISY	RW	0h	ASI daisy chain connection. 0d = All devices are connected in the common ASI bus 1d = All devices are daisy-chained for the ASI bus
6	Reserved	R	0h	Reserved
5	ASI_ERR	RW	0h	ASI bus error detection. 0d = Enable bus error detection 1d = Disable bus error detection
4	ASI_ERR_RCOV	RW	0h	ASI bus error auto resume. 0d = Enable auto resume after bus error recovery 1d = Disable auto resume after bus error recovery and remain powered down until the host configures the device
3-0	Reserved	R	0h	Reserved

8.6.1.3.8 ASI_CH1 Register (page = 0x00, address = 0x0B) [reset = 0h]

This register is the ASI slot configuration register for channel 1.

Figure 103. ASI_CH1 Register

7	6	5	4	3	2	1	0
Reserved	CH1_OUTPUT	CH1_SLOT[5:0]					
R-0h	RW-0h	RW-0h					

Table 59. ASI_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	CH1_OUTPUT	RW	0h	Channel 1 output line. 0d = Channel 1 output is on the ASI primary output pin (SDOUT) 1d = Channel 1 output is on the ASI secondary output pin (GPIO1 or GPOx)

Table 59. ASI_CH1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	CH1_SLOT[5:0]	RW	0h	Channel 1 slot assignment. 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is left slot 31 32d = TDM is slot 32 or I^2S, LJ is right slot 0 33d = TDM is slot 33 or I^2S, LJ is right slot 1 34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I^2S, LJ is right slot 31

8.6.1.3.9 ASI_CH2 Register (page = 0x00, address = 0x0C) [reset = 1h]

This register is the ASI slot configuration register for channel 2.

Figure 104. ASI_CH2 Register

7	6	5	4	3	2	1	0
Reserved	CH2_OUTPUT	CH2_SLOT[5:0]					
R-0h	RW-0h	RW-1h					

Table 60. ASI_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	CH2_OUTPUT	RW	0h	Channel 2 output line. 0d = Channel 2 output is on the ASI primary output pin (SDOUT) 1d = Channel 2 output is on the ASI secondary output pin (GPIO1 or GPOx)
5-0	CH2_SLOT[5:0]	RW	1h	Channel 2 slot assignment. 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is left slot 31 32d = TDM is slot 32 or I^2S, LJ is right slot 0 33d = TDM is slot 33 or I^2S, LJ is right slot 1 34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I^2S, LJ is right slot 31

8.6.1.3.10 ASI_CH3 Register (page = 0x00, address = 0x0D) [reset = 2h]

This register is the ASI slot configuration register for channel 3.

Figure 105. ASI_CH3 Register

7	6	5	4	3	2	1	0
Reserved	CH3_OUTPUT	CH3_SLOT[5:0]					
R-0h	RW-0h	RW-2h					

Table 61. ASI_CH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	CH3_OUTPUT	RW	0h	Channel 3 output line. 0d = Channel 3 output is on the ASI primary output pin (SDOUT) 1d = Channel 3 output is on the ASI secondary output pin (GPIO1 or GPOx)

Table 61. ASI_CH3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	CH3_SLOT[5:0]	RW	2h	Channel 3 slot assignment. 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is left slot 31 32d = TDM is slot 32 or I^2S, LJ is right slot 0 33d = TDM is slot 33 or I^2S, LJ is right slot 1 34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I^2S, LJ is right slot 31

8.6.1.3.11 ASI_CH4 Register (page = 0x00, address = 0x0E) [reset = 3h]

This register is the ASI slot configuration register for channel 4.

Figure 106. ASI_CH4 Register

7	6	5	4	3	2	1	0
Reserved	CH4_OUTPUT	CH4_SLOT[5:0]					
R-0h	RW-0h	RW-3h					

Table 62. ASI_CH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	CH4_OUTPUT	RW	0h	Channel 4 output line. 0d = Channel 4 output is on the ASI primary output pin (SDOUT) 1d = Channel 4 output is on the ASI secondary output pin (GPIO1 or GPOx)
5-0	CH4_SLOT[5:0]	RW	3h	Channel 4 slot assignment. 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is left slot 31 32d = TDM is slot 32 or I^2S, LJ is right slot 0 33d = TDM is slot 33 or I^2S, LJ is right slot 1 34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I^2S, LJ is right slot 31

8.6.1.3.12 ASI_CH5 Register (page = 0x00, address = 0x0F) [reset = 4h]

This register is the ASI slot configuration register for channel 5. Applicable only for PCM6x60-Q1.

Figure 107. ASI_CH5 Register

7	6	5	4	3	2	1	0
Reserved	CH5_OUTPUT	CH5_SLOT[5:0]					
R-0h	RW-0h	RW-4h					

Table 63. ASI_CH5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	CH5_OUTPUT	RW	0h	Channel 5 output line. 0d = Channel 5 output is on the ASI primary output pin (SDOUT) 1d = Channel 5 output is on the ASI secondary output pin (GPIO1 or GPOx)

Table 63. ASI_CH5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	CH5_SLOT[5:0]	RW	4h	Channel 5 slot assignment. 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is left slot 31 32d = TDM is slot 32 or I^2S, LJ is right slot 0 33d = TDM is slot 33 or I^2S, LJ is right slot 1 34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I^2S, LJ is right slot 31

8.6.1.3.13 ASI_CH6 Register (page = 0x00, address = 0x10) [reset = 5h]

This register is the ASI slot configuration register for channel 6. Applicable only for PCM6x60-Q1.

Figure 108. ASI_CH6 Register

7	6	5	4	3	2	1	0
Reserved	CH6_OUTPUT	CH6_SLOT[5:0]					
R-0h	RW-0h	RW-5h					

Table 64. ASI_CH6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	CH6_OUTPUT	RW	0h	Channel 6 output line. 0d = Channel 6 output is on the ASI primary output pin (SDOUT) 1d = Channel 6 output is on the ASI secondary output pin (GPIO1 or GPOx)
5-0	CH6_SLOT[5:0]	RW	5h	Channel 6 slot assignment. 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is left slot 31 32d = TDM is slot 32 or I^2S, LJ is right slot 0 33d = TDM is slot 33 or I^2S, LJ is right slot 1 34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I^2S, LJ is right slot 31

8.6.1.3.14 MST_CFG0 Register (page = 0x00, address = 0x13) [reset = 2h]

83

This register is the ASI master mode configuration register 0.

Figure 109. MST_CFG0 Register

7	6	5	4	3	2	1	0
MST_SLV_CFG	AUTO_CLK_CFG	AUTO_MODE_PLL_DIS	BCLK_FSYNC_GATE	FS_MODE	MCLK_FREQ_SEL[2:0]		
RW-0h	RW-0h	RW-0h	RW-0h	RW-0h	RW-2h		

Table 65. MST_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MST_SLV_CFG	RW	0h	ASI master or slave configuration register setting. 0d = Device is in slave mode (both BCLK and FSYNC are inputs to the device) 1d = Device is in master mode (both BCLK and FSYNC are generated from the device)
6	AUTO_CLK_CFG	RW	0h	Automatic clock configuration setting. 0d = Auto clock configuration is enabled (all internal clock divider and PLL configurations are auto derived) 1d = Auto clock configuration is disabled (custom mode and device GUI must be used for the device configuration settings)

Table 65. MST_CFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	AUTO_MODE_PLL_DIS	RW	0h	Automatic mode PLL setting. 0d = PLL is enabled in auto clock configuration 1d = PLL is disabled in auto clock configuration
4	BCLK_FSYNC_GATE	RW	0h	BCLK and FSYNC clock gate (valid when the device is in master mode). 0d = Do not gate BCLK and FSYNC 1d = Force gate BCLK and FSYNC when being transmitted from the device in master mode
3	FS_MODE	RW	0h	Sample rate setting (valid when the device is in master mode). 0d = f_S is a multiple (or submultiple) of 48 kHz 1d = f_S is a multiple (or submultiple) of 44.1 kHz
2-0	MCLK_FREQ_SEL[2:0]	RW	2h	These bits select the MCLK (GPIO or GPIx) frequency for the PLL source clock input (valid when the device is in master mode and MCLK_FREQ_SEL_MODE = 0). 0d = 12 MHz 1d = 12.288 MHz 2d = 13 MHz 3d = 16 MHz 4d = 19.2 MHz 5d = 19.68 MHz 6d = 24 MHz 7d = 24.576 MHz

8.6.1.3.15 MST_CFG1 Register (page = 0x00, address = 0x14) [reset = 48h]

48

This register is the ASI master mode configuration register 1.

Figure 110. MST_CFG1 Register

7	6	5	4	3	2	1	0
FS_RATE[3:0]				FS_BCLK_RATIO[3:0]			
RW-4h				RW-8h			

Table 66. MST_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	FS_RATE[3:0]	RW	4h	Programmed sample rate of the ASI bus (not used when the device is configured in slave mode auto clock configuration). 0d = 7.35 kHz or 8 kHz 1d = 14.7 kHz or 16 kHz 2d = 22.05 kHz or 24 kHz 3d = 29.4 kHz or 32 kHz 4d = 44.1 kHz or 48 kHz 5d = 88.2 kHz or 96 kHz 6d = 176.4 kHz or 192 kHz 7d = 352.8 kHz or 384 kHz 8d = 705.6 kHz or 768 kHz 9d to 15d = Reserved
3-0	FS_BCLK_RATIO[3:0]	RW	8h	Programmed BCLK to FSYNC frequency ratio of the ASI bus (not used when the device is configured in slave mode auto clock configuration). 0d = Ratio of 16 1d = Ratio of 24 2d = Ratio of 32 3d = Ratio of 48 4d = Ratio of 64 5d = Ratio of 96 6d = Ratio of 128 7d = Ratio of 192 8d = Ratio of 256 9d = Ratio of 384 10d = Ratio of 512 11d = Ratio of 1024 12d = Ratio of 2048 13d = Reserved 14d = Ratio of 144 15d = Reserved

8.6.1.3.16 ASI_STS Register (page = 0x00, address = 0x15) [reset = FFh]

This register s the ASI bus clock monitor status register

Figure 111. ASI_STS Register

7	6	5	4	3	2	1	0
FS_RATE_STS[3:0]				FS_RATIO_STS[3:0]			
R-Fh				R-Fh			

Table 67. ASI_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	FS_RATE_STS[3:0]	R	Fh	Detected sample rate of the ASI bus. 0d = 7.35 kHz or 8 kHz 1d = 14.7 kHz or 16 kHz 2d = 22.05 kHz or 24 kHz 3d = 29.4 kHz or 32 kHz 4d = 44.1 kHz or 48 kHz 5d = 88.2 kHz or 96 kHz 6d = 176.4 kHz or 192 kHz 7d = 352.8 kHz or 384 kHz 8d = 705.6 kHz or 768 kHz 9d to 14d = Reserved 15d = Invalid sample rate
3-0	FS_RATIO_STS[3:0]	R	Fh	Detected BCLK to FSYNC frequency ratio of the ASI bus. 0d = Ratio of 16 1d = Ratio of 24 2d = Ratio of 32 3d = Ratio of 48 4d = Ratio of 64 5d = Ratio of 96 6d = Ratio of 128 7d = Ratio of 192 8d = Ratio of 256 9d = Ratio of 384 10d = Ratio of 512 11d = Ratio of 1024 12d = Ratio of 2048 13d = Reserved 14d = Ratio of 144 15d = Invalid ratio

8.6.1.3.17 CLK_SRC Register (page = 0x00, address = 0x16) [reset = 10h]

This register is the clock source configuration register. ~~d8: 11 011 000~~

Figure 112. CLK_SRC Register d8: 10 011 000

7	6	5	4	3	2	1	0
DIS_PLL_SLV_CLK_SRC	MCLK_FREQ_SEL_MODE	MCLK_RATIO_SEL[2:0]			Reserved		
RW-0h	RW-0h	RW-2h			R-0h		

Table 68. CLK_SRC Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DIS_PLL_SLV_CLK_SRC	RW	0h	Audio root clock source setting when the device is configured with the PLL disabled in the auto clock configuration for slave mode (AUTO_MODE_PLL_DIS = 1). 0d = BCLK is used as the audio root clock source 1d = MCLK (GPIOx or GPIx) is used as the audio root clock source (the MCLK to FSYNC ratio is as per MCLK_RATIO_SEL setting)

Table 68. CLK_SRC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	MCLK_FREQ_SEL_MODE	RW	0h	Master mode MCLK (GPIOx or GPIx) frequency selection mode (valid when the device is in auto clock configuration). 0d = MCLK frequency is based on the MCLK_FREQ_SEL (P0_R13) configuration 1d = MCLK frequency is specified as a multiple of FSYNC in the MCLK_RATIO_SEL (P0_R32) configuration
5-3	MCLK_RATIO_SEL[2:0]	RW	2h	These bits select the MCLK (GPIOx or GPIx) to FSYNC ratio for master mode or when MCLK is used as the audio root clock source in slave mode. 0d = Ratio of 64 1d = Ratio of 256 2d = Ratio of 384 3d = Ratio of 512 4d = Ratio of 768 5d = Ratio of 1024 6d = Ratio of 1536 7d = Ratio of 2304
2-0	Reserved	R	0h	Reserved

8.6.1.3.18 GPIO_CFG0 Register (page = 0x00, address = 0x21) [reset = 22h]

This register is the GPIO configuration register 0.

Figure 113. GPIO_CFG0 Register

7	6	5	4	3	2	1	0
GPIO1_CFG[3:0]				Reserved	GPIO1_DRV[2:0]		
RW-2h				R-0h	RW-2h		

Table 69. GPIO_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	GPIO1_CFG[3:0]	RW	2h	GPIO1 configuration. 0d = GPIO1 is disabled 1d = GPIO1 is configured as a general-purpose output (GPO) 2d = GPIO1 is configured as a device interrupt output (IRQ) 3d = GPIO1 is configured as a secondary ASI output (SDOUT2) 4d = Reserved 5d = Reserved 6d = Reserved 7d = GPIO1 is configured as an input to power down all ADC channels 8d = GPIO1 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN) 9d = GPIO1 is configured as a general-purpose input (GPI) 10d = GPIO1 is configured as a master clock input (MCLK) 11d = GPIO1 is configured as an ASI input for daisy-chain (SDIN) 12d = Reserved 13d = Reserved 14d = Reserved
3	Reserved	R	0h	Reserved
2-0	GPIO1_DRV[2:0]	RW	2h	GPIO1 output drive configuration (not used when GPIO1 is configured as SDOUT2). 0d = Hi-Z output 1d = Drive active low and active high 2d = Drive active low and weak high 3d = Drive active low and Hi-Z 4d = Drive weak low and active high 5d = Drive Hi-Z and active high 6d to 7d = Reserved

8.6.1.3.19 GPIO_CFG1 Register (page = 0x00, address = 0x22) [reset = 0h]

This register is the GPIO configuration register 1. Not applicable for PCM6x60-Q1.

Figure 114. GPIO_CFG1 Register

7	6	5	4	3	2	1	0
GPIO2_CFG[3:0]				Reserved	GPIO2_DRV[2:0]		
RW-0h				R-0h	RW-0h		

Table 70. GPIO_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	GPIO2_CFG[3:0]	RW	0h	GPIO2 configuration. 0d = GPIO2 is disabled 1d = GPIO2 is configured as a general-purpose output (GPO) 2d = GPIO2 is configured as a device interrupt output (IRQ) 3d = GPIO2 is configured as a secondary ASI output (SDOUT2) 4d = Reserved 5d = Reserved 6d = Reserved 7d = GPIO2 is configured as an input to power down all ADC channels 8d = GPIO2 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN) 9d = GPIO2 is configured as a general-purpose input (GPI) 10d = GPIO2 is configured as a master clock input (MCLK) 11d = GPIO2 is configured as an ASI input for daisy-chain (SDIN) 12d = Reserved 13d = Reserved 14d = Reserved
3	Reserved	R	0h	Reserved
2-0	GPIO2_DRV[2:0]	RW	0h	GPIO2 output drive configuration (not used when GPIO2 is configured as SDOUT2). 0d = Hi-Z output 1d = Drive active low and active high 2d = Drive active low and weak high 3d = Drive active low and Hi-Z 4d = Drive weak low and active high 5d = Drive Hi-Z and active high 6d to 7d = Reserved

8.6.1.3.20 GPIO_CFG2 Register (page = 0x00, address = 0x23) [reset = 0h]

This register is the GPIO configuration register 2. Not applicable for PCM6x60-Q1.

Figure 115. GPIO_CFG2 Register

7	6	5	4	3	2	1	0
GPIO3_CFG[3:0]				Reserved	GPIO3_DRV[2:0]		
RW-0h				R-0h	RW-0h		

Table 71. GPIO_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	GPIO3_CFG[3:0]	RW	0h	GPIO3 configuration. 0d = GPIO3 is disabled 1d = GPIO3 is configured as a general-purpose output (GPO) 2d = GPIO3 is configured as a device interrupt output (IRQ) 3d = GPIO3 is configured as a secondary ASI output (SDOUT2) 4d = Reserved 5d = Reserved 6d = Reserved 7d = GPIO3 is configured as an input to power down all ADC channels 8d = GPIO3 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN) 9d = GPIO3 is configured as a general-purpose input (GPI) 10d = GPIO3 is configured as a master clock input (MCLK) 11d = GPIO3 is configured as an ASI input for daisy-chain (SDIN) 12d = Reserved 13d = Reserved 14d = Reserved
3	Reserved	R	0h	Reserved

Table 71. GPIO_CFG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	GPIO3_DRV[2:0]	RW	0h	GPIO3 output drive configuration (not used when GPIO3 is configured as SDOUT2). 0d = Hi-Z output 1d = Drive active low and active high 2d = Drive active low and weak high 3d = Drive active low and Hi-Z 4d = Drive weak low and active high 5d = Drive Hi-Z and active high 6d to 7d = Reserved

8.6.1.3.21 GPI_CFG0 Register (page = 0x00, address = 0x24) [reset = 0h]

This register is the GPI configuration register 0. Not applicable for PCM6x60-Q1.

Figure 116. GPI_CFG0 Register

7	6	5	4	3	2	1	0
GPI1_CFG[3:0]				Reserved			
RW-0h				R-0h			

Table 72. GPI_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	GPI1_CFG[3:0]	RW	0h	GPI1 configuration. 0d = GPI1 is disabled 1d to 6d = Reserved 7d = GPI1 is configured as an input to power down all ADC channels 8d = GPI1 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN) 9d = GPI1 is configured as a general-purpose input (GPI) 10d = GPI1 is configured as a master clock input (MCLK) 11d = GPI1 is configured as an ASI input for daisy-chain (SDIN) 12d = Reserved 13d = Reserved 14d = Reserved
3-0	Reserved	R	0h	Reserved

8.6.1.3.22 GPI_CFG1 Register (page = 0x00, address = 0x25) [reset = 0h]

This register is the GPI configuration register 1. Not applicable for PCM6x60-Q1.

Figure 117. GPI_CFG1 Register

7	6	5	4	3	2	1	0
GPI2_CFG[3:0]				Reserved			
RW-0h				R-0h			

Table 73. GPI_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	GPI2_CFG[3:0]	RW	0h	GPI2 configuration. 0d = GPI2 is disabled 1d to 6d = Reserved 7d = GPI2 is configured as an input to power down all ADC channels 8d = GPI2 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN) 9d = GPI2 is configured as a general-purpose input (GPI) 10d = GPI2 is configured as a master clock input (MCLK) 11d = GPI2 is configured as an ASI input for daisy-chain (SDIN) 12d = Reserved 13d = Reserved 14d = Reserved
3-0	Reserved	R	0h	Reserved

8.6.1.3.23 GPIO_VAL Register (page = 0x00, address = 0x26) [reset = 0h]

This register is the GPIO output value register.

Figure 118. GPIO_VAL Register

7	6	5	4	3	2	1	0
GPIO1_VAL	GPIO2_VAL	GPIO3_VAL	Reserved				
RW-0h	RW-0h	RW-0h	R-0h				

Table 74. GPIO_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO1_VAL	RW	0h	GPIO1 output value when configured as a GPO. 0d = Drive the output with a value of 0 1d = Drive the output with a value of 1
6	GPIO2_VAL	RW	0h	GPIO2 output value when configured as a GPO. Not applicable for PCM6x60-Q1. 0d = Drive the output with a value of 0 1d = Drive the output with a value of 1
5	GPIO3_VAL	RW	0h	GPIO3 output value when configured as a GPO. Not applicable for PCM6x60-Q1. 0d = Drive the output with a value of 0 1d = Drive the output with a value of 1
4-0	Reserved	R	0h	Reserved

8.6.1.3.24 GPIO_MON Register (page = 0x00, address = 0x27) [reset = 0h]

This register is the GPIO monitor value register.

Figure 119. GPIO_MON Register

7	6	5	4	3	2	1	0
GPIO1_MON	GPIO2_MON	GPIO3_MON	GPI1_MON	GPI2_MON	Reserved		
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h		

Table 75. GPIO_MON Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO1_MON	R	0h	GPIO1 monitor value when configured as a GPI. 0d = Input monitor value 0 1d = Input monitor value 1
6	GPIO2_MON	R	0h	GPIO2 monitor value when configured as a GPI. Not applicable for PCM6x60-Q1. 0d = Input monitor value 0 1d = Input monitor value 1
5	GPIO3_MON	R	0h	GPIO3 monitor value when configured as a GPI. Not applicable for PCM6x60-Q1. 0d = Input monitor value 0 1d = Input monitor value 1
4	GPI1_MON	R	0h	GPI1 monitor value when configured as a GPI. Not applicable for PCM6x60-Q1. 0d = Input monitor value 0 1d = Input monitor value 1
3	GPI2_MON	R	0h	GPI2 monitor value when configured as a GPI. Not applicable for PCM6x60-Q1. 0d = Input monitor value 0 1d = Input monitor value 1
2-0	Reserved	R	0h	Reserved

8.6.1.3.25 INT_CFG Register (page = 0x00, address = 0x28) [reset = 0h]

This regiser is the interrupt configuration register.

Figure 120. INT_CFG Register

7	6	5	4	3	2	1	0
INT_POL	INT_EVENT[1:0]		PD_ON_FLT_CFG[1:0]		LTCH_READ_CFG	PD_ON_FLT_RCV_CFG	LTCH_CLR_ON_READ
RW-0h	RW-0h		RW-0h		RW-0h	RW-0h	RW-0h

Table 76. INT_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_POL	RW	0h	Interrupt polarity. 0d = Active low (IRQZ) 1d = Active high (IRQ)
6-5	INT_EVENT[1:0]	RW	0h	Interrupt event configuration. 0d = INT asserts on any unmasked latched interrupts event 1d = Reserved 2d = INT asserts for 2 ms (typical) for every 4-ms (typical) duration on any unmasked latched interrupts event 3d = INT asserts for 2 ms (typical) one time on each pulse for any unmasked interrupts event
4-3	PD_ON_FLT_CFG[1:0]	RW	0h	Powerdown configuration when fault detected for any channel or MICBIAS fault detected. 0d = Faults event are not used for ADC and MICBIAS power down. It is recommend to set these bits as 2d to shutdown the blocks for which fault occurred. 1d = Only unmasked faults are used for power down of respective ADC channel; In case of MICBIAS fault detected, MICBIAS and all ADC channels gets powered-down based on P0_R58 settings 2d = Both masked or unmasked faults are used for power down of respective ADC channel; In case of MICBIAS fault detected, MICBIAS and all ADC channels gets powered-down based on P0_R58 settings. 3d = Reserved
2	LTCH_READ_CFG	RW	0h	Interrupt latch registers readback configuration. 0d = All interrupts can be read through the LTCH registers 1d = Only unmasked interrupts can be read through the LTCH registers
1	PD_ON_FLT_RCV_CFG	RW	0h	Recovery configuration for ADC channels when fault goes away. 0d = Auto recovery, ADC channels are re-powered up when fault goes away 1d = Manual recovery, ADC channels are required to power-up manually using P0_R119 when fault goes away
0	LTCH_CLR_ON_READ	RW	0h	Configuration for clearing LTCH register bits. 0d = LTCH register bits are cleared on register read only if live status is zero 1d = LTCH register bits are cleared on register read irrespective of live status and set only if live status goes again low to high

8.6.1.3.26 INT_MASK0 Register (page = 0x00, address = 0x29) [reset = FFh]

This register is the interrupt masks register 0.

Figure 121. INT_MASK0 Register

7	6	5	4	3	2	1	0
INT_MASK0[7]	INT_MASK0[6]	INT_MASK0[5]	INT_MASK0[4]	Reserved	Reserved	Reserved	Reserved
RW-1h	RW-1h	RW-1h	RW-1h	RW-1h	RW-1h	RW-1h	RW-1h

Table 77. INT_MASK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_MASK0[7]	RW	1h	ASI clock error mask. 0d = Unmask 1d = Mask
6	INT_MASK0[6]	RW	1h	PLL lock interrupt mask. 0d = Unmask 1d = Mask
5	INT_MASK0[5]	RW	1h	Boost or MICBIAS over temperature interrupt mask. 0d = Unmask 1d = Mask

Table 77. INT_MASK0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	INT_MASK0[4]	RW	1h	Boost or MICBIAS over current interrupt mask. 0d = Unmask 1d = Mask
3	Reserved	RW	1h	Reserved
2	Reserved	RW	1h	Reserved
1	Reserved	RW	1h	Reserved
0	Reserved	RW	1h	Reserved

8.6.1.3.27 INT_MASK1 Register (page = 0x00, address = 0x2A) [reset = 3h]

This register is the interrupt masks register 1.

Figure 122. INT_MASK1 Register

7	6	5	4	3	2	1	0
INT_MASK1[7]	INT_MASK1[6]	INT_MASK1[5]	INT_MASK1[4]	INT_MASK1[3]	INT_MASK1[2]	INT_MASK1[1]	Reserved
RW-0h	RW-0h	RW-0h	RW-0h	RW-0h	RW-0h	RW-1h	RW-1h

Table 78. INT_MASK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_MASK1[7]	RW	0h	Channel 1 input DC faults diagnostic interrupt mask. 0d = Unmask 1d = Mask
6	INT_MASK1[6]	RW	0h	Channel 2 input DC faults diagnostic interrupt mask. 0d = Unmask 1d = Mask
5	INT_MASK1[5]	RW	0h	Channel 3 input DC faults diagnostic interrupt mask. 0d = Unmask 1d = Mask
4	INT_MASK1[4]	RW	0h	Channel 4 input DC faults diagnostic interrupt mask. 0d = Unmask 1d = Mask
3	INT_MASK1[3]	RW	0h	Channel 5 input DC faults diagnostic interrupt mask. Applicable only for PCM6x60-Q1. 0d = Unmask 1d = Mask
2	INT_MASK1[2]	RW	0h	Channel 6 input DC faults diagnostic interrupt mask. Applicable only for PCM6x60-Q1. 0d = Unmask 1d = Mask
1	INT_MASK1[1]	RW	1h	Input faults diagnostic interrupt mask for "short to VBAT_IN" detect when VBAT_IN voltage is less than MICBIAS voltage. 0d = Unmask 1d = Mask
0	Reserved	RW	1h	Reserved

8.6.1.3.28 INT_MASK2 Register (page = 0x00, address = 0x2B) [reset = 0h]

This register is the interrupt masks register 2.

Figure 123. INT_MASK2 Register

7	6	5	4	3	2	1	0
INT_MASK2[7]	INT_MASK2[6]	INT_MASK2[5]	INT_MASK2[4]	INT_MASK2[3]	INT_MASK2[2]	INT_MASK2[1]	INT_MASK2[0]
RW-0h	RW-0h	RW-0h	RW-0h	RW-0h	RW-0h	RW-0h	RW-0h

Table 79. INT_MASK2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_MASK2[7]	RW	0h	Input diagnostics; Open inputs fault interrupt mask. 0d = Unmask 1d = Mask
6	INT_MASK2[6]	RW	0h	Input diagnostics; Inputs shorted fault interrupt mask. 0d = Unmask 1d = Mask
5	INT_MASK2[5]	RW	0h	Input diagnostics; INxP shorted to ground fault interrupt mask. 0d = Unmask 1d = Mask
4	INT_MASK2[4]	RW	0h	Input diagnostics; INxM shorted to ground fault interrupt mask. 0d = Unmask 1d = Mask
3	INT_MASK2[3]	RW	0h	Input diagnostics; INxP shorted to MICBIAS fault interrupt mask. 0d = Unmask 1d = Mask
2	INT_MASK2[2]	RW	0h	Input diagnostics; INxM shorted to MICBIAS fault interrupt mask. 0d = Unmask 1d = Mask
1	INT_MASK2[1]	RW	0h	Input diagnostics; INxP shorted to VBAT_IN fault interrupt mask. 0d = Unmask 1d = Mask
0	INT_MASK2[0]	RW	0h	Input diagnostics; INxM shorted to VBAT_IN fault interrupt mask. 0d = Unmask 1d = Mask

8.6.1.3.29 INT_LTCH0 Register (page = 0x00, address = 0x2C) [reset = 0h]

This register is the latched Interrupt readback register 0.

Figure 124. INT_LTCH0 Register

7	6	5	4	3	2	1	0
INT_LTCH0[7]	INT_LTCH0[6]	INT_LTCH0[5]	INT_LTCH0[4]	Reserved	Reserved	Reserved	Reserved
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 80. INT_LTCH0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LTCH0[7]	R	0h	Fault status for an ASI bus clock error (self-clearing bit). 0d = No fault detected 1d = Fault detected
6	INT_LTCH0[6]	R	0h	Status of PLL lock (self-clearing bit). 0d = No PLL lock detected 1d = PLL lock detected
5	INT_LTCH0[5]	R	0h	Fault status for boost or MICBIAS over temperature (self-clearing bit). 0d = No fault detected 1d = Fault detected
4	INT_LTCH0[4]	R	0h	Fault status for boost or MICBIAS over current (self-clearing bit). 0d = No fault detected 1d = Fault detected
3	Reserved	R	0h	Reserved
2	Reserved	R	0h	Reserved
1	Reserved	R	0h	Reserved
0	Reserved	R	0h	Reserved

8.6.1.3.30 CHx_LTCH Register (page = 0x00, address = 0x2D) [reset = 0h]

This register is the latched Interrupt status register for channel level diagnostic summary.

Figure 125. CHx_LTCH Register

7	6	5	4	3	2	1	0
STS_CHx_LTCH[7]	STS_CHx_LTCH[6]	STS_CHx_LTCH[5]	STS_CHx_LTCH[4]	STS_CHx_LTCH[3]	STS_CHx_LTCH[2]	STS_CHx_LTCH[1]	Reserved
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 81. CHx_LTCH Register Field Descriptions

Bit	Field	Type	Reset	Description
7	STS_CHx_LTCH[7]	R	0h	Status of CH1_LTCH (self-clearing bit). 0d = No faults occurred in channel 1 1d = Atleast a fault has occurred in channel 1
6	STS_CHx_LTCH[6]	R	0h	Status of CH2_LTCH (self-clearing bit). 0d = No faults occurred in channel 2 1d = Atleast a fault has occurred in channel 2
5	STS_CHx_LTCH[5]	R	0h	Status of CH3_LTCH (self-clearing bit). 0d = No faults occurred in channel 3 1d = Atleast a fault has occurred in channel 3
4	STS_CHx_LTCH[4]	R	0h	Status of CH4_LTCH (self-clearing bit). 0d = No faults occurred in channel 4 1d = Atleast a fault has occurred in channel 4
3	STS_CHx_LTCH[3]	R	0h	Status of CH5_LTCH (self-clearing bit). Applicable only for PCM6x60-Q1. 0d = No faults occurred in channel 5 1d = Atleast a fault has occurred in channel 5
2	STS_CHx_LTCH[2]	R	0h	Status of CH6_LTCH (self-clearing bit). Applicable only for PCM6x60-Q1. 0d = No faults occurred in channel 6 1d = Atleast a fault has occurred in channel 6
1	STS_CHx_LTCH[1]	R	0h	Status of short to VBAT_IN fault detected when VBAT_IN is less than MICBIAS (self-clearing bit). 0d = Short to VBAT_IN fault when VBAT_IN is less than MICBIAS has not occurred in any channel 1d = Short to VBAT_IN fault when VBAT_IN is less than MICBIAS has occurred in atleast one channel
0	Reserved	R	0h	Reserved

8.6.1.3.31 CH1_LTCH Register (page = 0x00, address = 0x2E) [reset = 0h]

This register is the latched Interrupt status register for channel 1 fault diagnostic

Figure 126. CH1_LTCH Register

7	6	5	4	3	2	1	0
CH1_LTCH[7]	CH1_LTCH[6]	CH1_LTCH[5]	CH1_LTCH[4]	CH1_LTCH[3]	CH1_LTCH[2]	CH1_LTCH[1]	CH1_LTCH[0]
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 82. CH1_LTCH Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH1_LTCH[7]	R	0h	Channel 1 open input fault status (self-clearing bit). 0d = No open input detected 1d = Open input detected
6	CH1_LTCH[6]	R	0h	Channel 1 input pair short fault status (self-clearing bit). 0d = No input pair short detected 1d = Input short to each other detected
5	CH1_LTCH[5]	R	0h	Channel 1 IN1P short to ground fault status (self-clearing bit). 0d = IN1P no short to ground detected 1d = IN1P short to ground detected
4	CH1_LTCH[4]	R	0h	Channel 1 IN1M short to ground fault status (self-clearing bit). 0d = IN1M no short to ground detected 1d = IN1M short to ground detected

Table 82. CH1_LTCH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CH1_LTCH[3]	R	0h	Channel 1 IN1P short to MICBIAS fault status (self-clearing bit). 0d = IN1P no short to MICBIAS detected 1d = IN1P short to MICBIAS detected
2	CH1_LTCH[2]	R	0h	Channel 1 IN1M short to MICBIAS fault status (self-clearing bit). 0d = IN1M no short to MICBIAS detected 1d = IN1M short to MICBIAS detected
1	CH1_LTCH[1]	R	0h	Channel 1 IN1P short to VBAT_IN fault status (self-clearing bit). 0d = IN1P no short to VBAT_IN detected 1d = IN1P short to VBAT_IN detected
0	CH1_LTCH[0]	R	0h	Channel 1 IN1M short to VBAT_IN fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-54d, INT_LTCH2 register). 0d = IN1M no short to VBAT_IN detected 1d = IN1M short to VBAT_IN detected

8.6.1.3.32 CH2_LTCH Register (page = 0x00, address = 0x2F) [reset = 0h]

This register is the latched Interrupt status register for channel 2 fault diagnostic.

Figure 127. CH2_LTCH Register

7	6	5	4	3	2	1	0
CH2_LTCH[7]	CH2_LTCH[6]	CH2_LTCH[5]	CH2_LTCH[4]	CH2_LTCH[3]	CH2_LTCH[2]	CH2_LTCH[1]	CH2_LTCH[0]
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 83. CH2_LTCH Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH2_LTCH[7]	R	0h	Channel 2 open input fault status (self-clearing bit). 0d = No open input detected 1d = Open input detected
6	CH2_LTCH[6]	R	0h	Channel 2 input pair short fault status (self-clearing bit). 0d = No input pair short detected 1d = Input short to each other detected
5	CH2_LTCH[5]	R	0h	Channel 2 IN2P short to ground fault status (self-clearing bit). 0d = IN2P no short to ground detected 1d = IN2P short to ground detected
4	CH2_LTCH[4]	R	0h	Channel 2 IN2M short to ground fault status (self-clearing bit). 0d = IN2M no short to ground detected 1d = IN2M short to ground detected
3	CH2_LTCH[3]	R	0h	Channel 2 IN2P short to MICBIAS fault status (self-clearing bit). 0d = IN2P no short to MICBIAS detected 1d = IN2P short to MICBIAS detected
2	CH2_LTCH[2]	R	0h	Channel 2 IN2M short to MICBIAS fault status (self-clearing bit). 0d = IN2M no short to MICBIAS detected 1d = IN2M short to MICBIAS detected
1	CH2_LTCH[1]	R	0h	Channel 2 IN2P short to VBAT_IN fault status (self-clearing bit). 0d = IN2P no short to VBAT_IN detected 1d = IN2P short to VBAT_IN detected
0	CH2_LTCH[0]	R	0h	Channel 2 IN2M short to VBAT_IN fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-54d, INT_LTCH2 register). 0d = IN2M no short to VBAT_IN detected 1d = IN2M short to VBAT_IN detected

8.6.1.3.33 CH3_LTCH Register (page = 0x00, address = 0x30) [reset = 0h]

This register is the latched Interrupt status register for channel3 fault diagnostic

Figure 128. CH3_LTCH Register

7	6	5	4	3	2	1	0
CH3_LTCH[7]	CH3_LTCH[6]	CH3_LTCH[5]	CH3_LTCH[4]	CH3_LTCH[3]	CH3_LTCH[2]	CH3_LTCH[1]	CH3_LTCH[0]
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 84. CH3_LTCH Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH3_LTCH[7]	R	0h	Channel 3 open input fault status (self-clearing bit). 0d = No open input detected 1d = Open input detected
6	CH3_LTCH[6]	R	0h	Channel 3 input pair short fault status (self-clearing bit). 0d = No input pair short detected 1d = Input short to each other detected
5	CH3_LTCH[5]	R	0h	Channel 3 IN3P short to ground fault status (self-clearing bit). 0d = IN3P no short to ground detected 1d = IN3P short to ground detected
4	CH3_LTCH[4]	R	0h	Channel 3 IN3M short to ground fault status (self-clearing bit). 0d = IN3M no short to ground detected 1d = IN3M short to ground detected
3	CH3_LTCH[3]	R	0h	Channel 3 IN3P short to MICBIAS fault status (self-clearing bit). 0d = IN3P no short to MICBIAS detected 1d = IN3P short to MICBIAS detected
2	CH3_LTCH[2]	R	0h	Channel 3 IN3M short to MICBIAS fault status (self-clearing bit). 0d = IN3M no short to MICBIAS detected 1d = IN3M short to MICBIAS detected
1	CH3_LTCH[1]	R	0h	Channel 3 IN3P short to VBAT_IN fault status (self-clearing bit). 0d = IN3P no short to VBAT_IN detected 1d = IN3P short to VBAT_IN detected
0	CH3_LTCH[0]	R	0h	Channel 3 IN3M short to VBAT_IN fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-54d, INT_LTCH2 register). 0d = IN3M no short to VBAT_IN detected 1d = IN3M short to VBAT_IN detected

8.6.1.3.34 CH4_LTCH Register (page = 0x00, address = 0x31) [reset = 0h]

This register is the latched Interrupt status register for channel 4 fault diagnostic.

Figure 129. CH4_LTCH Register

7	6	5	4	3	2	1	0
CH4_LTCH[7]	CH4_LTCH[6]	CH4_LTCH[5]	CH4_LTCH[4]	CH4_LTCH[3]	CH4_LTCH[2]	CH4_LTCH[1]	CH4_LTCH[0]
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 85. CH4_LTCH Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH4_LTCH[7]	R	0h	Channel 4 open input fault status (self-clearing bit). 0d = No open input detected 1d = Open input detected
6	CH4_LTCH[6]	R	0h	Channel 4 input pair short fault status (self-clearing bit). 0d = No input pair short detected 1d = Input short to each other detected
5	CH4_LTCH[5]	R	0h	Channel 4 IN4P short to ground fault status (self-clearing bit). 0d = IN4P no short to ground detected 1d = IN4P short to ground detected
4	CH4_LTCH[4]	R	0h	Channel 4 IN4M short to ground fault status (self-clearing bit). 0d = IN4M no short to ground detected 1d = IN4M short to ground detected
3	CH4_LTCH[3]	R	0h	Channel 4 IN4P short to MICBIAS fault status (self-clearing bit). 0d = IN4P no short to MICBIAS detected 1d = IN4P short to MICBIAS detected

Table 85. CH4_LTCH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	CH4_LTCH[2]	R	0h	Channel 4 IN4M short to MICBIAS fault status (self-clearing bit). 0d = IN4M no short to MICBIAS detected 1d = IN4M short to MICBIAS detected
1	CH4_LTCH[1]	R	0h	Channel 4 IN4P short to VBAT_IN fault status (self-clearing bit). 0d = IN4P no short to VBAT_IN detected 1d = IN4P short to VBAT_IN detected
0	CH4_LTCH[0]	R	0h	Channel 4 IN4M short to VBAT_IN fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-54d, INT_LTCH2 register). 0d = IN4M no short to VBAT_IN detected 1d = IN4M short to VBAT_IN detected

8.6.1.3.35 CH5_LTCH Register (page = 0x00, address = 0x32) [reset = 0h]

This register is the latched Interrupt status register for channel 5 fault diagnostic. Applicable only for PCM6x60-Q1.

Figure 130. CH5_LTCH Register

7	6	5	4	3	2	1	0
CH5_LTCH[7]	CH5_LTCH[6]	CH5_LTCH[5]	CH5_LTCH[4]	CH5_LTCH[3]	CH5_LTCH[2]	CH5_LTCH[1]	CH5_LTCH[0]
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 86. CH5_LTCH Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH5_LTCH[7]	R	0h	Channel 5 open input fault status (self-clearing bit). 0d = No open input detected 1d = Open input detected
6	CH5_LTCH[6]	R	0h	Channel 5 input pair short fault status (self-clearing bit). 0d = No input pair short detected 1d = Input short to each other detected
5	CH5_LTCH[5]	R	0h	Channel 5 IN5P short to ground fault status (self-clearing bit). 0d = IN5P no short to ground detected 1d = IN5P short to ground detected
4	CH5_LTCH[4]	R	0h	Channel 5 IN5M short to ground fault status (self-clearing bit). 0d = IN5M no short to ground detected 1d = IN5M short to ground detected
3	CH5_LTCH[3]	R	0h	Channel 5 IN5P short to MICBIAS fault status (self-clearing bit). 0d = IN5P no short to MICBIAS detected 1d = IN5P short to MICBIAS detected
2	CH5_LTCH[2]	R	0h	Channel 5 IN5M short to MICBIAS fault status (self-clearing bit). 0d = IN5M no short to MICBIAS detected 1d = IN5M short to MICBIAS detected
1	CH5_LTCH[1]	R	0h	Channel 5 IN5P short to VBAT_IN fault status (self-clearing bit). 0d = IN5P no short to VBAT_IN detected 1d = IN5P short to VBAT_IN detected
0	CH5_LTCH[0]	R	0h	Channel 5 IN5M short to VBAT_IN fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-54d, INT_LTCH2 register). 0d = IN5M no short to VBAT_IN detected 1d = IN5M short to VBAT_IN detected

8.6.1.3.36 CH6_LTCH Register (page = 0x00, address = 0x33) [reset = 0h]

This register is the latched Interrupt status register for channel 6 fault diagnostic. Applicable only for PCM6x60-Q1.

Figure 131. CH6_LTCH Register

7	6	5	4	3	2	1	0
CH6_LTCH[7]	CH6_LTCH[6]	CH6_LTCH[5]	CH6_LTCH[4]	CH6_LTCH[3]	CH6_LTCH[2]	CH6_LTCH[1]	CH6_LTCH[0]
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 87. CH6_LTCH Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH6_LTCH[7]	R	0h	Channel 6 open input fault status (self-clearing bit). 0d = No open input detected 1d = Open input detected
6	CH6_LTCH[6]	R	0h	Channel 6 input pair short fault status (self-clearing bit). 0d = No input pair short detected 1d = Input short to each other detected
5	CH6_LTCH[5]	R	0h	Channel 6 IN6P short to ground fault status (self-clearing bit). 0d = IN6P no short to ground detected 1d = IN6P short to ground detected
4	CH6_LTCH[4]	R	0h	Channel 6 IN6M short to ground fault status (self-clearing bit). 0d = IN6M no short to ground detected 1d = IN6M short to ground detected
3	CH6_LTCH[3]	R	0h	Channel 6 IN6P short to MICBIAS fault status (self-clearing bit). 0d = IN6P no short to MICBIAS detected 1d = IN6P short to MICBIAS detected
2	CH6_LTCH[2]	R	0h	Channel 6 IN6M short to MICBIAS fault status (self-clearing bit). 0d = IN6M no short to MICBIAS detected 1d = IN6M short to MICBIAS detected
1	CH6_LTCH[1]	R	0h	Channel 6 IN6P short to VBAT_IN fault status (self-clearing bit). 0d = IN6P no short to VBAT_IN detected 1d = IN6P short to VBAT_IN detected
0	CH6_LTCH[0]	R	0h	Channel 6 IN6M short to VBAT_IN fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-54d, INT_LTCH2 register). 0d = IN6M no short to VBAT_IN detected 1d = IN6M short to VBAT_IN detected

8.6.1.3.37 INT_MASK3 Register (page = 0x00, address = 0x34) [reset = 0h]

This register is the interrupt masks register 3.

Figure 132. INT_MASK3 Register

7	6	5	4	3	2	1	0
INT_MASK3[7]	INT_MASK3[6]	INT_MASK3[5]	INT_MASK3[4]	INT_MASK3[3]	Reserved		
RW-0h	RW-0h	RW-0h	RW-0h	RW-0h	R-0h		

Table 88. INT_MASK3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_MASK3[7]	RW	0h	INxP over voltage fault mask. 0d = Unmask 1d = Mask
6	INT_MASK3[6]	RW	0h	INxM over voltage fault mask. 0d = Unmask 1d = Mask
5	INT_MASK3[5]	RW	0h	MICBIAS high current fault mask. 0d = Unmask 1d = Mask
4	INT_MASK3[4]	RW	0h	MICBIAS low current fault mask. 0d = Unmask 1d = Mask
3	INT_MASK3[3]	RW	0h	MICBIAS over voltage fault mask. 0d = Unmask 1d = Mask
2-0	Reserved	R	0h	Reserved

8.6.1.3.38 INT_LTCH1 Register (page = 0x00, address = 0x35) [reset = 0h]

This register is the latched Interrupt readback register 1.

Figure 133. INT_LTCH1 Register

7	6	5	4	3	2	1	0
INT_LTCH1[7]	INT_LTCH1[6]	INT_LTCH1[5]	INT_LTCH1[4]	INT_LTCH1[3]	INT_LTCH1[2]	Reserved	
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	

Table 89. INT_LTCH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LTCH1[7]	R	0h	Channel 1 IN1P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-46d, CH1_LTCH register). 0d = No IN1P over voltage fault detected 1d = IN1P over voltage fault has detected
6	INT_LTCH1[6]	R	0h	Channel 2 IN2P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-47d, CH2_LTCH register). 0d = No IN2P over voltage fault detected 1d = IN2P over voltage fault has detected
5	INT_LTCH1[5]	R	0h	Channel 3 IN3P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-48d, CH3_LTCH register). 0d = No IN3P over voltage fault detected 1d = IN3P over voltage fault has detected
4	INT_LTCH1[4]	R	0h	Channel 4 IN4P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-49d, CH4_LTCH register). 0d = No IN4P over voltage fault detected 1d = IN4P over voltage fault has detected
3	INT_LTCH1[3]	R	0h	Channel 5 IN5P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-50d, CH5_LTCH register). Applicable only for PCM6x60-Q1. 0d = No IN5P over voltage fault detected 1d = IN5P over voltage fault has detected
2	INT_LTCH1[2]	R	0h	Channel 6 IN6P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-51d, CH6_LTCH register). Applicable only for PCM6x60-Q1. 0d = No IN6P over voltage fault detected 1d = IN6P over voltage fault has detected
1-0	Reserved	R	0h	Reserved

8.6.1.3.39 INT_LTCH2 Register (page = 0x00, address = 0x36) [reset = 0h]

This register is the latched Interrupt readback register 2.

Figure 134. INT_LTCH2 Register

7	6	5	4	3	2	1	0
INT_LTCH2[7]	INT_LTCH2[6]	INT_LTCH2[5]	INT_LTCH2[4]	INT_LTCH2[3]	INT_LTCH2[2]	Reserved	
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	

Table 90. INT_LTCH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LTCH2[7]	R	0h	Channel 1 IN1M over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-46d, CH1_LTCH register). 0d = No IN1M over voltage fault detected 1d = IN1M over voltage fault has detected
6	INT_LTCH2[6]	R	0h	Channel 2 IN2M over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-47d, CH2_LTCH register). 0d = No IN2M over voltage fault detected 1d = IN2M over voltage fault has detected
5	INT_LTCH2[5]	R	0h	Channel 3 IN3M over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-48d, CH3_LTCH register). 0d = No IN3M over voltage fault detected 1d = IN3M over voltage fault has detected

Table 90. INT_LTCH2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	INT_LTCH2[4]	R	0h	Channel 4 IN4M over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-49d, CH4_LTCH register). 0d = No IN4M over voltage fault detected 1d = IN4M over voltage fault has detected
3	INT_LTCH2[3]	R	0h	Channel 5 IN5M over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-50d, CH5_LTCH register). Applicable only for PCM6x60-Q1. 0d = No IN5M over voltage fault detected 1d = IN5M over voltage fault has detected
2	INT_LTCH2[2]	R	0h	Channel 6 IN6M over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-51d, CH6_LTCH register). Applicable only for PCM6x60-Q1. 0d = No IN6M over voltage fault detected 1d = IN6M over voltage fault has detected
1-0	Reserved	R	0h	Reserved

8.6.1.3.40 INT_LTCH3 Register (page = 0x00, address = 0x37) [reset = 0h]

This register is the latched Interrupt readback register 3.

Figure 135. INT_LTCH3 Register

7	6	5	4	3	2	1	0
INT_LTCH3[7]	INT_LTCH3[6]	INT_LTCH3[5]	Reserved				
R-0h	R-0h	R-0h	R-0h				

Table 91. INT_LTCH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LTCH3[7]	R	0h	Fault status for MICBIAS high current (self-clearing bit). 0d = No fault detected 1d = Fault detected
6	INT_LTCH3[6]	R	0h	Fault status for MICBIAS low current (self-clearing bit) 0d = No fault detected 1d = Fault detected
5	INT_LTCH3[5]	R	0h	Fault status for MICBIAS over voltage (self-clearing bit). 0d = No fault detected 1d = Fault detected
4-0	Reserved	R	0h	Reserved

8.6.1.3.41 MBDIAG_CFG0 Register (page = 0x00, address = 0x38) [reset = BAh]

This register is the MICBIAS diagnostic configuration register 0.

Figure 136. MBDIAG_CFG0 Register

7	6	5	4	3	2	1	0
MBIAS_HIGH_CURR_THRS[7:0]							
RW-BAh							

Table 92. MBDIAG_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MBIAS_HIGH_CURR_THRS[7:0]	RW	BAh	Threshold for MICBIAS high load current fault diagnostic. 0d to 56d = Reserved 57d = High load current threshold is set as 0 mA (typ) 58d = High load current threshold is set as 0.54 mA (typ) 59d = High load current threshold is set as 1.08 mA (typ) 60d to 185d = High load current threshold is set as per configuration 186d = High load current threshold is set as 69.66 mA (typ) 187d to 241d = High load current threshold is set as per configuration 242d = High load current threshold is set as 99.90 mA (typ) 243d to 255d = Reserved

8.6.1.3.42 MBDIAG_CFG1 Register (page = 0x00, address = 0x39) [reset = 4Bh]

This register is the MICBIAS diagnostic configuration register 1.

Figure 137. MBDIAG_CFG1 Register

7	6	5	4	3	2	1	0
MBIAS_LOW_CURR_THRS[7:0]							
RW-4Bh							

Table 93. MBDIAG_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MBIAS_LOW_CURR_THRS[7:0]	RW	4Bh	Threshold for MICBIAS low load current fault diagnostic. 0d to 56d = Reserved 57d = Low load current threshold is set as 0 mA (typ) 58d = Low load current threshold is set as 0.54 mA (typ) 59d = Low load current threshold is set as 1.08 mA (typ) 60d to 74d = Low load current threshold is set as per configuration 75d = Low load current threshold is set as 9.72 mA (typ) 76d to 241d = Low load current threshold is set as per configuration 242d = Low load current threshold is set as 99.90 mA (typ) 243d to 255d = Reserved

8.6.1.3.43 MBDIAG_CFG2 Register (page = 0x00, address = 0x3A) [reset = 10h]

This register is the MICBIAS diagnostic configuration register 2.

Figure 138. MBDIAG_CFG2 Register

7	6	5	4	3	2	1	0
PD_MBIAS_FAULT1	PD_MBIAS_FAULT2	PD_MBIAS_FAULT3	PD_MBIAS_FAULT4	Reserved	Reserved		
RW-0h	RW-0h	RW-0h	RW-1h	RW-0h	R-0h		

Table 94. MBDIAG_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PD_MBIAS_FAULT1	RW	0h	Powerdown configuration of MICBIAS fault 1 0d = No powerdown when MICBIAS fault detected 1d = MICBIAS and all ADC channels gets powerdown when low current fault occurs and P0_R40, PD_ON_FLT_CFG = 1d 1d = MICBIAS and all ADC channels gets powerdown when high current fault occurs and P0_R40, PD_ON_FLT_CFG = 2d
6	PD_MBIAS_FAULT2	RW	0h	Powerdown configuration of MICBIAS fault 2 0d = No powerdown when MICBIAS fault detected 1d = MICBIAS and all ADC channels gets powerdown when over voltage fault occurs and P0_R40, PD_ON_FLT_CFG = 1d 1d = MICBIAS and all ADC channels gets powerdown when low current fault occurs and P0_R40, PD_ON_FLT_CFG = 2d

Table 94. MBDIAG_CFG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	PD_MBIAS_FAULT3	RW	0h	Powerdown configuration of MICBIAS fault 3 0d = No powerdown when MICBIAS fault detected 1d = MICBIAS and all ADC channels gets powerdown when over temperature fault occurs and P0_R40, PD_ON_FLT_CFG = 1d 1d = MICBIAS and all ADC channels gets powerdown when over voltage fault occurs and P0_R40, PD_ON_FLT_CFG = 2d
4	PD_MBIAS_FAULT4	RW	1h	Powerdown configuration of MICBIAS fault 4 0d = No powerdown when MICBIAS fault detected 1d = MICBIAS and all ADC channels gets powerdown when high current fault occurs and P0_R40, PD_ON_FLT_CFG = 1d 1d = MICBIAS and all ADC channels gets powerdown when over temperature fault occurs and P0_R40, PD_ON_FLT_CFG = 2d. It is recommended to use this setting to protect chip from over temperature fault.
3	Reserved	RW	0h	Reserved
2-0	Reserved	R	0h	Reserved

8.6.1.3.44 BIAS_CFG Register (page = 0x00, address = 0x3B) [reset = D0h]

This register is the MICBIAS configuration register.

Figure 139. BIAS_CFG Register

7	6	5	4	3	2	1	0
MBIAS_VAL[3:0]				Reserved		Reserved	
RW-Dh				R-0h		RW-0h	

Table 95. BIAS_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	MBIAS_VAL[3:0]	RW	Dh	MICBIAS value. 0d = Reserved 1d = Reserved 2d = Reserved 3d = Reserved 4d = Reserved 5d = Reserved 6d = Reserved 7d = Microphone bias is set to 5 V 8d = Microphone bias is set to 5.5 V 9d = Microphone bias is set to 6 V 10d = Microphone bias is set to 6.5 V 11d = Microphone bias is set to 7 V 12d = Microphone bias is set to 7.5 V 13d = Microphone bias is set to 8 V 14d = Microphone bias is set to 8.5 V 15d = Microphone bias is set to 9 V
3-2	Reserved	R	0h	Reserved
1-0	Reserved	RW	0h	Reserved

8.6.1.3.45 CH1_CFG0 Register (page = 0x00, address = 0x3C) [reset = 10h]

This register is configuration register 0 for channel 1.

Figure 140. CH1_CFG0 Register

7	6	5	4	3	2	1	0
CH1_INTYP	CH1_INSRC[1:0]		CH1_DC	CH1_MIC_IN_RANGE	CH1_PGA_CFG[1:0]		CH1_AGCEN
RW-0h	RW-0h		RW-1h	RW-0h	RW-0h		RW-0h

Table 96. CH1_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH1_INTYP	RW	0h	Channel 1 input type. 0d = Microphone input 1d = Line input
6-5	CH1_INSRC[1:0]	RW	0h	Channel 1 input configuration. 0d = Analog differential input 1d = Analog single-ended input 2d = Reserved 3d = Reserved
4	CH1_DC	RW	1h	Channel 1 input coupling. 0d = AC-coupled input 1d = DC-coupled input
3	CH1_MIC_IN_RANGE	RW	0h	Channel 1 microphone input range. 0d = Low swing mode; Differential input AC signal full-scale of 2-V_{RMS} supported provided DC differential common mode voltage IN1P - IN1M < 4.2 V. Single-ended AC signal 1-V_{RMS} supported provided DC common mode voltage is < 2.1 V. 1d = High swing mode; Differential Input IN1P-IN1M peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the channel gain and digital volume control based on the max signal level used in system.
2-1	CH1_PGA_CFG[1:0]	RW	0h	Channel 1 CMRR Configuration. 0d = High SNR performance mode 1d = Reserved 2d = High CMRR performance mode 3d = Reserved
0	CH1_AGCEN	RW	0h	Channel 1 automatic gain controller (AGC) setting. 0d = AGC disabled 1d = AGC enabled based on the configuration of bit 3 in register 108 (P0_R108); This must be used only with AC-coupled input

8.6.1.3.46 CH1_CFG1 Register (page = 0x00, address = 0x3D) [reset = 0h]

This register is configuration register 1 for channel 1.

Figure 141. CH1_CFG1 Register

7	6	5	4	3	2	1	0
CH1_GAIN[5:0]						Reserved	Reserved
RW-0h						RW-0h	R-0h

Table 97. CH1_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	CH1_GAIN[5:0]	RW	0h	Channel 1 gain. 0d = Channel gain is set to 0 dB 1d = Channel gain is set to 1 dB 2d = Channel gain is set to 2 dB 3d to 41d = Channel gain is set as per configuration 42d = Channel gain is set to 42 dB 43d to 63d = Reserved
1	Reserved	RW	0h	Reserved
0	Reserved	R	0h	Reserved

8.6.1.3.47 CH1_CFG2 Register (page = 0x00, address = 0x3E) [reset = C9h]

This register is configuration register 2 for channel 1.

Figure 142. CH1_CFG2 Register

7	6	5	4	3	2	1	0
CH1_DVOL[7:0]							
RW-C9h							

Table 98. CH1_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH1_DVOL[7:0]	RW	C9h	Channel 1 digital volume control. 0d = Digital volume is muted 1d = Digital volume control is set to -100 dB 2d = Digital volume control is set to -99.5 dB 3d to 200d = Digital volume control is set as per configuration 201d = Digital volume control is set to 0 dB 202d = Digital volume control is set to 0.5 dB 203d to 253d = Digital volume control is set as per configuration 254d = Digital volume control is set to 26.5 dB 255d = Digital volume control is set to 27 dB

8.6.1.3.48 CH1_CFG3 Register (page = 0x00, address = 0x3F) [reset = 80h]

This register is configuration register 3 for channel 1.

Figure 143. CH1_CFG3 Register

7	6	5	4	3	2	1	0
CH1_GCAL[3:0]				Reserved			
RW-8h				R-0h			

Table 99. CH1_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	CH1_GCAL[3:0]	RW	8h	Channel 1 gain calibration. 0d = Gain calibration is set to -0.8 dB 1d = Gain calibration is set to -0.7 dB 2d = Gain calibration is set to -0.6 dB 3d to 7d = Gain calibration is set as per configuration 8d = Gain calibration is set to 0 dB 9d = Gain calibration is set to 0.1 dB 10d to 13d = Gain calibration is set as per configuration 14d = Gain calibration is set to 0.6 dB 15d = Gain calibration is set to 0.7 dB
3-0	Reserved	R	0h	Reserved

8.6.1.3.49 CH1_CFG4 Register (page = 0x00, address = 0x40) [reset = 0h]

This register is configuration register 4 for channel 1.

Figure 144. CH1_CFG4 Register

7	6	5	4	3	2	1	0
CH1_PCAL[7:0]							
RW-0h							

Table 100. CH1_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH1_PCAL[7:0]	RW	0h	Channel 1 phase calibration with modulator clock resolution. 0d = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock

8.6.1.3.50 CH2_CFG0 Register (page = 0x00, address = 0x41) [reset = 10h]

This register is configuration register 0 for channel 2.

Figure 145. CH2_CFG0 Register

7	6	5	4	3	2	1	0
CH2_INTYP	CH2_INSRC[1:0]		CH2_DC	CH2_MIC_IN_RANGE	CH2_PGA_CFG[1:0]		CH2_AGCEN
RW-0h	RW-0h		RW-1h	RW-0h	RW-0h		RW-0h

Table 101. CH2_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH2_INTYP	RW	0h	Channel 2 input type. 0d = Microphone input 1d = Line input
6-5	CH2_INSRC[1:0]	RW	0h	Channel 2 input configuration. 0d = Analog differential input 1d = Analog single-ended input 2d = Reserved 3d = Reserved
4	CH2_DC	RW	1h	Channel 2 input coupling. 0d = AC-coupled input 1d = DC-coupled input
3	CH2_MIC_IN_RANGE	RW	0h	Channel 2 microphone input range. 0d = Low swing mode; Differential input AC signal full-scale of 2-V_{RMS} supported provided DC differential common mode voltage IN1P - IN1M < 4.2 V. Single-ended AC signal 1-V_{RMS} supported provided DC common mode voltage is < 2.1 V. 1d = High swing mode; Differential Input IN1P-IN1M peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the channel gain and digital volume control based on the max signal level used in system.
2-1	CH2_PGA_CFG[1:0]	RW	0h	Channel 2 CMRR Configuration. 0d = High SNR performance mode 1d = Reserved 2d = High CMRR performance mode 3d = Reserved
0	CH2_AGCEN	RW	0h	Channel 2 automatic gain controller (AGC) setting. 0d = AGC disabled 1d = AGC enabled based on the configuration of bit 3 in register 108 (P0_R108); This must be used only with AC-coupled input

8.6.1.3.51 CH2_CFG1 Register (page = 0x00, address = 0x42) [reset = 0h]

This register is configuration register 1 for channel 2.

Figure 146. CH2_CFG1 Register

7	6	5	4	3	2	1	0
CH2_GAIN[5:0]						Reserved	Reserved
RW-0h						RW-0h	R-0h

Table 102. CH2_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	CH2_GAIN[5:0]	RW	0h	Channel 2 gain. 0d = Channel gain is set to 0 dB 1d = Channel gain is set to 1 dB 2d = Channel gain is set to 2 dB 3d to 41d = Channel gain is set as per configuration 42d = Channel gain is set to 42 dB 43d to 63d = Reserved
1	Reserved	RW	0h	Reserved
0	Reserved	R	0h	Reserved

8.6.1.3.52 CH2_CFG2 Register (page = 0x00, address = 0x43) [reset = C9h]

This register is configuration register 2 for channel 2.

Figure 147. CH2_CFG2 Register

7	6	5	4	3	2	1	0
CH2_DVOL[7:0]							
RW-C9h							

Table 103. CH2_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH2_DVOL[7:0]	RW	C9h	Channel 2 digital volume control. 0d = Digital volume is muted 1d = Digital volume control is set to -100 dB 2d = Digital volume control is set to -99.5 dB 3d to 200d = Digital volume control is set as per configuration 201d = Digital volume control is set to 0 dB 202d = Digital volume control is set to 0.5 dB 203d to 253d = Digital volume control is set as per configuration 254d = Digital volume control is set to 26.5 dB 255d = Digital volume control is set to 27 dB

8.6.1.3.53 CH2_CFG3 Register (page = 0x00, address = 0x44) [reset = 80h]

This register is configuration register 3 for channel 2.

Figure 148. CH2_CFG3 Register

7	6	5	4	3	2	1	0
CH2_GCAL[3:0]				Reserved			
RW-8h				R-0h			

Table 104. CH2_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	CH2_GCAL[3:0]	RW	8h	Channel 2 gain calibration. 0d = Gain calibration is set to -0.8 dB 1d = Gain calibration is set to -0.7 dB 2d = Gain calibration is set to -0.6 dB 3d to 7d = Gain calibration is set as per configuration 8d = Gain calibration is set to 0 dB 9d = Gain calibration is set to 0.1 dB 10d to 13d = Gain calibration is set as per configuration 14d = Gain calibration is set to 0.6 dB 15d = Gain calibration is set to 0.7 dB
3-0	Reserved	R	0h	Reserved

8.6.1.3.54 CH2_CFG4 Register (page = 0x00, address = 0x45) [reset = 0h]

This register is configuration register 4 for channel 2.

Figure 149. CH2_CFG4 Register

7	6	5	4	3	2	1	0
CH2_PCAL[7:0]							
RW-0h							

Table 105. CH2_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH2_PCAL[7:0]	RW	0h	Channel 2 phase calibration with modulator clock resolution. 0d = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock

8.6.1.3.55 CH3_CFG0 Register (page = 0x00, address = 0x46) [reset = 10h]

This register is configuration register 0 for channel 3.

Figure 150. CH3_CFG0 Register

7	6	5	4	3	2	1	0
CH3_INTYP	CH3_INSRC[1:0]		CH3_DC	CH3_MIC_IN_RANGE	CH3_PGA_CFG[1:0]		CH3_AGCEN
RW-0h	RW-0h		RW-1h	RW-0h	RW-0h		RW-0h

Table 106. CH3_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH3_INTYP	RW	0h	Channel 3 input type. 0d = Microphone input 1d = Line input
6-5	CH3_INSRC[1:0]	RW	0h	Channel 3 input configuration. 0d = Analog differential input 1d = Analog single-ended input 2d = Reserved 3d = Reserved
4	CH3_DC	RW	1h	Channel 3 input coupling. 0d = AC-coupled input 1d = DC-coupled input
3	CH3_MIC_IN_RANGE	RW	0h	Channel 3 microphone input range. 0d = Low swing mode; Differential input AC signal full-scale of 2-V_{RMS} supported provided DC differential common mode voltage IN1P - IN1M < 4.2 V. Single-ended AC signal 1-V_{RMS} supported provided DC common mode voltage is < 2.1 V. 1d = High swing mode; Differential Input IN1P-IN1M peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the channel gain and digital volume control based on the max signal level used in system.
2-1	CH3_PGA_CFG[1:0]	RW	0h	Channel 3 CMRR Configuration. 0d = High SNR performance mode 1d = Reserved 2d = High CMRR performance mode 3d = Reserved
0	CH3_AGCEN	RW	0h	Channel 3 automatic gain controller (AGC) setting. 0d = AGC disabled 1d = AGC enabled based on the configuration of bit 3 in register 108 (P0_R108); This must be used only with AC-coupled input

8.6.1.3.56 CH3_CFG1 Register (page = 0x00, address = 0x47) [reset = 0h]

This register is configuration register 1 for channel 3.

Figure 151. CH3_CFG1 Register

7	6	5	4	3	2	1	0
CH3_GAIN[5:0]						Reserved	Reserved
RW-0h						RW-0h	R-0h

Table 107. CH3_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	CH3_GAIN[5:0]	RW	0h	Channel 3 gain. 0d = Channel gain is set to 0 dB 1d = Channel gain is set to 1 dB 2d = Channel gain is set to 2 dB 3d to 41d = Channel gain is set as per configuration 42d = Channel gain is set to 42 dB 43d to 63d = Reserved
1	Reserved	RW	0h	Reserved
0	Reserved	R	0h	Reserved

8.6.1.3.57 CH3_CFG2 Register (page = 0x00, address = 0x48) [reset = C9h]

This register is configuration register 2 for channel 3.

Figure 152. CH3_CFG2 Register

7	6	5	4	3	2	1	0
CH3_DVOL[7:0]							
RW-C9h							

Table 108. CH3_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH3_DVOL[7:0]	RW	C9h	Channel 3 digital volume control. 0d = Digital volume is muted 1d = Digital volume control is set to -100 dB 2d = Digital volume control is set to -99.5 dB 3d to 200d = Digital volume control is set as per configuration 201d = Digital volume control is set to 0 dB 202d = Digital volume control is set to 0.5 dB 203d to 253d = Digital volume control is set as per configuration 254d = Digital volume control is set to 26.5 dB 255d = Digital volume control is set to 27 dB

8.6.1.3.58 CH3_CFG3 Register (page = 0x00, address = 0x49) [reset = 80h]

This register is configuration register 3 for channel 3.

Figure 153. CH3_CFG3 Register

7	6	5	4	3	2	1	0
CH3_GCAL[3:0]				Reserved			
RW-8h				R-0h			

Table 109. CH3_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	CH3_GCAL[3:0]	RW	8h	Channel 3 gain calibration. 0d = Gain calibration is set to -0.8 dB 1d = Gain calibration is set to -0.7 dB 2d = Gain calibration is set to -0.6 dB 3d to 7d = Gain calibration is set as per configuration 8d = Gain calibration is set to 0 dB 9d = Gain calibration is set to 0.1 dB 10d to 13d = Gain calibration is set as per configuration 14d = Gain calibration is set to 0.6 dB 15d = Gain calibration is set to 0.7 dB
3-0	Reserved	R	0h	Reserved

8.6.1.3.59 CH3_CFG4 Register (page = 0x00, address = 0x4A) [reset = 0h]

This register is configuration register 4 for channel 3.

Figure 154. CH3_CFG4 Register

7	6	5	4	3	2	1	0
CH3_PCAL[7:0]							
RW-0h							

Table 110. CH3_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH3_PCAL[7:0]	RW	0h	Channel 3 phase calibration with modulator clock resolution. 0d = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock

8.6.1.3.60 CH4_CFG0 Register (page = 0x00, address = 0x4B) [reset = 10h]

This register is configuration register 0 for channel 4.

Figure 155. CH4_CFG0 Register

7	6	5	4	3	2	1	0
CH4_INTYP	CH4_INSRC[1:0]		CH4_DC	CH4_MIC_IN_RANGE	CH4_PGA_CFG[1:0]		CH4_AGCEN
RW-0h	RW-0h		RW-1h	RW-0h	RW-0h		RW-0h

Table 111. CH4_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH4_INTYP	RW	0h	Channel 4 input type. 0d = Microphone input 1d = Line input
6-5	CH4_INSRC[1:0]	RW	0h	Channel 4 input configuration. 0d = Analog differential input 1d = Analog single-ended input 2d = Reserved 3d = Reserved
4	CH4_DC	RW	1h	Channel 4 input coupling. 0d = AC-coupled input 1d = DC-coupled input
3	CH4_MIC_IN_RANGE	RW	0h	Channel 4 microphone input range. 0d = Low swing mode; Differential input AC signal full-scale of 2-V_{RMS} supported provided DC differential common mode voltage IN1P - IN1M < 4.2 V. Single-ended AC signal 1-V_{RMS} supported provided DC common mode voltage is < 2.1 V. 1d = High swing mode; Differential Input IN1P-IN1M peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the channel gain and digital volume control based on the max signal level used in system.
2-1	CH4_PGA_CFG[1:0]	RW	0h	Channel 4 CMRR Configuration. 0d = High SNR performance mode 1d = Reserved 2d = High CMRR performance mode 3d = Reserved
0	CH4_AGCEN	RW	0h	Channel 4 automatic gain controller (AGC) setting. 0d = AGC disabled 1d = AGC enabled based on the configuration of bit 3 in register 108 (P0_R108); This must be used only with AC-coupled input

8.6.1.3.61 CH4_CFG1 Register (page = 0x00, address = 0x4C) [reset = 0h]

This register is configuration register 1 for channel 4.

Figure 156. CH4_CFG1 Register

7	6	5	4	3	2	1	0
CH4_GAIN[5:0]						Reserved	Reserved
RW-0h						RW-0h	R-0h

Table 112. CH4_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	CH4_GAIN[5:0]	RW	0h	Channel 4 gain. 0d = Channel gain is set to 0 dB 1d = Channel gain is set to 1 dB 2d = Channel gain is set to 2 dB 3d to 41d = Channel gain is set as per configuration 42d = Channel gain is set to 42 dB 43d to 63d = Reserved
1	Reserved	RW	0h	Reserved
0	Reserved	R	0h	Reserved

8.6.1.3.62 CH4_CFG2 Register (page = 0x00, address = 0x4D) [reset = C9h]

This register is configuration register 2 for channel 4.

Figure 157. CH4_CFG2 Register

7	6	5	4	3	2	1	0
CH4_DVOL[7:0]							
RW-C9h							

Table 113. CH4_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH4_DVOL[7:0]	RW	C9h	Channel 4 digital volume control. 0d = Digital volume is muted 1d = Digital volume control is set to -100 dB 2d = Digital volume control is set to -99.5 dB 3d to 200d = Digital volume control is set as per configuration 201d = Digital volume control is set to 0 dB 202d = Digital volume control is set to 0.5 dB 203d to 253d = Digital volume control is set as per configuration 254d = Digital volume control is set to 26.5 dB 255d = Digital volume control is set to 27 dB

8.6.1.3.63 CH4_CFG3 Register (page = 0x00, address = 0x4E) [reset = 80h]

This register is configuration register 3 for channel 4.

Figure 158. CH4_CFG3 Register

7	6	5	4	3	2	1	0
CH4_GCAL[3:0]				Reserved			
RW-8h				R-0h			

Table 114. CH4_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	CH4_GCAL[3:0]	RW	8h	Channel 4 gain calibration. 0d = Gain calibration is set to -0.8 dB 1d = Gain calibration is set to -0.7 dB 2d = Gain calibration is set to -0.6 dB 3d to 7d = Gain calibration is set as per configuration 8d = Gain calibration is set to 0 dB 9d = Gain calibration is set to 0.1 dB 10d to 13d = Gain calibration is set as per configuration 14d = Gain calibration is set to 0.6 dB 15d = Gain calibration is set to 0.7 dB
3-0	Reserved	R	0h	Reserved

8.6.1.3.64 CH4_CFG4 Register (page = 0x00, address = 0x4F) [reset = 0h]

This register is configuration register 4 for channel 4.

Figure 159. CH4_CFG4 Register

7	6	5	4	3	2	1	0
CH4_PCAL[7:0]							
RW-0h							

Table 115. CH4_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH4_PCAL[7:0]	RW	0h	Channel 4 phase calibration with modulator clock resolution. 0d = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock

8.6.1.3.65 CH5_CFG0 Register (page = 0x00, address = 0x50) [reset = 10h]

This register is configuration register 0 for channel 5.

Figure 160. CH5_CFG0 Register

7	6	5	4	3	2	1	0
CH5_INTYP	CH5_INSRC[1:0]		CH5_DC	CH5_MIC_IN_RANGE	CH5_PGA_CFG[1:0]		CH5_AGCEN
RW-0h	RW-0h		RW-1h	RW-0h	RW-0h		RW-0h

Table 116. CH5_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH5_INTYP	RW	0h	Channel 5 input type. 0d = Microphone input 1d = Line input
6-5	CH5_INSRC[1:0]	RW	0h	Channel 5 input configuration. 0d = Analog differential input 1d = Analog single-ended input 2d = Reserved
4	CH5_DC	RW	1h	Channel 5 input coupling. 0d = AC-coupled input 1d = DC-coupled input

Table 116. CH5_CFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CH5_MIC_IN_RANGE	RW	0h	Channel 5 microphone input range. 0d = Low swing mode; Differential input AC signal full-scale of 2-V_{RMS} supported provided DC differential common mode voltage IN1P - IN1M < 4.2 V. Single-ended AC signal 1-V_{RMS} supported provided DC common mode voltage is < 2.1 V. 1d = High swing mode; Differential Input IN1P-IN1M peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the channel gain and digital volume control based on the max signal level used in system.
2-1	CH5_PGA_CFG[1:0]	RW	0h	Channel 5 CMRR Configuration. 0d = High SNR performance mode 1d = Reserved 2d = High CMRR performance mode 3d = Reserved
0	CH5_AGCEN	RW	0h	Channel 5 automatic gain controller (AGC) setting. 0d = AGC disabled 1d = AGC enabled based on the configuration of bit 3 in register 108 (P0_R108); This must be used only with AC-coupled input

8.6.1.3.66 CH5_CFG1 Register (page = 0x00, address = 0x51) [reset = 0h]

This register is configuration register 1 for channel 5. Applicable only for PCM6x60-Q1.

Figure 161. CH5_CFG1 Register

7	6	5	4	3	2	1	0
CH5_GAIN[5:0]						Reserved	Reserved
RW-0h						RW-0h	R-0h

Table 117. CH5_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	CH5_GAIN[5:0]	RW	0h	Channel 5 gain. 0d = Channel gain is set to 0 dB 1d = Channel gain is set to 1 dB 2d = Channel gain is set to 2 dB 3d to 41d = Channel gain is set as per configuration 42d = Channel gain is set to 42 dB 43d to 63d = Reserved
1	Reserved	RW	0h	Reserved
0	Reserved	R	0h	Reserved

8.6.1.3.67 CH5_CFG2 Register (page = 0x00, address = 0x52) [reset = C9h]

This register is configuration register 2 for channel 5. Applicable only for PCM6x60-Q1.

Figure 162. CH5_CFG2 Register

7	6	5	4	3	2	1	0
CH5_DVOL[7:0]							
RW-C9h							

Table 118. CH5_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH5_DVOL[7:0]	RW	C9h	Channel 5 digital volume control. 0d = Digital volume is muted 1d = Digital volume control is set to -100 dB 2d = Digital volume control is set to -99.5 dB 3d to 200d = Digital volume control is set as per configuration 201d = Digital volume control is set to 0 dB 202d = Digital volume control is set to 0.5 dB 203d to 253d = Digital volume control is set as per configuration 254d = Digital volume control is set to 26.5 dB 255d = Digital volume control is set to 27 dB

8.6.1.3.68 CH5_CFG3 Register (page = 0x00, address = 0x53) [reset = 80h]

This register is configuration register 3 for channel 5. Applicable only for PCM6x60-Q1.

Figure 163. CH5_CFG3 Register

7	6	5	4	3	2	1	0
CH5_GCAL[3:0]				Reserved			
RW-8h				R-0h			

Table 119. CH5_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	CH5_GCAL[3:0]	RW	8h	Channel 5 gain calibration. 0d = Gain calibration is set to -0.8 dB 1d = Gain calibration is set to -0.7 dB 2d = Gain calibration is set to -0.6 dB 3d to 7d = Gain calibration is set as per configuration 8d = Gain calibration is set to 0 dB 9d = Gain calibration is set to 0.1 dB 10d to 13d = Gain calibration is set as per configuration 14d = Gain calibration is set to 0.6 dB 15d = Gain calibration is set to 0.7 dB
3-0	Reserved	R	0h	Reserved

8.6.1.3.69 CH5_CFG4 Register (page = 0x00, address = 0x54) [reset = 0h]

This register is configuration register 4 for channel 5. Applicable only for PCM6x60-Q1.

Figure 164. CH5_CFG4 Register

7	6	5	4	3	2	1	0
CH5_PCAL[7:0]							
RW-0h							

Table 120. CH5_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH5_PCAL[7:0]	RW	0h	Channel 5 phase calibration with modulator clock resolution. 0d = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock

8.6.1.3.70 CH6_CFG0 Register (page = 0x00, address = 0x55) [reset = 10h]

This register is configuration register 0 for channel 6.

Figure 165. CH6_CFG0 Register

7	6	5	4	3	2	1	0
CH6_INTYP	CH6_INSRC[1:0]		CH6_DC	CH6_MIC_IN_RANGE	CH6_PGA_CFG[1:0]		CH6_AGCEN
RW-0h	RW-0h		RW-1h	RW-0h	RW-0h		RW-0h

Table 121. CH6_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH6_INTYP	RW	0h	Channel 6 input type. 0d = Microphone input 1d = Line input
6-5	CH6_INSRC[1:0]	RW	0h	Channel 6 input configuration. 0d = Analog differential input 1d = Analog single-ended input 2d = Reserved
4	CH6_DC	RW	1h	Channel 6 input coupling. 0d = AC-coupled input 1d = DC-coupled input
3	CH6_MIC_IN_RANGE	RW	0h	Channel 6 microphone input range. 0d = Low swing mode; Differential input AC signal full-scale of 2-V_{RMS} supported provided DC differential common mode voltage IN1P - IN1M < 4.2 V. Single-ended AC signal 1-V_{RMS} supported provided DC common mode voltage is < 2.1 V. 1d = High swing mode; Differential Input IN1P-IN1M peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the channel gain and digital volume control based on the max signal level used in system.
2-1	CH6_PGA_CFG[1:0]	RW	0h	Channel 6 CMRR Configuration. 0d = High SNR performance mode 1d = Reserved 2d = High CMRR performance mode 3d = Reserved
0	CH6_AGCEN	RW	0h	Channel 6 automatic gain controller (AGC) setting. 0d = AGC disabled 1d = AGC enabled based on the configuration of bit 3 in register 108 (P0_R108); This must be used only with AC-coupled input

8.6.1.3.71 CH6_CFG1 Register (page = 0x00, address = 0x56) [reset = 0h]

This register is configuration register 1 for channel 6. Applicable only for PCM6x60-Q1.

Figure 166. CH6_CFG1 Register

7	6	5	4	3	2	1	0
CH6_GAIN[5:0]						Reserved	Reserved
RW-0h						RW-0h	R-0h

Table 122. CH6_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	CH6_GAIN[5:0]	RW	0h	Channel 6 gain. 0d = Channel gain is set to 0 dB 1d = Channel gain is set to 1 dB 2d = Channel gain is set to 2 dB 3d to 41d = Channel gain is set as per configuration 42d = Channel gain is set to 42 dB 43d to 63d = Reserved
1	Reserved	RW	0h	Reserved
0	Reserved	R	0h	Reserved

8.6.1.3.72 CH6_CFG2 Register (page = 0x00, address = 0x57) [reset = C9h]

This register is configuration register 2 for channel 6. Applicable only for PCM6x60-Q1.

Figure 167. CH6_CFG2 Register

7	6	5	4	3	2	1	0
CH6_DVOL[7:0]							
RW-C9h							

Table 123. CH6_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH6_DVOL[7:0]	RW	C9h	Channel 6 digital volume control. 0d = Digital volume is muted 1d = Digital volume control is set to -100 dB 2d = Digital volume control is set to -99.5 dB 3d to 200d = Digital volume control is set as per configuration 201d = Digital volume control is set to 0 dB 202d = Digital volume control is set to 0.5 dB 203d to 253d = Digital volume control is set as per configuration 254d = Digital volume control is set to 26.5 dB 255d = Digital volume control is set to 27 dB

8.6.1.3.73 CH6_CFG3 Register (page = 0x00, address = 0x58) [reset = 80h]

This register is configuration register 3 for channel 6. Applicable only for PCM6x60-Q1.

Figure 168. CH6_CFG3 Register

7	6	5	4	3	2	1	0
CH6_GCAL[3:0]				Reserved			
RW-8h				R-0h			

Table 124. CH6_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	CH6_GCAL[3:0]	RW	8h	Channel 6 gain calibration. 0d = Gain calibration is set to -0.8 dB 1d = Gain calibration is set to -0.7 dB 2d = Gain calibration is set to -0.6 dB 3d to 7d = Gain calibration is set as per configuration 8d = Gain calibration is set to 0 dB 9d = Gain calibration is set to 0.1 dB 10d to 13d = Gain calibration is set as per configuration 14d = Gain calibration is set to 0.6 dB 15d = Gain calibration is set to 0.7 dB
3-0	Reserved	R	0h	Reserved

8.6.1.3.74 CH6_CFG4 Register (page = 0x00, address = 0x59) [reset = 0h]

This register is configuration register 4 for channel 6. Applicable only for PCM6x60-Q1.

Figure 169. CH6_CFG4 Register

7	6	5	4	3	2	1	0
CH6_PCAL[7:0]							
RW-0h							

Table 125. CH6_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH6_PCAL[7:0]	RW	0h	Channel 6 phase calibration with modulator clock resolution. 0d = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock

8.6.1.3.75 DIAG_CFG0 Register (page = 0x00, address = 0x64) [reset = 0h]

This register is configuration register 0 for input fault diagnostics setting.

Figure 170. DIAG_CFG0 Register

7	6	5	4	3	2	1	0
CH1_DIAG_EN	CH2_DIAG_EN	CH3_DIAG_EN	CH4_DIAG_EN	CH5_DIAG_EN	CH6_DIAG_EN	INCL_SE_INM	INCL_AC_COUP
RW-0h	RW-0h	RW-0h	RW-0h	RW-0h	RW-0h	RW-0h	RW-0h

Table 126. DIAG_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH1_DIAG_EN	RW	0h	Channel 1 input (IN1P and IN1M) scan for diagnostics. 0d = Diagnostic disabled 1d = Diagnostic enabled
6	CH2_DIAG_EN	RW	0h	Channel 2 input (IN2P and IN2M) scan for diagnostics. 0d = Diagnostic disabled 1d = Diagnostic enabled
5	CH3_DIAG_EN	RW	0h	Channel 3 input (IN3P and IN3M) scan for diagnostics. 0d = Diagnostic disabled 1d = Diagnostic enabled
4	CH4_DIAG_EN	RW	0h	Channel 4 input (IN4P and IN4M) scan for diagnostics. 0d = Diagnostic disabled 1d = Diagnostic enabled
3	CH5_DIAG_EN	RW	0h	Channel 5 input (IN5P and IN5M) scan for diagnostics. Applicable only for PCM6x60-Q1. 0d = Diagnostic disabled 1d = Diagnostic enabled
2	CH6_DIAG_EN	RW	0h	Channel 6 input (IN6P and IN6M) scan for diagnostics. Applicable only for PCM6x60-Q1. 0d = Diagnostic disabled 1d = Diagnostic enabled
1	INCL_SE_INM	RW	0h	INxM pin diagnostics scan selection for single-ended configuration. 0d = INxM pins of single-ended channels are excluded for diagnosis 1d = INxM pins of single-ended channels are included for diagnosis
0	INCL_AC_COUP	RW	0h	AC-coupled channels pins scan selection for diagnostics. 0d = INxP and INxM pins of AC-coupled channels are excluded for diagnosis 1d = INxP and INxM pins of AC-coupled channels are included for diagnosis

8.6.1.3.76 DIAG_CFG1 Register (page = 0x00, address = 0x65) [reset = 37h]

This register is configuration register 1 for input fault diagnostics setting.

Figure 171. DIAG_CFG1 Register

7	6	5	4	3	2	1	0
DIAG_SHT_TERM[3:0]				DIAG_SHT_VBAT_IN[3:0]			
RW-3h				RW-7h			

Table 127. DIAG_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_SHT_TERM[3:0]	RW	3h	INxP and INxM terminal short detect threshold. 0d = INxP and INxM terminal short detect threshold value is 0 mV (typ) 1d = INxP and INxM terminal short detect threshold value is 30 mV (typ) 2d = INxP and INxM terminal short detect threshold value is 60 mV (typ) 10d to 13d = INxP and INxM terminal short detect threshold value is set as per configuration 14d = INxP and INxM terminal short detect threshold value is 420 mV (typ) 15d = INxP and INxM terminal short detect threshold value is 450 mV (typ)
3-0	DIAG_SHT_VBAT_IN[3:0]	RW	7h	Short to VBAT_IN detect threshold. 0d = Short to VBAT_IN detect threshold value is 0 mV (typ) 1d = Short to VBAT_IN detect threshold value is 30 mV (typ) 2d = Short to VBAT_IN detect threshold value is 60 mV (typ) 10d to 13d = Short to VBAT_IN detect threshold value is set as per configuration 14d = Short to VBAT_IN detect threshold value is 420 mV (typ) 15d = Short to VBAT_IN detect threshold value is 450 mV (typ)

8.6.1.3.77 DIAG_CFG2 Register (page = 0x00, address = 0x66) [reset = 87h]

This register is configuration register 2 for input fault diagnostics setting.

Figure 172. DIAG_CFG2 Register

7	6	5	4	3	2	1	0
DIAG_SHT_GND[3:0]				DIAG_SHT_MICBIAS[3:0]			
RW-8h				RW-7h			

Table 128. DIAG_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_SHT_GND[3:0]	RW	8h	Short to ground detect threshold. 0d = Short to ground detect threshold value is 0 mV (typ) 1d = Short to ground detect threshold value is 60 mV (typ) 2d = Short to ground detect threshold value is 120 mV (typ) 10d to 13d = Short to ground detect threshold value is set as per configuration 14d = Short to ground detect threshold value is 840 mV (typ) 15d = Short to ground detect threshold value is 900 mV (typ)
3-0	DIAG_SHT_MICBIAS[3:0]	RW	7h	Short to MICBIAS detect threshold. 0d = Short to MICBIAS detect threshold value is 0 mV (typ) 1d = Short to MICBIAS detect threshold value is 30 mV (typ) 2d = Short to MICBIAS detect threshold value is 60 mV (typ) 10d to 13d = Short to MICBIAS detect threshold value is set as per configuration 14d = Short to MICBIAS detect threshold value is 420 mV (typ) 15d = Short to MICBIAS detect threshold value is 450 mV (typ)

8.6.1.3.78 DIAG_CFG3 Register (page = 0x00, address = 0x67) [reset = B8h]

This register is configuration register 3 for input fault diagnostics setting.

Figure 173. DIAG_CFG3 Register

7	6	5	4	3	2	1	0
REP_RATE[1:0]		Reserved		FAULT_DBNCE_SEL[1:0]		VSHORT_DBNCE	DIAG_2X_THRES
RW-2h		RW-3h		RW-2h		RW-0h	RW-0h

Table 129. DIAG_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	REP_RATE[1:0]	RW	2h	Fault monitoring scan repetition rate. 0d = Continuos back to back scanning of selected channels input pins without any idle time 1d = Fault monitoring repetition rate of 1 ms for selected channels input pins scanning 2d = Fault monitoring repetition rate of 4 ms for selected channels input pins scanning 3d = Fault monitoring repetition rate of 8 ms for selected channels input pins scanning
5-4	Reserved	RW	3h	Reserved
3-2	FAULT_DBNCE_SEL[1:0]	RW	2h	Debounce count for all the faults (except VBAT_IN short when VBAT_IN < MICBIAS). 0d = 16 counts for debounce to filter-out any false faults detection 1d = 8 counts for debounce to filter-out any false faults detection 2d = 4 counts for debounce to filter-out any false faults detection 3d = No debounce count
1	VSHORT_DBNCE	RW	0h	VBAT_IN short debounce count only when VBAT_IN < MICBIAS. 0d = 16 counts for debounce to filter-out any false faults detection 1d = 8 counts for debounce to filter-out any false faults detection
0	DIAG_2X_THRES	RW	0h	Diagnostic thresholds range scale. 0d = Thresholds same as configured in P0_R101 and P0_R102 1d = All the configuration thresholds gets scale by 2 times

8.6.1.3.79 DIAG_CFG4 Register (page = 0x00, address = 0x68) [reset = 0h]

This register is configuration register 4 for input fault diagnostics setting.

Figure 174. DIAG_CFG4 Register

7	6	5	4	3	2	1	0
DIAG_MOV_AVG_CFG[1:0]		MOV_AVG_DIS_MBIAS_LOAD	MOV_AVG_DIS_TEMP_SENS	Reserved			
RW-0h		RW-0h	RW-0h	R-0h			

Table 130. DIAG_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	DIAG_MOV_AVG_CFG[1:0]	RW	0h	Moving average configuration. 0d = Moving average disabled 1d = Moving average enabled with 0.5 weightage for old scanned data and new scanned data 2d = Moving average enabled with 0.75 weightage for old scanned data and 0.25 weightage for new scanned data 3d = Reserved
5	MOV_AVG_DIS_MBIAS_LOAD	RW	0h	Moving average configuration for MICBIAS high and low load current fault detection 0d = Moving average as defined by DIAG_MOV_AVG_CFG setting 1d = Moving average is forced disabled for MICBIAS load current fault detection to achieve faster response time
4	MOV_AVG_DIS_TEMP_SENS	RW	0h	Moving average configuration for over temperature fault detection 0d = Moving average as defined by DIAG_MOV_AVG_CFG setting 1d = Moving average is forced disabled for over temperature fault detection to achieve faster response time
3-0	Reserved	R	0h	Reserved

8.6.1.3.80 DSP_CFG0 Register (page = 0x00, address = 0x6B) [reset = 1h]

This register is the digital signal processor (DSP) configuration register 0.

Figure 175. DSP_CFG0 Register

7	6	5	4	3	2	1	0
Reserved		DECI_FILT[1:0]		CH_SUM[1:0]		HPF_SEL[1:0]	
R-0h		RW-0h		RW-0h		RW-1h	

Table 131. DSP_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R	0h	Reserved
5-4	DECI_FILT[1:0]	RW	0h	Decimation filter response. 0d = Linear phase 1d = Low latency 2d = Ultra-low latency
3-2	CH_SUM[1:0]	RW	0h	Channel summation mode for higher SNR 0d = Channel summation mode is disabled 1d = 2-channel summation mode is enabled to generate a (CH1 + CH2) / 2 and a (CH3 + CH4) / 2 output 2d = 4-channel summation mode is enabled to generate a (CH1 + CH2 + CH3 + CH4) / 4 output 3d = Reserved
1-0	HPF_SEL[1:0]	RW	1h	High-pass filter (HPF) selection. 0d = Programmable first-order IIR filter for a custom HPF with default coefficient values in P4_R72 to P4_R83 set as the all-pass filter 1d = HPF with a cutoff of 0.00025 x f_S (12 Hz at f_S = 48 kHz) is selected 2d = HPF with a cutoff of 0.002 x f_S (96 Hz at f_S = 48 kHz) is selected 3d = HPF with a cutoff of 0.008 x f_S (384 Hz at f_S = 48 kHz) is selected

8.6.1.3.81 DSP_CFG1 Register (page = 0x00, address = 0x6C) [reset = 48h]

This register is the digital signal processor (DSP) configuration register 1.

Figure 176. DSP_CFG1 Register

7	6	5	4	3	2	1	0
DVOL_GANG	BIQUAD_CFG[1:0]		DISABLE_SOFT_STEP	AGC_SEL	Reserved	Reserved	
RW-0h	RW-2h		RW-0h	RW-1h	RW-0h	R-0h	

Table 132. DSP_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DVOL_GANG	RW	0h	DVOL control ganged across channels. 0d = Each channel has its own DVOL CTRL settings as programmed in the CHx_DVOL bits 1d = All active channels must use the channel 1 DVOL setting (CH1_DVOL) irrespective of whether channel 1 is turned on or not
6-5	BIQUAD_CFG[1:0]	RW	2h	Number of biquads per channel configuration. 0d = No biquads per channel; biquads are all disabled 1d = 1 biquad per channel 2d = 2 biquads per channel 3d = 3 biquads per channel
4	DISABLE_SOFT_STEP	RW	0h	Soft-stepping disable during DVOL change, mute, and unmute. 0d = Soft-stepping enabled 1d = Soft-stepping disabled
3	AGC_SEL	RW	1h	AGC master enable setting. 0d = Reserved; Write always 1 to this register bit 1d = AGC selected as configured for each channel using CHx_CFG0 register
2	Reserved	RW	0h	Reserved
1-0	Reserved	R	0h	Reserved

8.6.1.3.82 AGC_CFG0 Register (page = 0x00, address = 0x70) [reset = E7h]

This register is the automatic gain controller (AGC) configuration register 0.

Figure 177. AGC_CFG0 Register

7	6	5	4	3	2	1	0
AGC_LVL[3:0]				AGC_MAXGAIN[3:0]			
RW-Eh				RW-7h			

Table 133. AGC_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	AGC_LVL[3:0]	RW	Eh	AGC output signal target level. 0d = Output signal target level is -6 dB 1d = Output signal target level is -8 dB 2d = Output signal target level is -10 dB 3d to 13d = Output signal target level is as per configuration 14d = Output signal target level is -34 dB 15d = Output signal target level is -36 dB
3-0	AGC_MAXGAIN[3:0]	RW	7h	AGC maximum gain allowed. 0d = Maximum gain allowed is 3 dB 1d = Maximum gain allowed is 6 dB 2d = Maximum gain allowed is 9 dB 3d to 11d = Maximum gain allowed is as per configuration 12d = Maximum gain allowed is 39 dB 13d = Maximum gain allowed is 42 dB 14d to 15d = Reserved

8.6.1.3.83 IN_CH_EN Register (page = 0x00, address = 0x73) [reset = FCh]

This register is the input channel enable configuration register.

Figure 178. IN_CH_EN Register

7	6	5	4	3	2	1	0
IN_CH1_EN	IN_CH2_EN	IN_CH3_EN	IN_CH4_EN	IN_CH5_EN	IN_CH6_EN	Reserved	Reserved
RW-1h	RW-1h	RW-1h	RW-1h	RW-1h	RW-1h	RW-0h	RW-0h

Table 134. IN_CH_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	IN_CH1_EN	RW	1h	Input channel 1 enable setting. 0d = Channel 1 is disabled 1d = Channel 1 is enabled
6	IN_CH2_EN	RW	1h	Input channel 2 enable setting. 0d = Channel 2 is disabled 1d = Channel 2 is enabled
5	IN_CH3_EN	RW	1h	Input channel 3 enable setting. 0d = Channel 3 is disabled 1d = Channel 3 is enabled
4	IN_CH4_EN	RW	1h	Input channel 4 enable setting. 0d = Channel 4 is disabled 1d = Channel 4 is enabled
3	IN_CH5_EN	RW	1h	Input channel 5 enable setting. Applicable only for PCM6x60-Q1. 0d = Channel 5 is disabled 1d = Channel 5 is enabled
2	IN_CH6_EN	RW	1h	Input channel 6 enable setting. Applicable only for PCM6x60-Q1. 0d = Channel 6 is disabled 1d = Channel 6 is enabled
1	Reserved	RW	0h	Reserved
0	Reserved	RW	0h	Reserved

8.6.1.3.84 ASI_OUT_CH_EN Register (page = 0x00, address = 0x74) [reset = 0h]

This register is the ASI output channel enable configuration register.

Figure 179. ASI_OUT_CH_EN Register

7	6	5	4	3	2	1	0
ASI_OUT_CH1_EN	ASI_OUT_CH2_EN	ASI_OUT_CH3_EN	ASI_OUT_CH4_EN	ASI_OUT_CH5_EN	ASI_OUT_CH6_EN	Reserved	Reserved
RW-0h	RW-0h	RW-0h	RW-0h	RW-0h	RW-0h	RW-0h	RW-0h

Table 135. ASI_OUT_CH_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ASI_OUT_CH1_EN	RW	0h	ASI output channel 1 enable setting. 0d = Channel 1 output slot is in a tri-state condition 1d = Channel 1 output slot is enabled
6	ASI_OUT_CH2_EN	RW	0h	ASI output channel 2 enable setting. 0d = Channel 2 output slot is in a tri-state condition 1d = Channel 2 output slot is enabled
5	ASI_OUT_CH3_EN	RW	0h	ASI output channel 3 enable setting. 0d = Channel 3 output slot is in a tri-state condition 1d = Channel 3 output slot is enabled
4	ASI_OUT_CH4_EN	RW	0h	ASI output channel 4 enable setting. 0d = Channel 4 output slot is in a tri-state condition 1d = Channel 4 output slot is enabled
3	ASI_OUT_CH5_EN	RW	0h	ASI output channel 5 enable setting. Applicable only for PCM6x60-Q1. 0d = Channel 5 output slot is in a tri-state condition 1d = Channel 5 output slot is enabled
2	ASI_OUT_CH6_EN	RW	0h	ASI output channel 6 enable setting. Applicable only for PCM6x60-Q1. 0d = Channel 6 output slot is in a tri-state condition 1d = Channel 6 output slot is enabled
1	Reserved	RW	0h	Reserved
0	Reserved	RW	0h	Reserved

8.6.1.3.85 PWR_CFG Register (page = 0x00, address = 0x75) [reset = 0h]

This register is the power-up configuration register.

Figure 180. PWR_CFG Register

7	6	5	4	3	2	1	0
MICBIAS_PDZ	ADC_PDZ	PLL_PDZ	DYN_CH_PUPD_EN	DYN_MAXCH_SEL[1:0]		Reserved	Reserved
RW-0h	RW-0h	RW-0h	RW-0h	RW-0h		RW-0h	R-0h

Table 136. PWR_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MICBIAS_PDZ	RW	0h	Power control for MICBIAS. 0d = Power down MICBIAS 1d = Power up MICBIAS
6	ADC_PDZ	RW	0h	Power control for ADC channels. 0d = Power down all ADC channels 1d = Power up all enabled ADC channels
5	PLL_PDZ	RW	0h	Power control for the PLL. 0d = Power down the PLL 1d = Power up the PLL
4	DYN_CH_PUPD_EN	RW	0h	Dynamic channel power-up, power-down enable. 0d = Channel power-up, power-down is not supported if any channel recording is on 1d = Channel can be powered up or down individually, even if channel recording is on. Do not powered-down channel 1 if this bit is set to '1'

Table 136. PWR_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	DYN_MAXCH_SEL[1:0]	RW	0h	Dynamic mode maximum channel select configuration. 0d = Channel 1 and channel 2 are used with dynamic channel power-up, power-down feature enabled 1d = Channel 1 to channel 4 are used with dynamic channel power-up, power-down feature enabled 2d = Channel 1 to channel 6 are used with dynamic channel power-up, power-down feature enabled
1	Reserved	RW	0h	Reserved
0	Reserved	R	0h	Reserved

8.6.1.3.86 DEV_STS0 Register (page = 0x00, address = 0x76) [reset = 0h]

This register is the device status value register 0.

Figure 181. DEV_STS0 Register

7	6	5	4	3	2	1	0
CH1_STATUS	CH2_STATUS	CH3_STATUS	CH4_STATUS	CH5_STATUS	CH6_STATUS	Reserved	Reserved
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 137. DEV_STS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH1_STATUS	R	0h	ADC channel 1 power status. 0d = ADC channel is powered down 1d = ADC channel is powered up
6	CH2_STATUS	R	0h	ADC channel 2 power status. 0d = ADC channel is powered down 1d = ADC channel is powered up
5	CH3_STATUS	R	0h	ADC channel 3 power status. 0d = ADC channel is powered down 1d = ADC channel is powered up
4	CH4_STATUS	R	0h	ADC channel 4 power status. 0d = ADC channel is powered down 1d = ADC channel is powered up
3	CH5_STATUS	R	0h	ADC channel 5 power status. Applicable only for PCM6x60-Q1. 0d = ADC channel is powered down 1d = ADC channel is powered up
2	CH6_STATUS	R	0h	ADC channel 6 power status. Applicable only for PCM6x60-Q1. 0d = ADC channel is powered down 1d = ADC channel is powered up
1	Reserved	R	0h	Reserved
0	Reserved	R	0h	Reserved

8.6.1.3.87 DEV_STS1 Register (page = 0x00, address = 0x77) [reset = 80h]

This register is the device status value register 1.

Figure 182. DEV_STS1 Register

7	6	5	4	3	2	1	0
MODE_STS[2:0]			BOOST_STS	MBIAS_STS	CHx_PD_FLT_STS	ALL_CHx_PD_FLT_STS	MAN_RCV_PD_FLT_CHK
R-4h			R-0h	R-0h	R-0h	R-0h	RW-0h

Table 138. DEV_STS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	MODE_STS[2:0]	R	4h	Device mode status. 4d = Device is in sleep mode or software shutdown mode 6d = Device is in active mode with all ADC channels turned off 7d = Device is in active mode with at least one ADC channel turned on
4	BOOST_STS	R	0h	Boost power up status. 0d = Boost is powered down 1d = Boost is powered up
3	MBIAS_STS	R	0h	MICBIAS power up status. 0d = MICBIAS is powered down 1d = MICBIAS is powered up
2	CHx_PD_FLT_STS	R	0h	ADC channel power down status caused by INxx inputs faults. 0d = No ADC channel is powered down caused by INxx inputs faults 1d = Atleast a ADC channel is powered down caused by INxx inputs faults
1	ALL_CHx_PD_FLT_STS	R	0h	ADC channel power down status caused by MICBIAS faults. 0d = No ADC channel is powered down caused by MICBIAS faults 1d = All ADC channels are powered down caused by MICBIAS faults
0	MAN_RCV_PD_FLT_CHK	RW	0h	Manual recovery (self-clearing bit). 0d = No effect 1d = Recheck all fault status and re-powerup ADC channels and/or MICBIAS if they do not have any faults. Before setting this bit, reset P0_R58 register and re-configure P0_R58 to desired setting only after manual recover gets over.

8.6.1.3.88 I2C_CKSUM Register (page = 0x00, address = 0x7E) [reset = 0h]

This register returns the I^2C transactions checksum value.

Figure 183. I2C_CKSUM Register

7	6	5	4	3	2	1	0
I2C_CKSUM[7:0]							
R/W-0h							

Table 139. I2C_CKSUM Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	I2C_CKSUM[7:0]	R/W	0h	These bits return the I^2C transactions checksum value. Writing to this register resets the checksum to the written value. This register is updated on writes to other registers on all pages.

8.6.1.4 Register Description: Page = 0x01

8.6.1.4.1 PAGE_CFG Register (page = 0x01, address = 0x00) [reset = 0h]

The device memory map is divided into pages. This register sets the page.

Figure 184. PAGE_CFG Register

7	6	5	4	3	2	1	0
PAGE[7:0]							
RW-0h							

Table 140. PAGE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PAGE[7:0]	RW	0h	These bits set the device page. 0d = Page 0 1d = Page 1 ... 255d = Page 255

8.6.1.4.2 MBIAS_LOAD Register (page = 0x01, address = 0x16) [reset = 0h]

This register is the MICBIAS internal load sink configuration register.

Figure 185. MBIAS_LOAD Register

7	6	5	4	3	2	1	0
MICBIAS_INT_LOAD_SINK_EN	MICBIAS_INT_LOAD_SINK_VAL[2:0]			Reserved			
RW-0h	RW-0h			R-0h			

Table 141. MBIAS_LOAD Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MICBIAS_INT_LOAD_SINK_EN	RW	0h	MICBIAS internal load sink setting. 0d = MICBIAS internal load sink is enabled with setting automatically calculated based on device configuration 1d = MICBIAS internal load sink is enabled based on D6-4 register bits; This setting must be used for single-ended AC-coupled input to support high signal swing
6-4	MICBIAS_INT_LOAD_SINK_VAL[2:0]	RW	0h	MICBIAS internal load sink current value 0d = MICBIAS internal load sink current is set to 0 mA (typ) 1d = MICBIAS internal load sink current is set to 4.3 mA (typ) 2d = MICBIAS internal load sink current is set to 8.6 mA (typ) 3d = MICBIAS internal load sink current is set to 12.9 mA (typ) 4d = MICBIAS internal load sink current is set to 17.2 mA (typ) 5d = MICBIAS internal load sink current is set to 21.5 mA (typ) 6d = MICBIAS internal load sink current is set to 25.8 mA (typ) 7d = MICBIAS internal load sink current is set to 30.1 mA (typ)
3-0	Reserved	R	0h	Reserved

8.6.1.4.3 INT_LIVE0 Register (page = 0x01, address = 0x2C) [reset = 0h]

This register is the live Interrupt readback register 0.

Figure 186. INT_LIVE0 Register

7	6	5	4	3	2	1	0
INT_LIVE0[7]	INT_LIVE0[6]	INT_LIVE0[5]	INT_LIVE0[4]	Reserved	Reserved	Reserved	Reserved
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 142. INT_LIVE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LIVE0[7]	R	0h	Fault status for an ASI bus clock error. 0d = No fault detected 1d = Fault detected
6	INT_LIVE0[6]	R	0h	Status of PLL lock. 0d = No PLL lock detected 1d = PLL lock detected
5	INT_LIVE0[5]	R	0h	Fault status for boost or MICBIAS over temperature. 0d = No fault detected 1d = Fault detected
4	INT_LIVE0[4]	R	0h	Fault status for boost or MICBIAS over current. 0d = No fault detected 1d = Fault detected
3	Reserved	R	0h	Reserved
2	Reserved	R	0h	Reserved
1	Reserved	R	0h	Reserved
0	Reserved	R	0h	Reserved

8.6.1.4.4 CHx_LIVE Register (page = 0x01, address = 0x2D) [reset = 0h]

This register is the live Interrupt status register for channel level diagnostic summary.

Figure 187. CHx_LIVE Register

7	6	5	4	3	2	1	0
STS_CHx_LIVE[7]	STS_CHx_LIVE[6]	STS_CHx_LIVE[5]	STS_CHx_LIVE[4]	STS_CHx_LIVE[3]	STS_CHx_LIVE[2]	STS_CHx_LIVE[1]	Reserved
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 143. CHx_LIVE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	STS_CHx_LIVE[7]	R	0h	Status of CH1_LIVE. 0d = No faults occurred in channel 1 1d = Atleast a fault has occurred in channel 1
6	STS_CHx_LIVE[6]	R	0h	Status of CH2_LIVE. 0d = No faults occurred in channel 2 1d = Atleast a fault has occurred in channel 2
5	STS_CHx_LIVE[5]	R	0h	Status of CH3_LIVE. 0d = No faults occurred in channel 3 1d = Atleast a fault has occurred in channel 3
4	STS_CHx_LIVE[4]	R	0h	Status of CH4_LIVE. 0d = No faults occurred in channel 4 1d = Atleast a fault has occurred in channel 4
3	STS_CHx_LIVE[3]	R	0h	Status of CH5_LIVE. Applicable only for PCM6x60-Q1. 0d = No faults occurred in channel 5 1d = Atleast a fault has occurred in channel 5
2	STS_CHx_LIVE[2]	R	0h	Status of CH6_LIVE. Applicable only for PCM6x60-Q1. 0d = No faults occurred in channel 6 1d = Atleast a fault has occurred in channel 6
1	STS_CHx_LIVE[1]	R	0h	Status of short to VBAT_IN fault detected when VBAT_IN is less than MICBIAS. 0d = Short to VBAT_IN fault when VBAT_IN is less than MICBIAS has not occurred in any channel 1d = Short to VBAT_IN fault when VBAT_IN is less than MICBIAS has occurred in atleast one channel
0	Reserved	R	0h	Reserved

8.6.1.4.5 CH1_LIVE Register (page = 0x01, address = 0x2E) [reset = 0h]

This register is the live Interrupt status register for channel 1 fault diagnostic

Figure 188. CH1_LIVE Register

7	6	5	4	3	2	1	0
CH1_LIVE[7]	CH1_LIVE[6]	CH1_LIVE[5]	CH1_LIVE[4]	CH1_LIVE[3]	CH1_LIVE[2]	CH1_LIVE[1]	CH1_LIVE[0]
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 144. CH1_LIVE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH1_LIVE[7]	R	0h	Channel 1 open input fault status. 0d = No open input detected 1d = Open input detected
6	CH1_LIVE[6]	R	0h	Channel 1 input pair short fault status. 0d = No input pair short detected 1d = Input short to each other detected
5	CH1_LIVE[5]	R	0h	Channel 1 IN1P short to ground fault status. 0d = IN1P no short to ground detected 1d = IN1P short to ground detected
4	CH1_LIVE[4]	R	0h	Channel 1 IN1M short to ground fault status. 0d = IN1M no short to ground detected 1d = IN1M short to ground detected

Table 144. CH1_LIVE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CH1_LIVE[3]	R	0h	Channel 1 IN1P short to MICBIAS fault status. 0d = IN1P no short to MICBIAS detected 1d = IN1P short to MICBIAS detected
2	CH1_LIVE[2]	R	0h	Channel 1 IN1M short to MICBIAS fault status. 0d = IN1M no short to MICBIAS detected 1d = IN1M short to MICBIAS detected
1	CH1_LIVE[1]	R	0h	Channel 1 IN1P short to VBAT_IN fault status. 0d = IN1P no short to VBAT_IN detected 1d = IN1P short to VBAT_IN detected
0	CH1_LIVE[0]	R	0h	Channel 1 IN1M short to VBAT_IN fault status. 0d = IN1M no short to VBAT_IN detected 1d = IN1M short to VBAT_IN detected

8.6.1.4.6 CH2_LIVE Register (page = 0x01, address = 0x2F) [reset = 0h]

This register is the live Interrupt status register for channel 2 fault diagnostic.

Figure 189. CH2_LIVE Register

7	6	5	4	3	2	1	0
CH2_LIVE[7]	CH2_LIVE[6]	CH2_LIVE[5]	CH2_LIVE[4]	CH2_LIVE[3]	CH2_LIVE[2]	CH2_LIVE[1]	CH2_LIVE[0]
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 145. CH2_LIVE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH2_LIVE[7]	R	0h	Channel 2 open input fault status. 0d = No open input detected 1d = Open input detected
6	CH2_LIVE[6]	R	0h	Channel 2 input pair short fault status. 0d = No input pair short detected 1d = Input short to each other detected
5	CH2_LIVE[5]	R	0h	Channel 2 IN2P short to ground fault status. 0d = IN2P no short to ground detected 1d = IN2P short to ground detected
4	CH2_LIVE[4]	R	0h	Channel 2 IN2M short to ground fault status. 0d = IN2M no short to ground detected 1d = IN2M short to ground detected
3	CH2_LIVE[3]	R	0h	Channel 2 IN2P short to MICBIAS fault status. 0d = IN2P no short to MICBIAS detected 1d = IN2P short to MICBIAS detected
2	CH2_LIVE[2]	R	0h	Channel 2 IN2M short to MICBIAS fault status. 0d = IN2M no short to MICBIAS detected 1d = IN2M short to MICBIAS detected
1	CH2_LIVE[1]	R	0h	Channel 2 IN2P short to VBAT_IN fault status. 0d = IN2P no short to VBAT_IN detected 1d = IN2P short to VBAT_IN detected
0	CH2_LIVE[0]	R	0h	Channel 2 IN2M short to VBAT_IN fault status. 0d = IN2M no short to VBAT_IN detected 1d = IN2M short to VBAT_IN detected

8.6.1.4.7 CH3_LIVE Register (page = 0x01, address = 0x30) [reset = 0h]

This register is the live Interrupt status register for channel3 fault diagnostic

Figure 190. CH3_LIVE Register

7	6	5	4	3	2	1	0
CH3_LIVE[7]	CH3_LIVE[6]	CH3_LIVE[5]	CH3_LIVE[4]	CH3_LIVE[3]	CH3_LIVE[2]	CH3_LIVE[1]	CH3_LIVE[0]
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 146. CH3_LIVE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH3_LIVE[7]	R	0h	Channel 3 open input fault status. 0d = No open input detected 1d = Open input detected
6	CH3_LIVE[6]	R	0h	Channel 3 input pair short fault status. 0d = No input pair short detected 1d = Input short to each other detected
5	CH3_LIVE[5]	R	0h	Channel 3 IN3P short to ground fault status. 0d = IN3P no short to ground detected 1d = IN3P short to ground detected
4	CH3_LIVE[4]	R	0h	Channel 3 IN3M short to ground fault status. 0d = IN3M no short to ground detected 1d = IN3M short to ground detected
3	CH3_LIVE[3]	R	0h	Channel 3 IN3P short to MICBIAS fault status. 0d = IN3P no short to MICBIAS detected 1d = IN3P short to MICBIAS detected
2	CH3_LIVE[2]	R	0h	Channel 3 IN3M short to MICBIAS fault status. 0d = IN3M no short to MICBIAS detected 1d = IN3M short to MICBIAS detected
1	CH3_LIVE[1]	R	0h	Channel 3 IN3P short to VBAT_IN fault status. 0d = IN3P no short to VBAT_IN detected 1d = IN3P short to VBAT_IN detected
0	CH3_LIVE[0]	R	0h	Channel 3 IN3M short to VBAT_IN fault status. 0d = IN3M no short to VBAT_IN detected 1d = IN3M short to VBAT_IN detected

8.6.1.4.8 CH4_LIVE Register (page = 0x01, address = 0x31) [reset = 0h]

This register is the live Interrupt status register for channel 4 fault diagnostic.

Figure 191. CH4_LIVE Register

7	6	5	4	3	2	1	0
CH4_LIVE[7]	CH4_LIVE[6]	CH4_LIVE[5]	CH4_LIVE[4]	CH4_LIVE[3]	CH4_LIVE[2]	CH4_LIVE[1]	CH4_LIVE[0]
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 147. CH4_LIVE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH4_LIVE[7]	R	0h	Channel 4 open input fault status. 0d = No open input detected 1d = Open input detected
6	CH4_LIVE[6]	R	0h	Channel 4 input pair short fault status. 0d = No input pair short detected 1d = Input short to each other detected
5	CH4_LIVE[5]	R	0h	Channel 4 IN4P short to ground fault status. 0d = IN4P no short to ground detected 1d = IN4P short to ground detected
4	CH4_LIVE[4]	R	0h	Channel 4 IN4M short to ground fault status. 0d = IN4M no short to ground detected 1d = IN4M short to ground detected
3	CH4_LIVE[3]	R	0h	Channel 4 IN4P short to MICBIAS fault status. 0d = IN4P no short to MICBIAS detected 1d = IN4P short to MICBIAS detected
2	CH4_LIVE[2]	R	0h	Channel 4 IN4M short to MICBIAS fault status. 0d = IN4M no short to MICBIAS detected 1d = IN4M short to MICBIAS detected
1	CH4_LIVE[1]	R	0h	Channel 4 IN4P short to VBAT_IN fault status. 0d = IN4P no short to VBAT_IN detected 1d = IN4P short to VBAT_IN detected

Table 147. CH4_LIVE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CH4_LIVE[0]	R	0h	Channel 4 IN4M short to VBAT_IN fault status. 0d = IN4M no short to VBAT_IN detected 1d = IN4M short to VBAT_IN detected

8.6.1.4.9 CH5_LIVE Register (page = 0x01, address = 0x32) [reset = 0h]

This register is the live Interrupt status register for channel 5 fault diagnostic. Applicable only for PCM6x60-Q1.

Figure 192. CH5_LIVE Register

7	6	5	4	3	2	1	0
CH5_LIVE[7]	CH5_LIVE[6]	CH5_LIVE[5]	CH5_LIVE[4]	CH5_LIVE[3]	CH5_LIVE[2]	CH5_LIVE[1]	CH5_LIVE[0]
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 148. CH5_LIVE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH5_LIVE[7]	R	0h	Channel 5 open input fault status. 0d = No open input detected 1d = Open input detected
6	CH5_LIVE[6]	R	0h	Channel 5 input pair short fault status. 0d = No input pair short detected 1d = Input short to each other detected
5	CH5_LIVE[5]	R	0h	Channel 5 IN5P short to ground fault status. 0d = IN5P no short to ground detected 1d = IN5P short to ground detected
4	CH5_LIVE[4]	R	0h	Channel 5 IN5M short to ground fault status. 0d = IN5M no short to ground detected 1d = IN5M short to ground detected
3	CH5_LIVE[3]	R	0h	Channel 5 IN5P short to MICBIAS fault status. 0d = IN5P no short to MICBIAS detected 1d = IN5P short to MICBIAS detected
2	CH5_LIVE[2]	R	0h	Channel 5 IN5M short to MICBIAS fault status. 0d = IN5M no short to MICBIAS detected 1d = IN5M short to MICBIAS detected
1	CH5_LIVE[1]	R	0h	Channel 5 IN5P short to VBAT_IN fault status. 0d = IN5P no short to VBAT_IN detected 1d = IN5P short to VBAT_IN detected
0	CH5_LIVE[0]	R	0h	Channel 5 IN5M short to VBAT_IN fault status. 0d = IN5M no short to VBAT_IN detected 1d = IN5M short to VBAT_IN detected

8.6.1.4.10 CH6_LIVE Register (page = 0x01, address = 0x33) [reset = 0h]

This register is the live Interrupt status register for channel 6 fault diagnostic. Applicable only for PCM6x60-Q1.

Figure 193. CH6_LIVE Register

7	6	5	4	3	2	1	0
CH6_LIVE[7]	CH6_LIVE[6]	CH6_LIVE[5]	CH6_LIVE[4]	CH6_LIVE[3]	CH6_LIVE[2]	CH6_LIVE[1]	CH6_LIVE[0]
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 149. CH6_LIVE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH6_LIVE[7]	R	0h	Channel 6 open input fault status. 0d = No open input detected 1d = Open input detected

Table 149. CH6_LIVE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	CH6_LIVE[6]	R	0h	Channel 6 input pair short fault status. 0d = No input pair short detected 1d = Input short to each other detected
5	CH6_LIVE[5]	R	0h	Channel 6 IN6P short to ground fault status. 0d = IN6P no short to ground detected 1d = IN6P short to ground detected
4	CH6_LIVE[4]	R	0h	Channel 6 IN6M short to ground fault status. 0d = IN6M no short to ground detected 1d = IN6M short to ground detected
3	CH6_LIVE[3]	R	0h	Channel 6 IN6P short to MICBIAS fault status. 0d = IN6P no short to MICBIAS detected 1d = IN6P short to MICBIAS detected
2	CH6_LIVE[2]	R	0h	Channel 6 IN6M short to MICBIAS fault status. 0d = IN6M no short to MICBIAS detected 1d = IN6M short to MICBIAS detected
1	CH6_LIVE[1]	R	0h	Channel 6 IN6P short to VBAT_IN fault status. 0d = IN6P no short to VBAT_IN detected 1d = IN6P short to VBAT_IN detected
0	CH6_LIVE[0]	R	0h	Channel 6 IN6M short to VBAT_IN fault status. 0d = IN6M no short to VBAT_IN detected 1d = IN6M short to VBAT_IN detected

8.6.1.4.11 INT_LIVE1 Register (page = 0x01, address = 0x35) [reset = 0h]

This register is the live Interrupt readback register 1.

Figure 194. INT_LIVE1 Register

7	6	5	4	3	2	1	0
INT_LIVE1[7]	INT_LIVE1[6]	INT_LIVE1[5]	INT_LIVE1[4]	INT_LIVE1[3]	INT_LIVE1[2]	Reserved	
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	

Table 150. INT_LIVE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LIVE1[7]	R	0h	Channel 1 IN1P over voltage fault status. 0d = No IN1P over voltage fault detected 1d = IN1P over voltage fault has detected
6	INT_LIVE1[6]	R	0h	Channel 2 IN2P over voltage fault status. 0d = No IN2P over voltage fault detected 1d = IN2P over voltage fault has detected
5	INT_LIVE1[5]	R	0h	Channel 3 IN3P over voltage fault status. 0d = No IN3P over voltage fault detected 1d = IN3P over voltage fault has detected
4	INT_LIVE1[4]	R	0h	Channel 4 IN4P over voltage fault status. 0d = No IN4P over voltage fault detected 1d = IN4P over voltage fault has detected
3	INT_LIVE1[3]	R	0h	Channel 5 IN5P over voltage fault status. Applicable only for PCM6x60-Q1. 0d = No IN5P over voltage fault detected 1d = IN5P over voltage fault has detected
2	INT_LIVE1[2]	R	0h	Channel 6 IN6P over voltage fault status. Applicable only for PCM6x60-Q1. 0d = No IN6P over voltage fault detected 1d = IN6P over voltage fault has detected
1-0	Reserved	R	0h	Reserved

8.6.1.4.12 INT_LIVE3 Register (page = 0x01, address = 0x37) [reset = 0h]

This register is the live Interrupt readback register 3.

Figure 195. INT_LIVE3 Register

7	6	5	4	3	2	1	0
INT_LIVE3[7]	INT_LIVE3[6]	INT_LIVE3[5]	Reserved				
R-0h	R-0h	R-0h	R-0h				

Table 151. INT_LIVE3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LIVE3[7]	R	0h	Fault status for MICBIAS high current. 0d = No fault detected 1d = Fault detected
6	INT_LIVE3[6]	R	0h	Fault status for MICBIAS low current 0d = No fault detected 1d = Fault detected
5	INT_LIVE3[5]	R	0h	Fault status for MICBIAS over voltage. 0d = No fault detected 1d = Fault detected
4-0	Reserved	R	0h	Reserved

8.6.1.4.13 MBIAS_OV_CFG Register (page = 0x01, address = 0x55) [reset = 40h]

This register is the MICBIAS overvoltage configuration register.

Figure 196. MBIAS_OV_CFG Register

7	6	5	4	3	2	1	0
MBIAS_OV_THRES[2:0]			Reserved				
RW-2h			R-0h				

Table 152. MBIAS_OV_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	MBIAS_OV_THRES[2:0]	RW	2h	MICBIAS overvoltage fault detection threshold above MICBIAS programmed voltage. 0d = No threshold over programmed voltage 1d = 10 mV (typ) threshold over programmed voltage 2d = 40 mV (typ) threshold over programmed voltage (default) 3d to 6d = Threshold value is set as per configuration with step size of 30mV (typ) 7d = 190 mV (typ) threshold over programmed voltage (default)
4-0	Reserved	R	0h	Reserved

8.6.1.4.14 DIAGDATA_CFG Register (page = 0x01, address = 0x59) [reset = 0h]

This register is the diagnostic data configuration register.

Figure 197. DIAGDATA_CFG Register

7	6	5	4	3	2	1	0
Reserved				Reserved			HOLD_SAR_DATA
RW-0h				R-0h			RW-0h

Table 153. DIAGDATA_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	RW	0h	Reserved
3-1	Reserved	R	0h	Reserved
0	HOLD_SAR_DATA	RW	0h	Hold SAR data update during register readback. 0b= Data update is not held, data register is continuously updated; this setting must be used when moving average is enabled for fault detection 1b= Data update is held, data register readback can be done

8.6.1.4.15 DIAG_MON_MSB_VBAT Register (page = 0x01, address = 0x5A) [reset = 0h]

This register is the MSB data byte of VBAT_IN monitoring.

Figure 198. DIAG_MON_MSB_VBAT Register

7	6	5	4	3	2	1	0
DIAG_MON_MSB_VBAT[7:0]							
R-0h							

Table 154. DIAG_MON_MSB_VBAT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIAG_MON_MSB_VBAT[7:0]	R	0h	Diagnostic SAR monitor data MSB byte

8.6.1.4.16 DIAG_MON_LSB_VBAT Register (page = 0x01, address = 0x5B) [reset = 0h]

This register is the LSB data nibble of VBAT_IN monitoring.

Figure 199. DIAG_MON_LSB_VBAT Register

7	6	5	4	3	2	1	0
DIAG_MON_LSB_VBAT[3:0]				CHANNEL_ID[3:0]			
R-0h				R-0h			

Table 155. DIAG_MON_LSB_VBAT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_MON_LSB_VBAT[3:0]	R	0h	Diagnostic SAR monitor data LSB nibble
3-0	CHANNEL_ID[3:0]	R	0h	Channel ID value

8.6.1.4.17 DIAG_MON_MSB_MBIAS Register (page = 0x01, address = 0x5C) [reset = 0h]

This register is the MSB data byte of MICBIAS monitoring.

Figure 200. DIAG_MON_MSB_MBIAS Register

7	6	5	4	3	2	1	0
DIAG_MON_MSB_MBIAS[7:0]							
R-0h							

Table 156. DIAG_MON_MSB_MBIAS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIAG_MON_MSB_MBIAS[7:0]	R	0h	Diagnostic SAR monitor data MSB byte

8.6.1.4.18 DIAG_MON_LSB_MBIAS Register (page = 0x01, address = 0x5D) [reset = 1h]

This register is the LSB data nibble of MICBIAS monitoring.

Figure 201. DIAG_MON_LSB_MBIAS Register

7	6	5	4	3	2	1	0
DIAG_MON_LSB_MBIAS[3:0]				CHANNEL_ID[3:0]			
R-0h				R-1h			

Table 157. DIAG_MON_LSB_MBIAS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_MON_LSB_MBIAS[3:0]	R	0h	Diagnostic SAR monitor data LSB nibble

Table 157. DIAG_MON_LSB_MBIAS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CHANNEL_ID[3:0]	R	1h	Channel ID value

8.6.1.4.19 DIAG_MON_MSB_IN1P Register (page = 0x01, address = 0x5E) [reset = 0h]

This register is the MSB data byte of IN1P monitoring.

Figure 202. DIAG_MON_MSB_IN1P Register

7	6	5	4	3	2	1	0
DIAG_MON_MSB_CH1P[7:0]							
R-0h							

Table 158. DIAG_MON_MSB_IN1P Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIAG_MON_MSB_CH1P[7:0]	R	0h	Diagnostic SAR monitor data MSB byte

8.6.1.4.20 DIAG_MON_LSB_IN1P Register (page = 0x01, address = 0x5F) [reset = 2h]

This register is the LSB data nibble of IN1P monitoring.

Figure 203. DIAG_MON_LSB_IN1P Register

7	6	5	4	3	2	1	0
DIAG_MON_LSB_CH1P[3:0]				CHANNEL_ID[3:0]			
R-0h				R-2h			

Table 159. DIAG_MON_LSB_IN1P Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_MON_LSB_CH1P[3:0]	R	0h	Diagnostic SAR monitor data LSB nibble
3-0	CHANNEL_ID[3:0]	R	2h	Channel ID value

8.6.1.4.21 DIAG_MON_MSB_IN1M Register (page = 0x01, address = 0x60) [reset = 0h]

This register is the MSB data byte of IN1M monitoring.

Figure 204. DIAG_MON_MSB_IN1M Register

7	6	5	4	3	2	1	0
DIAG_MON_MSB_CH1N[7:0]							
R-0h							

Table 160. DIAG_MON_MSB_IN1M Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIAG_MON_MSB_CH1N[7:0]	R	0h	Diagnostic SAR monitor data MSB byte

8.6.1.4.22 DIAG_MON_LSB_IN1M Register (page = 0x01, address = 0x61) [reset = 3h]

This register is the LSB data nibble of IN1M monitoring.

Figure 205. DIAG_MON_LSB_IN1M Register

7	6	5	4	3	2	1	0
DIAG_MON_LSB_CH1N[3:0]				CHANNEL_ID[3:0]			
R-0h				R-3h			

Table 161. DIAG_MON_LSB_IN1M Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_MON_LSB_CH1N[3:0]	R	0h	Diagnostic SAR monitor data LSB nibble
3-0	CHANNEL_ID[3:0]	R	3h	Channel ID value

8.6.1.4.23 DIAG_MON_MSB_IN2P Register (page = 0x01, address = 0x62) [reset = 0h]

This register is the MSB data byte of IN2P monitoring.

Figure 206. DIAG_MON_MSB_IN2P Register

7	6	5	4	3	2	1	0
DIAG_MON_MSB_CH2P[7:0]							
R-0h							

Table 162. DIAG_MON_MSB_IN2P Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIAG_MON_MSB_CH2P[7:0]	R	0h	Diagnostic SAR monitor data MSB byte

8.6.1.4.24 DIAG_MON_LSB_IN2P Register (page = 0x01, address = 0x63) [reset = 4h]

This register is the LSB data nibble of IN2P monitoring.

Figure 207. DIAG_MON_LSB_IN2P Register

7	6	5	4	3	2	1	0
DIAG_MON_LSB_CH2P[3:0]				CHANNEL_ID[3:0]			
R-0h				R-4h			

Table 163. DIAG_MON_LSB_IN2P Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_MON_LSB_CH2P[3:0]	R	0h	Diagnostic SAR monitor data LSB nibble
3-0	CHANNEL_ID[3:0]	R	4h	Channel ID value

8.6.1.4.25 DIAG_MON_MSB_IN2M Register (page = 0x01, address = 0x64) [reset = 0h]

This register is the MSB data byte of IN2M monitoring.

Figure 208. DIAG_MON_MSB_IN2M Register

7	6	5	4	3	2	1	0
DIAG_MON_MSB_CH2N[7:0]							
R-0h							

Table 164. DIAG_MON_MSB_IN2M Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIAG_MON_MSB_CH2N[7:0]	R	0h	Diagnostic SAR monitor data MSB byte

8.6.1.4.26 DIAG_MON_LSB_IN2M Register (page = 0x01, address = 0x65) [reset = 5h]

This register is the LSB data nibble of IN2M monitoring.

Figure 209. DIAG_MON_LSB_IN2M Register

7	6	5	4	3	2	1	0
DIAG_MON_LSB_CH2N[3:0]				CHANNEL_ID[3:0]			
R-0h				R-5h			

Table 165. DIAG_MON_LSB_IN2M Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_MON_LSB_CH2N[3:0]	R	0h	Diagnostic SAR monitor data LSB nibble
3-0	CHANNEL_ID[3:0]	R	5h	Channel ID value

8.6.1.4.27 DIAG_MON_MSB_IN3P Register (page = 0x01, address = 0x66) [reset = 0h]

This register is the MSB data byte of IN3P monitoring.

Figure 210. DIAG_MON_MSB_IN3P Register

7	6	5	4	3	2	1	0
DIAG_MON_MSB_CH3P[7:0]							
R-0h							

Table 166. DIAG_MON_MSB_IN3P Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIAG_MON_MSB_CH3P[7:0]	R	0h	Diagnostic SAR monitor data MSB byte

8.6.1.4.28 DIAG_MON_LSB_IN3P Register (page = 0x01, address = 0x67) [reset = 6h]

This register is the LSB data nibble of IN3P monitoring.

Figure 211. DIAG_MON_LSB_IN3P Register

7	6	5	4	3	2	1	0
DIAG_MON_LSB_CH3P[3:0]				CHANNEL_ID[3:0]			
R-0h				R-6h			

Table 167. DIAG_MON_LSB_IN3P Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_MON_LSB_CH3P[3:0]	R	0h	Diagnostic SAR monitor data LSB nibble
3-0	CHANNEL_ID[3:0]	R	6h	Channel ID value

8.6.1.4.29 DIAG_MON_MSB_IN3M Register (page = 0x01, address = 0x68) [reset = 0h]

This register is the MSB data byte of IN3M monitoring.

Figure 212. DIAG_MON_MSB_IN3M Register

7	6	5	4	3	2	1	0
DIAG_MON_MSB_CH3N[7:0]							
R-0h							

Table 168. DIAG_MON_MSB_IN3M Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIAG_MON_MSB_CH3N[7:0]	R	0h	Diagnostic SAR monitor data MSB byte

8.6.1.4.30 DIAG_MON_LSB_IN3M Register (page = 0x01, address = 0x69) [reset = 7h]

This register is the LSB data nibble of IN3M monitoring.

Figure 213. DIAG_MON_LSB_IN3M Register

7	6	5	4	3	2	1	0
DIAG_MON_LSB_CH3N[3:0]				CHANNEL_ID[3:0]			
R-0h				R-7h			

Table 169. DIAG_MON_LSB_IN3M Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_MON_LSB_CH3N[3:0]	R	0h	Diagnostic SAR monitor data LSB nibble
3-0	CHANNEL_ID[3:0]	R	7h	Channel ID value

8.6.1.4.31 DIAG_MON_MSB_IN4P Register (page = 0x01, address = 0x6A) [reset = 0h]

This register is the MSB data byte of IN4P monitoring.

Figure 214. DIAG_MON_MSB_IN4P Register

7	6	5	4	3	2	1	0
DIAG_MON_MSB_CH4P[7:0]							
R-0h							

Table 170. DIAG_MON_MSB_IN4P Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIAG_MON_MSB_CH4P[7:0]	R	0h	Diagnostic SAR monitor data MSB byte

8.6.1.4.32 DIAG_MON_LSB_IN4P Register (page = 0x01, address = 0x6B) [reset = 8h]

This register is the LSB data nibble of IN4P monitoring.

Figure 215. DIAG_MON_LSB_IN4P Register

7	6	5	4	3	2	1	0
DIAG_MON_LSB_CH4P[3:0]				CHANNEL_ID[3:0]			
R-0h				R-8h			

Table 171. DIAG_MON_LSB_IN4P Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_MON_LSB_CH4P[3:0]	R	0h	Diagnostic SAR monitor data LSB nibble
3-0	CHANNEL_ID[3:0]	R	8h	Channel ID value

8.6.1.4.33 DIAG_MON_MSB_IN4M Register (page = 0x01, address = 0x6C) [reset = 0h]

This register is the MSB data byte of IN4M monitoring.

Figure 216. DIAG_MON_MSB_IN4M Register

7	6	5	4	3	2	1	0
DIAG_MON_MSB_CH4N[7:0]							
R-0h							

Table 172. DIAG_MON_MSB_IN4M Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIAG_MON_MSB_CH4N[7:0]	R	0h	Diagnostic SAR monitor data MSB byte

8.6.1.4.34 DIAG_MON_LSB_IN4M Register (page = 0x01, address = 0x6D) [reset = 9h]

This register is the LSB data nibble of IN4M monitoring.

Figure 217. DIAG_MON_LSB_IN4M Register

7	6	5	4	3	2	1	0
DIAG_MON_LSB_CH4N[3:0]				CHANNEL_ID[3:0]			
R-0h				R-9h			

Table 173. DIAG_MON_LSB_IN4M Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_MON_LSB_CH4N[3:0]	R	0h	Diagnostic SAR monitor data LSB nibble
3-0	CHANNEL_ID[3:0]	R	9h	Channel ID value

8.6.1.4.35 DIAG_MON_MSB_IN5P Register (page = 0x01, address = 0x6E) [reset = 0h]

This register is the MSB data byte of IN5P monitoring. Applicable only for PCM6x60-Q1.

Figure 218. DIAG_MON_MSB_IN5P Register

7	6	5	4	3	2	1	0
DIAG_MON_MSB_CH5P[7:0]							
R-0h							

Table 174. DIAG_MON_MSB_IN5P Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIAG_MON_MSB_CH5P[7:0]	R	0h	Diagnostic SAR monitor data MSB byte

8.6.1.4.36 DIAG_MON_LSB_IN5P Register (page = 0x01, address = 0x6F) [reset = Ah]

This register is the LSB data nibble of IN5P monitoring. Applicable only for PCM6x60-Q1.

Figure 219. DIAG_MON_LSB_IN5P Register

7	6	5	4	3	2	1	0
DIAG_MON_LSB_CH5P[3:0]				CHANNEL_ID[3:0]			
R-0h				R-Ah			

Table 175. DIAG_MON_LSB_IN5P Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_MON_LSB_CH5P[3:0]	R	0h	Diagnostic SAR monitor data LSB nibble
3-0	CHANNEL_ID[3:0]	R	Ah	Channel ID value

8.6.1.4.37 DIAG_MON_MSB_IN5M Register (page = 0x01, address = 0x70) [reset = 0h]

This register is the MSB data byte of IN5M monitoring. Applicable only for PCM6x60-Q1.

Figure 220. DIAG_MON_MSB_IN5M Register

7	6	5	4	3	2	1	0
DIAG_MON_MSB_CH5N[7:0]							
R-0h							

Table 176. DIAG_MON_MSB_IN5M Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIAG_MON_MSB_CH5N[7:0]	R	0h	Diagnostic SAR monitor data MSB byte

8.6.1.4.38 DIAG_MON_LSB_IN5M Register (page = 0x01, address = 0x71) [reset = Bh]

This register is the LSB data nibble of IN5M monitoring. Applicable only for PCM6x60-Q1.

Figure 221. DIAG_MON_LSB_IN5M Register

7	6	5	4	3	2	1	0
DIAG_MON_LSB_CH5N[3:0]				CHANNEL_ID[3:0]			
R-0h				R-Bh			

Table 177. DIAG_MON_LSB_IN5M Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_MON_LSB_CH5N[3:0]	R	0h	Diagnostic SAR monitor data LSB nibble
3-0	CHANNEL_ID[3:0]	R	Bh	Channel ID value

8.6.1.4.39 DIAG_MON_MSB_IN6P Register (page = 0x01, address = 0x72) [reset = 0h]

This register is the MSB data byte of IN6P monitoring. Applicable only for PCM6x60-Q1.

Figure 222. DIAG_MON_MSB_IN6P Register

7	6	5	4	3	2	1	0
DIAG_MON_MSB_CH6P[7:0]							
R-0h							

Table 178. DIAG_MON_MSB_IN6P Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIAG_MON_MSB_CH6P[7:0]	R	0h	Diagnostic SAR monitor data MSB byte

8.6.1.4.40 DIAG_MON_LSB_IN6P Register (page = 0x01, address = 0x73) [reset = Ch]

This register is the LSB data nibble of IN6P monitoring. Applicable only for PCM6x60-Q1.

Figure 223. DIAG_MON_LSB_IN6P Register

7	6	5	4	3	2	1	0
DIAG_MON_LSB_CH6P[3:0]				CHANNEL_ID[3:0]			
R-0h				R-Ch			

Table 179. DIAG_MON_LSB_IN6P Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_MON_LSB_CH6P[3:0]	R	0h	Diagnostic SAR monitor data LSB nibble
3-0	CHANNEL_ID[3:0]	R	Ch	Channel ID value

8.6.1.4.41 DIAG_MON_MSB_IN6M Register (page = 0x01, address = 0x74) [reset = 0h]

This register is the MSB data byte of IN6M monitoring. Applicable only for PCM6x60-Q1.

Figure 224. DIAG_MON_MSB_IN6M Register

7	6	5	4	3	2	1	0
DIAG_MON_MSB_CH6N[7:0]							
R-0h							

Table 180. DIAG_MON_MSB_IN6M Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIAG_MON_MSB_CH6N[7:0]	R	0h	Diagnostic SAR monitor data MSB byte

8.6.1.4.42 DIAG_MON_LSB_IN6M Register (page = 0x01, address = 0x75) [reset = Dh]

This register is the LSB data nibble of IN6M monitoring. Applicable only for PCM6x60-Q1.

Figure 225. DIAG_MON_LSB_IN6M Register

7	6	5	4	3	2	1	0
DIAG_MON_LSB_CH6N[3:0]				CHANNEL_ID[3:0]			
R-0h				R-Dh			

Table 181. DIAG_MON_LSB_IN6M Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_MON_LSB_CH6N[3:0]	R	0h	Diagnostic SAR monitor data LSB nibble
3-0	CHANNEL_ID[3:0]	R	Dh	Channel ID value

8.6.1.4.43 DIAG_MON_MSB_TEMP Register (page = 0x01, address = 0x76) [reset = 0h]

This register is the MSB data byte of temperature monitoring.

Figure 226. DIAG_MON_MSB_TEMP Register

7	6	5	4	3	2	1	0
DIAG_MON_MSB_TEMP[7:0]							
R-0h							

Table 182. DIAG_MON_MSB_TEMP Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIAG_MON_MSB_TEMP[7:0]	R	0h	Diagnostic SAR monitor data MSB byte

8.6.1.4.44 DIAG_MON_LSB_TEMP Register (page = 0x01, address = 0x77) [reset = Eh]

This register is the LSB data nibble of temperature monitoring.

Figure 227. DIAG_MON_LSB_TEMP Register

7	6	5	4	3	2	1	0
DIAG_MON_LSB_TEMP[3:0]				CHANNEL_ID[3:0]			
R-0h				R-Eh			

Table 183. DIAG_MON_LSB_TEMP Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_MON_LSB_TEMP[3:0]	R	0h	Diagnostic SAR monitor data LSB nibble

Table 183. DIAG_MON_LSB_TEMP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CHANNEL_ID[3:0]	R	Eh	Channel ID value

8.6.1.4.45 DIAG_MON_MSB_LOAD Register (page = 0x01, address = 0x78) [reset = 0h]

This register is the MSB data byte of MICBIAS load current monitoring.

Figure 228. DIAG_MON_MSB_LOAD Register

7	6	5	4	3	2	1	0
DIAG_MON_MSB_LOAD[7:0]							
R-0h							

Table 184. DIAG_MON_MSB_LOAD Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIAG_MON_MSB_LOAD[7:0]	R	0h	Diagnostic SAR monitor data MSB byte

8.6.1.4.46 DIAG_MON_LSB_LOAD Register (page = 0x01, address = 0x79) [reset = Fh]

This register is the LSB data nibble of MICBIAS load current monitoring.

Figure 229. DIAG_MON_LSB_LOAD Register

7	6	5	4	3	2	1	0
DIAG_MON_LSB_LOAD[3:0]				CHANNEL_ID[3:0]			
R-0h				R-Fh			

Table 185. DIAG_MON_LSB_LOAD Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_MON_LSB_LOAD[3:0]	R	0h	Diagnostic SAR monitor data LSB nibble
3-0	CHANNEL_ID[3:0]	R	Fh	Channel ID value

8.6.2 Programmable Coefficient Registers

8.6.2.1 Programmable Coefficient Registers: Page = 0x02

This register page (shown in Register Description: Page = 0x00) consists of the programmable coefficients for the biquad 1 to biquad 6 filters. To optimize the coefficients register transaction time for page 2, page 3, and page 4, the device also supports (by default) auto-incremented pages for the I^2C and SPI burst writes and reads. After a transaction of register address 0x7F, the device auto increments to the next page at register 0x08 to transact the next coefficient value. These programmable coefficients are 32-bit, two's complement numbers. For a successful coefficient register transaction, the host device must write and read all four bytes starting with the most significant byte (BYT1) for a target coefficient register transaction. When using SPI for a coefficient register read transaction, the device transmits the first byte as a dummy read byte; therefore, the host must read five bytes, including the first dummy read byte and the last four bytes corresponding to the coefficient register value starting with the most significant byte (BYT1).

Table 186. Page 0x02 Programmable Coefficient Registers

ADDRESS	REGISTER	RESET	DESCRIPTION
0x00	PAGE[7:0]	0x00	Device page register
0x08	BQ1_N0_BYT1[7:0]	0x7F	Programmable biquad 1, N0 coefficient byte[31:24]
0x09	BQ1_N0_BYT2[7:0]	0xFF	Programmable biquad 1, N0 coefficient byte[23:16]
0x0A	BQ1_N0_BYT3[7:0]	0xFF	Programmable biquad 1, N0 coefficient byte[15:8]
0x0B	BQ1_N0_BYT4[7:0]	0xFF	Programmable biquad 1, N0 coefficient byte[7:0]
0x0C	BQ1_N1_BYT1[7:0]	0x00	Programmable biquad 1, N1 coefficient byte[31:24]
0x0D	BQ1_N1_BYT2[7:0]	0x00	Programmable biquad 1, N1 coefficient byte[23:16]
0x0E	BQ1_N1_BYT3[7:0]	0x00	Programmable biquad 1, N1 coefficient byte[15:8]
0x0F	BQ1_N1_BYT4[7:0]	0x00	Programmable biquad 1, N1 coefficient byte[7:0]
0x10	BQ1_N2_BYT1[7:0]	0x00	Programmable biquad 1, N2 coefficient byte[31:24]
0x11	BQ1_N2_BYT2[7:0]	0x00	Programmable biquad 1, N2 coefficient byte[23:16]
0x12	BQ1_N2_BYT3[7:0]	0x00	Programmable biquad 1, N2 coefficient byte[15:8]
0x13	BQ1_N2_BYT4[7:0]	0x00	Programmable biquad 1, N2 coefficient byte[7:0]
0x14	BQ1_D1_BYT1[7:0]	0x00	Programmable biquad 1, D1 coefficient byte[31:24]
0x15	BQ1_D1_BYT2[7:0]	0x00	Programmable biquad 1, D1 coefficient byte[23:16]
0x16	BQ1_D1_BYT3[7:0]	0x00	Programmable biquad 1, D1 coefficient byte[15:8]
0x17	BQ1_D1_BYT4[7:0]	0x00	Programmable biquad 1, D1 coefficient byte[7:0]
0x18	BQ1_D2_BYT1[7:0]	0x00	Programmable biquad 1, D2 coefficient byte[31:24]
0x19	BQ1_D2_BYT2[7:0]	0x00	Programmable biquad 1, D2 coefficient byte[23:16]
0x1A	BQ1_D2_BYT3[7:0]	0x00	Programmable biquad 1, D2 coefficient byte[15:8]
0x1B	BQ1_D2_BYT4[7:0]	0x00	Programmable biquad 1, D2 coefficient byte[7:0]
0x1C	BQ2_N0_BYT1[7:0]	0x7F	Programmable biquad 2, N0 coefficient byte[31:24]
0x1D	BQ2_N0_BYT2[7:0]	0xFF	Programmable biquad 2, N0 coefficient byte[23:16]
0x1E	BQ2_N0_BYT3[7:0]	0xFF	Programmable biquad 2, N0 coefficient byte[15:8]
0x1F	BQ2_N0_BYT4[7:0]	0xFF	Programmable biquad 2, N0 coefficient byte[7:0]
0x20	BQ2_N1_BYT1[7:0]	0x00	Programmable biquad 2, N1 coefficient byte[31:24]
0x21	BQ2_N1_BYT2[7:0]	0x00	Programmable biquad 2, N1 coefficient byte[23:16]
0x22	BQ2_N1_BYT3[7:0]	0x00	Programmable biquad 2, N1 coefficient byte[15:8]
0x23	BQ2_N1_BYT4[7:0]	0x00	Programmable biquad 2, N1 coefficient byte[7:0]
0x24	BQ2_N2_BYT1[7:0]	0x00	Programmable biquad 2, N2 coefficient byte[31:24]
0x25	BQ2_N2_BYT2[7:0]	0x00	Programmable biquad 2, N2 coefficient byte[23:16]
0x26	BQ2_N2_BYT3[7:0]	0x00	Programmable biquad 2, N2 coefficient byte[15:8]
0x27	BQ2_N2_BYT4[7:0]	0x00	Programmable biquad 2, N2 coefficient byte[7:0]
0x28	BQ2_D1_BYT1[7:0]	0x00	Programmable biquad 2, D1 coefficient byte[31:24]
0x29	BQ2_D1_BYT2[7:0]	0x00	Programmable biquad 2, D1 coefficient byte[23:16]
0x2A	BQ2_D1_BYT3[7:0]	0x00	Programmable biquad 2, D1 coefficient byte[15:8]
0x2B	BQ2_D1_BYT4[7:0]	0x00	Programmable biquad 2, D1 coefficient byte[7:0]
0x2C	BQ2_D2_BYT1[7:0]	0x00	Programmable biquad 2, D2 coefficient byte[31:24]

Table 186. Page 0x02 Programmable Coefficient Registers (continued)

0x2D	BQ2_D2_BYT2[7:0]	0x00	Programmable biquad 2, D2 coefficient byte[23:16]
0x2E	BQ2_D2_BYT3[7:0]	0x00	Programmable biquad 2, D2 coefficient byte[15:8]
0x2F	BQ2_D2_BYT4[7:0]	0x00	Programmable biquad 2, D2 coefficient byte[7:0]
0x30	BQ3_N0_BYT1[7:0]	0x7F	Programmable biquad 3, N0 coefficient byte[31:24]
0x31	BQ3_N0_BYT2[7:0]	0xFF	Programmable biquad 3, N0 coefficient byte[23:16]
0x32	BQ3_N0_BYT3[7:0]	0xFF	Programmable biquad 3, N0 coefficient byte[15:8]
0x33	BQ3_N0_BYT4[7:0]	0xFF	Programmable biquad 3, N0 coefficient byte[7:0]
0x34	BQ3_N1_BYT1[7:0]	0x00	Programmable biquad 3, N1 coefficient byte[31:24]
0x35	BQ3_N1_BYT2[7:0]	0x00	Programmable biquad 3, N1 coefficient byte[23:16]
0x36	BQ3_N1_BYT3[7:0]	0x00	Programmable biquad 3, N1 coefficient byte[15:8]
0x37	BQ3_N1_BYT4[7:0]	0x00	Programmable biquad 3, N1 coefficient byte[7:0]
0x38	BQ3_N2_BYT1[7:0]	0x00	Programmable biquad 3, N2 coefficient byte[31:24]
0x39	BQ3_N2_BYT2[7:0]	0x00	Programmable biquad 3, N2 coefficient byte[23:16]
0x3A	BQ3_N2_BYT3[7:0]	0x00	Programmable biquad 3, N2 coefficient byte[15:8]
0x3B	BQ3_N2_BYT4[7:0]	0x00	Programmable biquad 3, N2 coefficient byte[7:0]
0x3C	BQ3_D1_BYT1[7:0]	0x00	Programmable biquad 3, D1 coefficient byte[31:24]
0x3D	BQ3_D1_BYT2[7:0]	0x00	Programmable biquad 3, D1 coefficient byte[23:16]
0x3E	BQ3_D1_BYT3[7:0]	0x00	Programmable biquad 3, D1 coefficient byte[15:8]
0x3F	BQ3_D1_BYT4[7:0]	0x00	Programmable biquad 3, D1 coefficient byte[7:0]
0x40	BQ3_D2_BYT1[7:0]	0x00	Programmable biquad 3, D2 coefficient byte[31:24]
0x41	BQ3_D2_BYT2[7:0]	0x00	Programmable biquad 3, D2 coefficient byte[23:16]
0x42	BQ3_D2_BYT3[7:0]	0x00	Programmable biquad 3, D2 coefficient byte[15:8]
0x43	BQ3_D2_BYT4[7:0]	0x00	Programmable biquad 3, D2 coefficient byte[7:0]
0x44	BQ4_N0_BYT1[7:0]	0x7F	Programmable biquad 4, N0 coefficient byte[31:24]
0x45	BQ4_N0_BYT2[7:0]	0xFF	Programmable biquad 4, N0 coefficient byte[23:16]
0x46	BQ4_N0_BYT3[7:0]	0xFF	Programmable biquad 4, N0 coefficient byte[15:8]
0x47	BQ4_N0_BYT4[7:0]	0xFF	Programmable biquad 4, N0 coefficient byte[7:0]
0x48	BQ4_N1_BYT1[7:0]	0x00	Programmable biquad 4, N1 coefficient byte[31:24]
0x49	BQ4_N1_BYT2[7:0]	0x00	Programmable biquad 4, N1 coefficient byte[23:16]
0x4A	BQ4_N1_BYT3[7:0]	0x00	Programmable biquad 4, N1 coefficient byte[15:8]
0x4B	BQ4_N1_BYT4[7:0]	0x00	Programmable biquad 4, N1 coefficient byte[7:0]
0x4C	BQ4_N2_BYT1[7:0]	0x00	Programmable biquad 4, N2 coefficient byte[31:24]
0x4D	BQ4_N2_BYT2[7:0]	0x00	Programmable biquad 4, N2 coefficient byte[23:16]
0x4E	BQ4_N2_BYT3[7:0]	0x00	Programmable biquad 4, N2 coefficient byte[15:8]
0x4F	BQ4_N2_BYT4[7:0]	0x00	Programmable biquad 4, N2 coefficient byte[7:0]
0x50	BQ4_D1_BYT1[7:0]	0x00	Programmable biquad 4, D1 coefficient byte[31:24]
0x51	BQ4_D1_BYT2[7:0]	0x00	Programmable biquad 4, D1 coefficient byte[23:16]
0x52	BQ4_D1_BYT3[7:0]	0x00	Programmable biquad 4, D1 coefficient byte[15:8]
0x53	BQ4_D1_BYT4[7:0]	0x00	Programmable biquad 4, D1 coefficient byte[7:0]
0x54	BQ4_D2_BYT1[7:0]	0x00	Programmable biquad 4, D2 coefficient byte[31:24]
0x55	BQ4_D2_BYT2[7:0]	0x00	Programmable biquad 4, D2 coefficient byte[23:16]
0x56	BQ4_D2_BYT3[7:0]	0x00	Programmable biquad 4, D2 coefficient byte[15:8]
0x57	BQ4_D2_BYT4[7:0]	0x00	Programmable biquad 4, D2 coefficient byte[7:0]
0x58	BQ5_N0_BYT1[7:0]	0x7F	Programmable biquad 5, N0 coefficient byte[31:24]
0x59	BQ5_N0_BYT2[7:0]	0xFF	Programmable biquad 5, N0 coefficient byte[23:16]
0x5A	BQ5_N0_BYT3[7:0]	0xFF	Programmable biquad 5, N0 coefficient byte[15:8]
0x5B	BQ5_N0_BYT4[7:0]	0xFF	Programmable biquad 5, N0 coefficient byte[7:0]
0x5C	BQ5_N1_BYT1[7:0]	0x00	Programmable biquad 5, N1 coefficient byte[31:24]
0x5D	BQ5_N1_BYT2[7:0]	0x00	Programmable biquad 5, N1 coefficient byte[23:16]
0x5E	BQ5_N1_BYT3[7:0]	0x00	Programmable biquad 5, N1 coefficient byte[15:8]
0x5F	BQ5_N1_BYT4[7:0]	0x00	Programmable biquad 5, N1 coefficient byte[7:0]
0x60	BQ5_N2_BYT1[7:0]	0x00	Programmable biquad 5, N2 coefficient byte[31:24]

Table 186. Page 0x02 Programmable Coefficient Registers (continued)

0x61	BQ5_N2_BYT2[7:0]	0x00	Programmable biquad 5, N2 coefficient byte[23:16]
0x62	BQ5_N2_BYT3[7:0]	0x00	Programmable biquad 5, N2 coefficient byte[15:8]
0x63	BQ5_N2_BYT4[7:0]	0x00	Programmable biquad 5, N2 coefficient byte[7:0]
0x64	BQ5_D1_BYT1[7:0]	0x00	Programmable biquad 5, D1 coefficient byte[31:24]
0x65	BQ5_D1_BYT2[7:0]	0x00	Programmable biquad 5, D1 coefficient byte[23:16]
0x66	BQ5_D1_BYT3[7:0]	0x00	Programmable biquad 5, D1 coefficient byte[15:8]
0x67	BQ5_D1_BYT4[7:0]	0x00	Programmable biquad 5, D1 coefficient byte[7:0]
0x68	BQ5_D2_BYT1[7:0]	0x00	Programmable biquad 5, D2 coefficient byte[31:24]
0x69	BQ5_D2_BYT2[7:0]	0x00	Programmable biquad 5, D2 coefficient byte[23:16]
0x6A	BQ5_D2_BYT3[7:0]	0x00	Programmable biquad 5, D2 coefficient byte[15:8]
0x6B	BQ5_D2_BYT4[7:0]	0x00	Programmable biquad 5, D2 coefficient byte[7:0]
0x6C	BQ6_N0_BYT1[7:0]	0x7F	Programmable biquad 6, N0 coefficient byte[31:24]
0x6D	BQ6_N0_BYT2[7:0]	0xFF	Programmable biquad 6, N0 coefficient byte[23:16]
0x6E	BQ6_N0_BYT3[7:0]	0xFF	Programmable biquad 6, N0 coefficient byte[15:8]
0x6F	BQ6_N0_BYT4[7:0]	0xFF	Programmable biquad 6, N0 coefficient byte[7:0]
0x70	BQ6_N1_BYT1[7:0]	0x00	Programmable biquad 6, N1 coefficient byte[31:24]
0x71	BQ6_N1_BYT2[7:0]	0x00	Programmable biquad 6, N1 coefficient byte[23:16]
0x72	BQ6_N1_BYT3[7:0]	0x00	Programmable biquad 6, N1 coefficient byte[15:8]
0x73	BQ6_N1_BYT4[7:0]	0x00	Programmable biquad 6, N1 coefficient byte[7:0]
0x74	BQ6_N2_BYT1[7:0]	0x00	Programmable biquad 6, N2 coefficient byte[31:24]
0x75	BQ6_N2_BYT2[7:0]	0x00	Programmable biquad 6, N2 coefficient byte[23:16]
0x76	BQ6_N2_BYT3[7:0]	0x00	Programmable biquad 6, N2 coefficient byte[15:8]
0x77	BQ6_N2_BYT4[7:0]	0x00	Programmable biquad 6, N2 coefficient byte[7:0]
0x78	BQ6_D1_BYT1[7:0]	0x00	Programmable biquad 6, D1 coefficient byte[31:24]
0x79	BQ6_D1_BYT2[7:0]	0x00	Programmable biquad 6, D1 coefficient byte[23:16]
0x7A	BQ6_D1_BYT3[7:0]	0x00	Programmable biquad 6, D1 coefficient byte[15:8]
0x7B	BQ6_D1_BYT4[7:0]	0x00	Programmable biquad 6, D1 coefficient byte[7:0]
0x7C	BQ6_D2_BYT1[7:0]	0x00	Programmable biquad 6, D2 coefficient byte[31:24]
0x7D	BQ6_D2_BYT2[7:0]	0x00	Programmable biquad 6, D2 coefficient byte[23:16]
0x7E	BQ6_D2_BYT3[7:0]	0x00	Programmable biquad 6, D2 coefficient byte[15:8]
0x7F	BQ6_D2_BYT4[7:0]	0x00	Programmable biquad 6, D2 coefficient byte[7:0]

8.6.2.2 Programmable Coefficient Registers: Page = 0x03

This register page (shown in Table 187) consists of the programmable coefficients for the biquad 7 to biquad 12 filters. To optimize the coefficients register transaction time for page 2, page 3, and page 4, the device also supports (by default) auto-incremented pages for the I^2C and SPI burst writes and reads. After a transaction of register address 0x7F, the device auto increments to the next page at register 0x08 to transact the next coefficient value. These programmable coefficients are 32-bit, two's complement numbers. For a successful coefficient register transaction, the host device must write and read all four bytes starting with the most significant byte (BYT1) for a target coefficient register transaction. When using SPI for a coefficient register read transaction, the device transmits the first byte as a dummy read byte; therefore, the host must read five bytes, including the first dummy read byte and the last four bytes corresponding to the coefficient register value starting with the most significant byte (BYT1).

Table 187. Page 0x03 Programmable Coefficient Registers

ADDR	REGISTER	RESET	DESCRIPTION
0x00	PAGE[7:0]	0x00	Device page register
0x08	BQ7_N0_BYT1[7:0]	0x7F	Programmable biquad 7, N0 coefficient byte[31:24]
0x09	BQ7_N0_BYT2[7:0]	0xFF	Programmable biquad 7, N0 coefficient byte[23:16]
0x0A	BQ7_N0_BYT3[7:0]	0xFF	Programmable biquad 7, N0 coefficient byte[15:8]
0x0B	BQ7_N0_BYT4[7:0]	0xFF	Programmable biquad 7, N0 coefficient byte[7:0]
0x0C	BQ7_N1_BYT1[7:0]	0x00	Programmable biquad 7, N1 coefficient byte[31:24]
0x0D	BQ7_N1_BYT2[7:0]	0x00	Programmable biquad 7, N1 coefficient byte[23:16]
0x0E	BQ7_N1_BYT3[7:0]	0x00	Programmable biquad 7, N1 coefficient byte[15:8]
0x0F	BQ7_N1_BYT4[7:0]	0x00	Programmable biquad 7, N1 coefficient byte[7:0]
0x10	BQ7_N2_BYT1[7:0]	0x00	Programmable biquad 7, N2 coefficient byte[31:24]
0x11	BQ7_N2_BYT2[7:0]	0x00	Programmable biquad 7, N2 coefficient byte[23:16]
0x12	BQ7_N2_BYT3[7:0]	0x00	Programmable biquad 7, N2 coefficient byte[15:8]
0x13	BQ7_N2_BYT4[7:0]	0x00	Programmable biquad 7, N2 coefficient byte[7:0]
0x14	BQ7_D1_BYT1[7:0]	0x00	Programmable biquad 7, D1 coefficient byte[31:24]
0x15	BQ7_D1_BYT2[7:0]	0x00	Programmable biquad 7, D1 coefficient byte[23:16]
0x16	BQ7_D1_BYT3[7:0]	0x00	Programmable biquad 7, D1 coefficient byte[15:8]
0x17	BQ7_D1_BYT4[7:0]	0x00	Programmable biquad 7, D1 coefficient byte[7:0]
0x18	BQ7_D2_BYT1[7:0]	0x00	Programmable biquad 7, D2 coefficient byte[31:24]
0x19	BQ7_D2_BYT2[7:0]	0x00	Programmable biquad 7, D2 coefficient byte[23:16]
0x1A	BQ7_D2_BYT3[7:0]	0x00	Programmable biquad 7, D2 coefficient byte[15:8]
0x1B	BQ7_D2_BYT4[7:0]	0x00	Programmable biquad 7, D2 coefficient byte[7:0]
0x1C	BQ8_N0_BYT1[7:0]	0x7F	Programmable biquad 8, N0 coefficient byte[31:24]
0x1D	BQ8_N0_BYT2[7:0]	0xFF	Programmable biquad 8, N0 coefficient byte[23:16]
0x1E	BQ8_N0_BYT3[7:0]	0xFF	Programmable biquad 8, N0 coefficient byte[15:8]
0x1F	BQ8_N0_BYT4[7:0]	0xFF	Programmable biquad 8, N0 coefficient byte[7:0]
0x20	BQ8_N1_BYT1[7:0]	0x00	Programmable biquad 8, N1 coefficient byte[31:24]
0x21	BQ8_N1_BYT2[7:0]	0x00	Programmable biquad 8, N1 coefficient byte[23:16]
0x22	BQ8_N1_BYT3[7:0]	0x00	Programmable biquad 8, N1 coefficient byte[15:8]
0x23	BQ8_N1_BYT4[7:0]	0x00	Programmable biquad 8, N1 coefficient byte[7:0]
0x24	BQ8_N2_BYT1[7:0]	0x00	Programmable biquad 8, N2 coefficient byte[31:24]
0x25	BQ8_N2_BYT2[7:0]	0x00	Programmable biquad 8, N2 coefficient byte[23:16]
0x26	BQ8_N2_BYT3[7:0]	0x00	Programmable biquad 8, N2 coefficient byte[15:8]
0x27	BQ8_N2_BYT4[7:0]	0x00	Programmable biquad 8, N2 coefficient byte[7:0]
0x28	BQ8_D1_BYT1[7:0]	0x00	Programmable biquad 8, D1 coefficient byte[31:24]
0x29	BQ8_D1_BYT2[7:0]	0x00	Programmable biquad 8, D1 coefficient byte[23:16]
0x2A	BQ8_D1_BYT3[7:0]	0x00	Programmable biquad 8, D1 coefficient byte[15:8]
0x2B	BQ8_D1_BYT4[7:0]	0x00	Programmable biquad 8, D1 coefficient byte[7:0]
0x2C	BQ8_D2_BYT1[7:0]	0x00	Programmable biquad 8, D2 coefficient byte[31:24]
0x2D	BQ8_D2_BYT2[7:0]	0x00	Programmable biquad 8, D2 coefficient byte[23:16]
0x2E	BQ8_D2_BYT3[7:0]	0x00	Programmable biquad 8, D2 coefficient byte[15:8]

Table 187. Page 0x03 Programmable Coefficient Registers (continued)

0x2F	BQ8_D2_BYT4[7:0]	0x00	Programmable biquad 8, D2 coefficient byte[7:0]
0x30	BQ9_N0_BYT1[7:0]	0x7F	Programmable biquad 9, N0 coefficient byte[31:24]
0x31	BQ9_N0_BYT2[7:0]	0xFF	Programmable biquad 9, N0 coefficient byte[23:16]
0x32	BQ9_N0_BYT3[7:0]	0xFF	Programmable biquad 9, N0 coefficient byte[15:8]
0x33	BQ9_N0_BYT4[7:0]	0xFF	Programmable biquad 9, N0 coefficient byte[7:0]
0x34	BQ9_N1_BYT1[7:0]	0x00	Programmable biquad 9, N1 coefficient byte[31:24]
0x35	BQ9_N1_BYT2[7:0]	0x00	Programmable biquad 9, N1 coefficient byte[23:16]
0x36	BQ9_N1_BYT3[7:0]	0x00	Programmable biquad 9, N1 coefficient byte[15:8]
0x37	BQ9_N1_BYT4[7:0]	0x00	Programmable biquad 9, N1 coefficient byte[7:0]
0x38	BQ9_N2_BYT1[7:0]	0x00	Programmable biquad 9, N2 coefficient byte[31:24]
0x39	BQ9_N2_BYT2[7:0]	0x00	Programmable biquad 9, N2 coefficient byte[23:16]
0x3A	BQ9_N2_BYT3[7:0]	0x00	Programmable biquad 9, N2 coefficient byte[15:8]
0x3B	BQ9_N2_BYT4[7:0]	0x00	Programmable biquad 9, N2 coefficient byte[7:0]
0x3C	BQ9_D1_BYT1[7:0]	0x00	Programmable biquad 9, D1 coefficient byte[31:24]
0x3D	BQ9_D1_BYT2[7:0]	0x00	Programmable biquad 9, D1 coefficient byte[23:16]
0x3E	BQ9_D1_BYT3[7:0]	0x00	Programmable biquad 9, D1 coefficient byte[15:8]
0x3F	BQ9_D1_BYT4[7:0]	0x00	Programmable biquad 9, D1 coefficient byte[7:0]
0x40	BQ9_D2_BYT1[7:0]	0x00	Programmable biquad 9, D2 coefficient byte[31:24]
0x41	BQ9_D2_BYT2[7:0]	0x00	Programmable biquad 9, D2 coefficient byte[23:16]
0x42	BQ9_D2_BYT3[7:0]	0x00	Programmable biquad 9, D2 coefficient byte[15:8]
0x43	BQ9_D2_BYT4[7:0]	0x00	Programmable biquad 9, D2 coefficient byte[7:0]
0x44	BQ10_N0_BYT1[7:0]	0x7F	Programmable biquad 10, N0 coefficient byte[31:24]
0x45	BQ10_N0_BYT2[7:0]	0xFF	Programmable biquad 10, N0 coefficient byte[23:16]
0x46	BQ10_N0_BYT3[7:0]	0xFF	Programmable biquad 10, N0 coefficient byte[15:8]
0x47	BQ10_N0_BYT4[7:0]	0xFF	Programmable biquad 10, N0 coefficient byte[7:0]
0x48	BQ10_N1_BYT1[7:0]	0x00	Programmable biquad 10, N1 coefficient byte[31:24]
0x49	BQ10_N1_BYT2[7:0]	0x00	Programmable biquad 10, N1 coefficient byte[23:16]
0x4A	BQ10_N1_BYT3[7:0]	0x00	Programmable biquad 10, N1 coefficient byte[15:8]
0x4B	BQ10_N1_BYT4[7:0]	0x00	Programmable biquad 10, N1 coefficient byte[7:0]
0x4C	BQ10_N2_BYT1[7:0]	0x00	Programmable biquad 10, N2 coefficient byte[31:24]
0x4D	BQ10_N2_BYT2[7:0]	0x00	Programmable biquad 10, N2 coefficient byte[23:16]
0x4E	BQ10_N2_BYT3[7:0]	0x00	Programmable biquad 10, N2 coefficient byte[15:8]
0x4F	BQ10_N2_BYT4[7:0]	0x00	Programmable biquad 10, N2 coefficient byte[7:0]
0x50	BQ10_D1_BYT1[7:0]	0x00	Programmable biquad 10, D1 coefficient byte[31:24]
0x51	BQ10_D1_BYT2[7:0]	0x00	Programmable biquad 10, D1 coefficient byte[23:16]
0x52	BQ10_D1_BYT3[7:0]	0x00	Programmable biquad 10, D1 coefficient byte[15:8]
0x53	BQ10_D1_BYT4[7:0]	0x00	Programmable biquad 10, D1 coefficient byte[7:0]
0x54	BQ10_D2_BYT1[7:0]	0x00	Programmable biquad 10, D2 coefficient byte[31:24]
0x55	BQ10_D2_BYT2[7:0]	0x00	Programmable biquad 10, D2 coefficient byte[23:16]
0x56	BQ10_D2_BYT3[7:0]	0x00	Programmable biquad 10, D2 coefficient byte[15:8]
0x57	BQ10_D2_BYT4[7:0]	0x00	Programmable biquad 10, D2 coefficient byte[7:0]
0x58	BQ11_N0_BYT1[7:0]	0x7F	Programmable biquad 11, N0 coefficient byte[31:24]
0x59	BQ11_N0_BYT2[7:0]	0xFF	Programmable biquad 11, N0 coefficient byte[23:16]
0x5A	BQ11_N0_BYT3[7:0]	0xFF	Programmable biquad 11, N0 coefficient byte[15:8]
0x5B	BQ11_N0_BYT4[7:0]	0xFF	Programmable biquad 11, N0 coefficient byte[7:0]
0x5C	BQ11_N1_BYT1[7:0]	0x00	Programmable biquad 11, N1 coefficient byte[31:24]
0x5D	BQ11_N1_BYT2[7:0]	0x00	Programmable biquad 11, N1 coefficient byte[23:16]
0x5E	BQ11_N1_BYT3[7:0]	0x00	Programmable biquad 11, N1 coefficient byte[15:8]
0x5F	BQ11_N1_BYT4[7:0]	0x00	Programmable biquad 11, N1 coefficient byte[7:0]
0x60	BQ11_N2_BYT1[7:0]	0x00	Programmable biquad 11, N2 coefficient byte[31:24]
0x61	BQ11_N2_BYT2[7:0]	0x00	Programmable biquad 11, N2 coefficient byte[23:16]
0x62	BQ11_N2_BYT3[7:0]	0x00	Programmable biquad 11, N2 coefficient byte[15:8]

Table 187. Page 0x03 Programmable Coefficient Registers (continued)

0x63	BQ11_N2_BYT4[7:0]	0x00	Programmable biquad 11, N2 coefficient byte[7:0]
0x64	BQ11_D1_BYT1[7:0]	0x00	Programmable biquad 11, D1 coefficient byte[31:24]
0x65	BQ11_D1_BYT2[7:0]	0x00	Programmable biquad 11, D1 coefficient byte[23:16]
0x66	BQ11_D1_BYT3[7:0]	0x00	Programmable biquad 11, D1 coefficient byte[15:8]
0x67	BQ11_D1_BYT4[7:0]	0x00	Programmable biquad 11, D1 coefficient byte[7:0]
0x68	BQ11_D2_BYT1[7:0]	0x00	Programmable biquad 11, D2 coefficient byte[31:24]
0x69	BQ11_D2_BYT2[7:0]	0x00	Programmable biquad 11, D2 coefficient byte[23:16]
0x6A	BQ11_D2_BYT3[7:0]	0x00	Programmable biquad 11, D2 coefficient byte[15:8]
0x6B	BQ11_D2_BYT4[7:0]	0x00	Programmable biquad 11, D2 coefficient byte[7:0]
0x6C	BQ12_N0_BYT1[7:0]	0x7F	Programmable biquad 12, N0 coefficient byte[31:24]
0x6D	BQ12_N0_BYT2[7:0]	0xFF	Programmable biquad 12, N0 coefficient byte[23:16]
0x6E	BQ12_N0_BYT3[7:0]	0xFF	Programmable biquad 12, N0 coefficient byte[15:8]
0x6F	BQ12_N0_BYT4[7:0]	0xFF	Programmable biquad 12, N0 coefficient byte[7:0]
0x70	BQ12_N1_BYT1[7:0]	0x00	Programmable biquad 12, N1 coefficient byte[31:24]
0x71	BQ12_N1_BYT2[7:0]	0x00	Programmable biquad 12, N1 coefficient byte[23:16]
0x72	BQ12_N1_BYT3[7:0]	0x00	Programmable biquad 12, N1 coefficient byte[15:8]
0x73	BQ12_N1_BYT4[7:0]	0x00	Programmable biquad 12, N1 coefficient byte[7:0]
0x74	BQ12_N2_BYT1[7:0]	0x00	Programmable biquad 12, N2 coefficient byte[31:24]
0x75	BQ12_N2_BYT2[7:0]	0x00	Programmable biquad 12, N2 coefficient byte[23:16]
0x76	BQ12_N2_BYT3[7:0]	0x00	Programmable biquad 12, N2 coefficient byte[15:8]
0x77	BQ12_N2_BYT4[7:0]	0x00	Programmable biquad 12, N2 coefficient byte[7:0]
0x78	BQ12_D1_BYT1[7:0]	0x00	Programmable biquad 12, D1 coefficient byte[31:24]
0x79	BQ12_D1_BYT2[7:0]	0x00	Programmable biquad 12, D1 coefficient byte[23:16]
0x7A	BQ12_D1_BYT3[7:0]	0x00	Programmable biquad 12, D1 coefficient byte[15:8]
0x7B	BQ12_D1_BYT4[7:0]	0x00	Programmable biquad 12, D1 coefficient byte[7:0]
0x7C	BQ12_D2_BYT1[7:0]	0x00	Programmable biquad 12, D2 coefficient byte[31:24]
0x7D	BQ12_D2_BYT2[7:0]	0x00	Programmable biquad 12, D2 coefficient byte[23:16]
0x7E	BQ12_D2_BYT3[7:0]	0x00	Programmable biquad 12, D2 coefficient byte[15:8]
0x7F	BQ12_D2_BYT4[7:0]	0x00	Programmable biquad 12, D2 coefficient byte[7:0]

8.6.2.3 Programmable Coefficient Registers: Page = 0x04

This register page (shown in Table 188) consists of the programmable coefficients for mixer 1 to mixer 4 and the first-order IIR filter. All mixer coefficients are 32-bit, two's complement numbers using a 1.31 number format. The value of 0x7FFFFFFF is equivalent to +1 (0-dB gain), the value 0x00000000 is equivalent to mute (zero data) and all values in between set the mixer attenuation computed using Equation 4. If the MSB is set to '1' then the attenuation remains the same but the signal phase is inverted. All IIR filter programmable coefficients are 32-bit, two's complement numbers. For a successful coefficient register transaction, the host device must write and read all four bytes starting with the most significant byte (BYT1) for a target coefficient register transaction. When using SPI for a coefficient register read transaction, the device transits the first byte as a dummy read byte; therefore, the host must read five bytes, including the first dummy read byte and the last four bytes corresponding to the coefficient register value starting with the most significant byte (BYT1).

$$\text{hex2dec (value)} / 2^{31} \quad (4)$$

Table 188. Page 0x04 Programmable Coefficient Registers

ADDR	REGISTER	RESET	DESCRIPTION
0x00	PAGE[7:0]	0x00	Device page register
0x08	MIX1_CH1_BYT1[7:0]	0x7F	Digital mixer 1, channel 1 coefficient byte[31:24]
0x09	MIX1_CH1_BYT2[7:0]	0xFF	Digital mixer 1, channel 1 coefficient byte[23:16]
0x0A	MIX1_CH1_BYT3[7:0]	0xFF	Digital mixer 1, channel 1 coefficient byte[15:8]
0x0B	MIX1_CH1_BYT4[7:0]	0xFF	Digital mixer 1, channel 1 coefficient byte[7:0]
0x0C	MIX1_CH2_BYT1[7:0]	0x00	Digital mixer 1, channel 2 coefficient byte[31:24]
0x0D	MIX1_CH2_BYT2[7:0]	0x00	Digital mixer 1, channel 2 coefficient byte[23:16]
0x0E	MIX1_CH2_BYT3[7:0]	0x00	Digital mixer 1, channel 2 coefficient byte[15:8]
0x0F	MIX1_CH2_BYT4[7:0]	0x00	Digital mixer 1, channel 2 coefficient byte[7:0]
0x10	MIX1_CH3_BYT1[7:0]	0x00	Digital mixer 1, channel 3 coefficient byte[31:24]
0x11	MIX1_CH3_BYT2[7:0]	0x00	Digital mixer 1, channel 3 coefficient byte[23:16]
0x12	MIX1_CH3_BYT3[7:0]	0x00	Digital mixer 1, channel 3 coefficient byte[15:8]
0x13	MIX1_CH3_BYT4[7:0]	0x00	Digital mixer 1, channel 3 coefficient byte[7:0]
0x14	MIX1_CH4_BYT1[7:0]	0x00	Digital mixer 1, channel 4 coefficient byte[31:24]
0x15	MIX1_CH4_BYT2[7:0]	0x00	Digital mixer 1, channel 4 coefficient byte[23:16]
0x16	MIX1_CH4_BYT3[7:0]	0x00	Digital mixer 1, channel 4 coefficient byte[15:8]
0x17	MIX1_CH4_BYT4[7:0]	0x00	Digital mixer 1, channel 4 coefficient byte[7:0]
0x18	MIX2_CH1_BYT1[7:0]	0x00	Digital mixer 2, channel 1 coefficient byte[31:24]
0x19	MIX2_CH1_BYT2[7:0]	0x00	Digital mixer 2, channel 1 coefficient byte[23:16]
0x1A	MIX2_CH1_BYT3[7:0]	0x00	Digital mixer 2, channel 1 coefficient byte[15:8]
0x1B	MIX2_CH1_BYT4[7:0]	0x00	Digital mixer 2, channel 1 coefficient byte[7:0]
0x1C	MIX2_CH2_BYT1[7:0]	0x7F	Digital mixer 2, channel 2 coefficient byte[31:24]
0x1D	MIX2_CH2_BYT2[7:0]	0xFF	Digital mixer 2, channel 2 coefficient byte[23:16]
0x1E	MIX2_CH2_BYT3[7:0]	0xFF	Digital mixer 2, channel 2 coefficient byte[15:8]
0x1F	MIX2_CH2_BYT4[7:0]	0xFF	Digital mixer 2, channel 2 coefficient byte[7:0]
0x20	MIX2_CH3_BYT1[7:0]	0x00	Digital mixer 2, channel 3 coefficient byte[31:24]
0x21	MIX2_CH3_BYT2[7:0]	0x00	Digital mixer 2, channel 3 coefficient byte[23:16]
0x22	MIX2_CH3_BYT3[7:0]	0x00	Digital mixer 2, channel 3 coefficient byte[15:8]
0x23	MIX2_CH3_BYT4[7:0]	0x00	Digital mixer 2, channel 3 coefficient byte[7:0]
0x24	MIX2_CH4_BYT1[7:0]	0x00	Digital mixer 2, channel 4 coefficient byte[31:24]
0x25	MIX2_CH4_BYT2[7:0]	0x00	Digital mixer 2, channel 4 coefficient byte[23:16]
0x26	MIX2_CH4_BYT3[7:0]	0x00	Digital mixer 2, channel 4 coefficient byte[15:8]
0x27	MIX2_CH4_BYT4[7:0]	0x00	Digital mixer 2, channel 4 coefficient byte[7:0]
0x28	MIX3_CH1_BYT1[7:0]	0x00	Digital mixer 3, channel 1 coefficient byte[31:24]
0x29	MIX3_CH1_BYT2[7:0]	0x00	Digital mixer 3, channel 1 coefficient byte[23:16]
0x2A	MIX3_CH1_BYT3[7:0]	0x00	Digital mixer 3, channel 1 coefficient byte[15:8]
0x2B	MIX3_CH1_BYT4[7:0]	0x00	Digital mixer 3, channel 1 coefficient byte[7:0]
0x2C	MIX3_CH2_BYT1[7:0]	0x00	Digital mixer 3, channel 2 coefficient byte[31:24]
0x2D	MIX3_CH2_BYT2[7:0]	0x00	Digital mixer 3, channel 2 coefficient byte[23:16]

Table 188. Page 0x04 Programmable Coefficient Registers (continued)

0x2E	MIX3_CH2_BYT3[7:0]	0x00	Digital mixer 3, channel 2 coefficient byte[15:8]
0x2F	MIX3_CH2_BYT4[7:0]	0x00	Digital mixer 3, channel 2 coefficient byte[7:0]
0x30	MIX3_CH3_BYT1[7:0]	0x7F	Digital mixer 3, channel 3 coefficient byte[31:24]
0x31	MIX3_CH3_BYT2[7:0]	0xFF	Digital mixer 3, channel 3 coefficient byte[23:16]
0x32	MIX3_CH3_BYT3[7:0]	0xFF	Digital mixer 3, channel 3 coefficient byte[15:8]
0x33	MIX3_CH3_BYT4[7:0]	0xFF	Digital mixer 3, channel 3 coefficient byte[7:0]
0x34	MIX3_CH4_BYT1[7:0]	0x00	Digital mixer 3, channel 4 coefficient byte[31:24]
0x35	MIX3_CH4_BYT2[7:0]	0x00	Digital mixer 3, channel 4 coefficient byte[23:16]
0x36	MIX3_CH4_BYT3[7:0]	0x00	Digital mixer 3, channel 4 coefficient byte[15:8]
0x37	MIX3_CH4_BYT4[7:0]	0x00	Digital mixer 3, channel 4 coefficient byte[7:0]
0x38	MIX4_CH1_BYT1[7:0]	0x00	Digital mixer 4, channel 1 coefficient byte[31:24]
0x39	MIX4_CH1_BYT2[7:0]	0x00	Digital mixer 4, channel 1 coefficient byte[23:16]
0x3A	MIX4_CH1_BYT3[7:0]	0x00	Digital mixer 4, channel 1 coefficient byte[15:8]
0x3B	MIX4_CH1_BYT4[7:0]	0x00	Digital mixer 4, channel 1 coefficient byte[7:0]
0x3C	MIX4_CH2_BYT1[7:0]	0x00	Digital mixer 4, channel 2 coefficient byte[31:24]
0x3D	MIX4_CH2_BYT2[7:0]	0x00	Digital mixer 4, channel 2 coefficient byte[23:16]
0x3E	MIX4_CH2_BYT3[7:0]	0x00	Digital mixer 4, channel 2 coefficient byte[15:8]
0x3F	MIX4_CH2_BYT4[7:0]	0x00	Digital mixer 4, channel 2 coefficient byte[7:0]
0x40	MIX4_CH3_BYT1[7:0]	0x00	Digital mixer 4, channel 3 coefficient byte[31:24]
0x41	MIX4_CH3_BYT2[7:0]	0x00	Digital mixer 4, channel 3 coefficient byte[23:16]
0x42	MIX4_CH3_BYT3[7:0]	0x00	Digital mixer 4, channel 3 coefficient byte[15:8]
0x43	MIX4_CH3_BYT4[7:0]	0x00	Digital mixer 4, channel 3 coefficient byte[7:0]
0x44	MIX4_CH4_BYT1[7:0]	0x7F	Digital mixer 4, channel 4 coefficient byte[31:24]
0x45	MIX4_CH4_BYT2[7:0]	0xFF	Digital mixer 4, channel 4 coefficient byte[23:16]
0x46	MIX4_CH4_BYT3[7:0]	0xFF	Digital mixer 4, channel 4 coefficient byte[15:8]
0x47	MIX4_CH4_BYT4[7:0]	0xFF	Digital mixer 4, channel 4 coefficient byte[7:0]
0x48	IIR_N0_BYT1[7:0]	0x7F	Programmable first-order IIR, N0 coefficient byte[31:24]
0x49	IIR_N0_BYT2[7:0]	0xFF	Programmable first-order IIR, N0 coefficient byte[23:16]
0x4A	IIR_N0_BYT3[7:0]	0xFF	Programmable first-order IIR, N0 coefficient byte[15:8]
0x4B	IIR_N0_BYT4[7:0]	0xFF	Programmable first-order IIR, N0 coefficient byte[7:0]
0x4C	IIR_N1_BYT1[7:0]	0x00	Programmable first-order IIR, N1 coefficient byte[31:24]
0x4D	IIR_N1_BYT2[7:0]	0x00	Programmable first-order IIR, N1 coefficient byte[23:16]
0x4E	IIR_N1_BYT3[7:0]	0x00	Programmable first-order IIR, N1 coefficient byte[15:8]
0x4F	IIR_N1_BYT4[7:0]	0x00	Programmable first-order IIR, N1 coefficient byte[7:0]
0x50	IIR_D1_BYT1[7:0]	0x00	Programmable first-order IIR, D1 coefficient byte[31:24]
0x51	IIR_D1_BYT2[7:0]	0x00	Programmable first-order IIR, D1 coefficient byte[23:16]
0x52	IIR_D1_BYT3[7:0]	0x00	Programmable first-order IIR, D1 coefficient byte[15:8]
0x53	IIR_D1_BYT4[7:0]	0x00	Programmable first-order IIR, D1 coefficient byte[7:0]