CHALMERS
Department of Computer Science and Engineering

2022-09-29

DAT094
Introduction to Electronic System Design
Files in common_files

Lab 4

Common_files

Files additional to the MAC filter files that are needed in the total_system

Files

`sample_clock.vhdl` – the sample clock in the system (default 40 kHz)

`SPI_clock.vhdl.do` – the SPI transfer clock in the system (default 2 MHz

`SPI_AD.vhdl` – communication with the ADC using a SPI interface

`SPI_DA.vhdl` – communication with the DAAC using a SPI interface