default:

Timing

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00 ns	6.912 ns	2.70 ns

Latency

Summary

Latency (cycles)		Latency (absolute)		Interval (cycles)		
min	max	min	max	min	max	Type
91	91	0.910 us	0.910 us	92	92	no

Detail

Utilization Estimates

Summary

Name	BRAM_18K	DSP	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	0	78	-
FIFO	-	-	-	-	-
Instance	2	3	556	476	-
Memory	-	-	-	-	-
Multiplexer	-	-	-	45	-
Register	-	-	70	-	-
Total	2	3	626	599	0
Available	120	80	35200	17600	0
Utilization (%)	1	3	1	3	0

Pipeline:

Timing

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00 ns	6.912 ns	2.70 ns

Latency

Summary

Latency (cycles)		Latency (absolute)		Interval (cycles)		
min	max	min	max	min	max	Type
87	87	0.870 us	0.870 us	81	81	yes

Detail

Instance

Loop

Utilization Estimates

Summary

Name	BRAM_18K	DSP	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	0	1278	-
FIFO	-	-	-	-	-
Instance	2	3	362	233	-
Memory	-	-	-	-	-
Multiplexer	-	-	-	866	-
Register	-	-	1395	-	-
Total	2	3	1757	2377	0
Available	120	80	35200	17600	0
Utilization (%)	1	3	4	13	0

Dataflow:

Timing

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00 ns	6.912 ns	2.70 ns

Latency

Summary

Latency (cycles)		Latency (absolute)		Interval (cycles)		
min	max	min	max	min	max	Type
87	87	0.870 us	0.870 us	88	88	dataflow

Detail

Instance

Loop

Utilization Estimates

Summary

Name	BRAM_18K	DSP	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	0	12	-
FIFO	-	-	297	204	-
Instance	2	3	730	698	-
Memory	-	-	-	-	-
Multiplexer	-	-	-	18	-
Register	-	-	2	-	-
Total	2	3	1029	932	0
Available	120	80	35200	17600	0
Utilization (%)	1	3	2	5	0

Loop unroll:
factor = 1

Timing

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00 ns	8.151 ns	2.70 ns

Latency

Summary

Latency (cycles)		Latency (absolute)		Interval (cycles)		
min	max	min	max	min	max	Type
115	115	1.150 us	1.150 us	116	116	no

Detail

Instance

Loop

Utilization Estimates

Summary

Name	BRAM_18K	DSP	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	0	110	-
FIFO	-	-	-	-	-
Instance	2	3	957	1330	-
Memory	-	-	-	-	-
Multiplexer	-	-	-	45	-
Register	-	-	135	-	-
Total	2	3	1092	1485	0
Available	120	80	35200	17600	0
Utilization (%)	1	3	3	8	0

factor = 2

Timing

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00 ns	6.912 ns	2.70 ns

Latency

Summary

Latency (cycles)		Latency (absolute)		Interval (cycles)		
min	max	min	max	min	max	Type
146	146	1.460 us	1.460 us	147	147	no

Detail

Instance

Loop

Utilization Estimates

Summary

Name	BRAM_18K	DSP	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	0	78	-
FIFO	-	-	-	-	-
Instance	2	3	1928	1638	-
Memory	-	-	-	-	-
Multiplexer	-	-	-	392	-
Register	-	-	94	-	-
Total	2	3	2022	2108	0
Available	120	80	35200	17600	0
Utilization (%)	1	3	5	11	0

ARRAY_PARTITION

Timing

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00 ns	6.912 ns	2.70 ns

Latency

Summary

Latency (cycles)		Latency (absolute)		Interval (cycles)		
min	max	min	max	min	max	Type
20	20	0.200 us	0.200 us	21	21	no

Detail

Instance

Loop

Utilization Estimates

Summary

Name	BRAM_18K	DSP	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	0	78	-
FIFO	-	-	-	-	-
Instance	0	3	1312	1252	-
Memory	-	-	-	-	-
Multiplexer	-	-	-	45	-
Register	-	-	70	-	-
Total	0	3	1382	1375	0
Available	120	80	35200	17600	0
Utilization (%)	0	3	3	7	0

Array reshape:

Timing

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00 ns	6.912 ns	2.70 ns

Latency

Summary

Latency (cycles)		Latency (absolute)		Interval (cycles)		
min	max	min	max	min	max	Type
91	91	0.910 us	0.910 us	92	92	no

Detail

Instance

Loop

Utilization Estimates

Summary

Name	BRAM_18K	DSP	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	0	78	-
FIFO	-	-	-	-	-
Instance	16	3	842	1555	-
Memory	-	-	-	-	-
Multiplexer	-	-	-	45	-
Register	-	-	70	-	-
Total	16	3	912	1678	0
Available	120	80	35200	17600	0
Utilization (%)	13	3	2	9	0

Array partition and pipelining:

Timing

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00 ns	6.912 ns	2.70 ns

Latency

Summary

Latency (cycles)		Latency (absolute)		Interval (cycles)		
min	max	min	max	min	max	Type
15	15	0.150 us	0.150 us	9	9	yes

Detail

Instance

Loop

Utilization Estimates

Summary

Name	BRAM_18K	DSP	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	0	2458	-
FIFO	-	-	-	-	-
Instance	0	3	1002	838	-
Memory	-	-	-	-	-
Multiplexer	-	-	-	562	-
Register	-	-	1835	-	-
Total	0	3	2837	3858	0
Available	120	80	35200	17600	0
Utilization (%)	0	3	8	21	0

Array partition and dataflow

Timing

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00 ns	6.912 ns	2.70 ns

Latency

Summary

Latency (cycles)		Latency (absolute)		Interval (cycles)		
min	max	min	max	min	max	Type
16	16	0.160 us	0.160 us	17	17	dataflow

Detail

Instance

Loop

Utilization Estimates

Summary

Name	BRAM_18K	DSP	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	0	12	-
FIFO	-	-	297	204	-
Instance	0	3	1487	1474	-
Memory	-	-	-	-	-
Multiplexer	-	-	-	18	-
Register	-	-	2	-	-
Total	0	3	1786	1708	0
Available	120	80	35200	17600	0
Utilization (%)	0	3	5	9	0

Array Partition, pipeline and array reshape:

Timing

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00 ns	6.912 ns	2.70 ns

Latency

Summary

Latency (cycles)		Latency (absolute)		Interval (cycles)		
min	max	min	max	min	max	Type
8	8	80.000 ns	80.000 ns	2	2	yes

Detail

Instance

Loop

Utilization Estimates

Summary

Name	BRAM_18K	DSP	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	0	2682	-
FIFO	-	-	-	-	-
Instance	0	3	2928	5347	-
Memory	-	-	-	-	-
Multiplexer	-	-	-	46	-
Register	-	-	2215	32	-
Total	0	3	5143	8107	0
Available	120	80	35200	17600	0
Utilization (%)	0	3	14	46	0