Digital Clock, Alarm & Chronometer

Team Current Comedian

INEL5206-040H

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Project Overview

Objectives:

- The primary objective of this project is to accurately display time in hours, minutes, and seconds, and update it in real-time using the Basys3 FPGA.
- This board provides switches, buttons, and LED displays that serve as the user interface so they can control the settings of the clock.
- We will use the seven-segment displays of the board to visually represent the time in a human-readable format.
- The program will have a clock, an alarm and a chronometer.

Project Description

The digital clock and alarm system must have a setting mode to configure the clock's time and the time when the alarm will be set off. Time needs to be displayed on the seven-segment LED display of the Basys3 board, showing the hours and the minutes. The digital clock must utilize one of the two-hour time formats and the alarm itself should be a sound alarm via a small buzzer and 3 LEDs that will be connected to the Basys3 board itself. Once the alarm is set to the desired hour, the alarm will go off when the clock reaches the set time. The clock will count every second. Also, it will have a feature that you can postpone for 5 minutes the alarm, a Daylight Savings Time Setting, a chronometer mode, and the clock can be configurable to 24 or 12-hours clock.

Poster


Team Current Comedian
DIGITAL CLOCK & ALARM
02:45 AM
24°C
In the realm of digital electronics and FPGA programming, creating a digital clock is a quintessential project that combines fundamental concepts of hardware design and real-time systems. The project at hand is the implementation of a digital clock using Verilog hardware description language to program the Basys 3 Board on Vivado. Our objective is to design a digital clock that works as a, clock, an alarm using sound alert, lights and implement other features.This project will have several states being a clock, a clock alarm, a chronometer, a Daylight Saving setting, snooze the alarm for 5 min, and 24 or 12 hours clock configuration to achieve the purpose of this project and the course.
Press Signal
FPGA BASYS3
Buttons and Switches
Seven-Segment Display
Clock, Alarm & Chronometer porgram
LEDs
Speaker
RGB LEDs
Members
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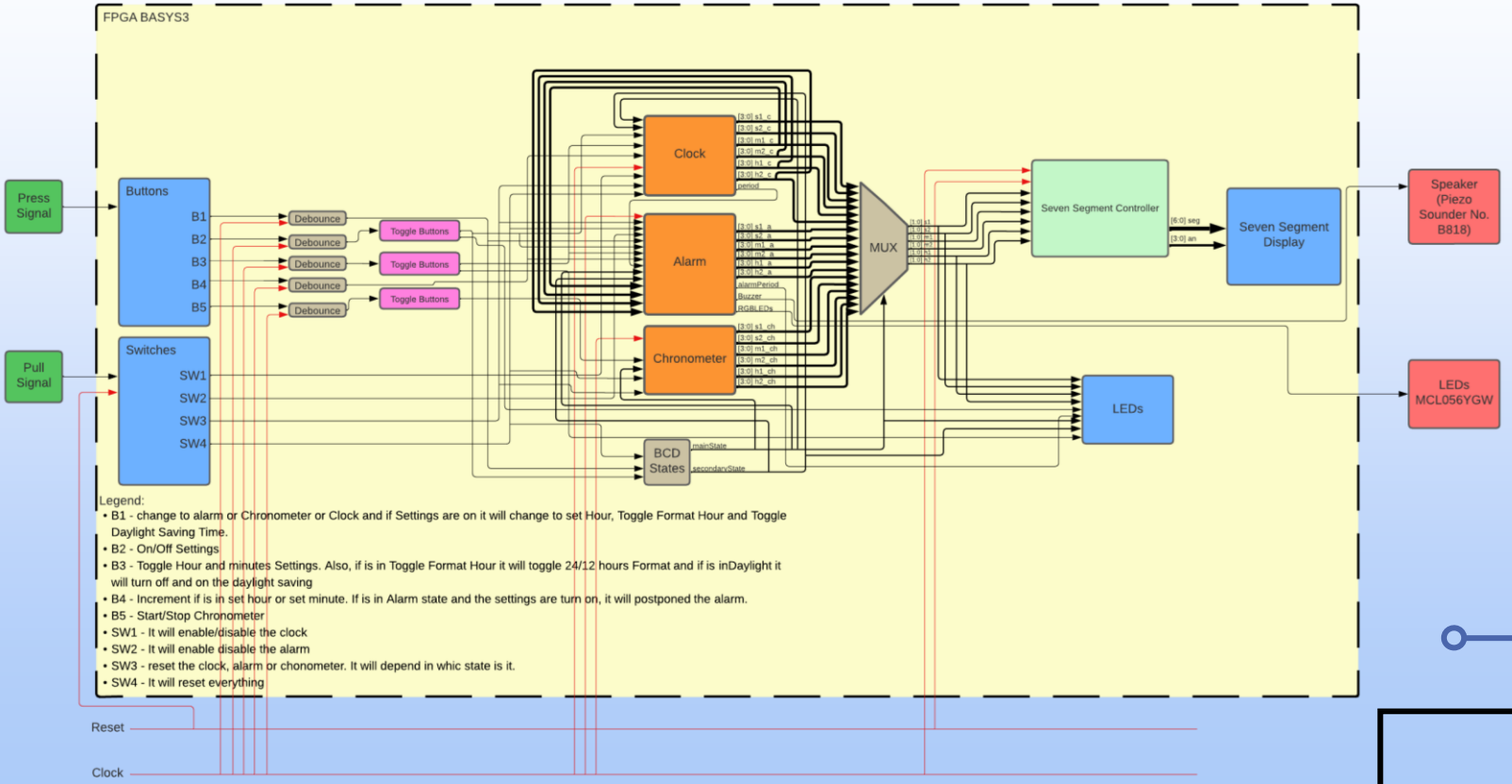
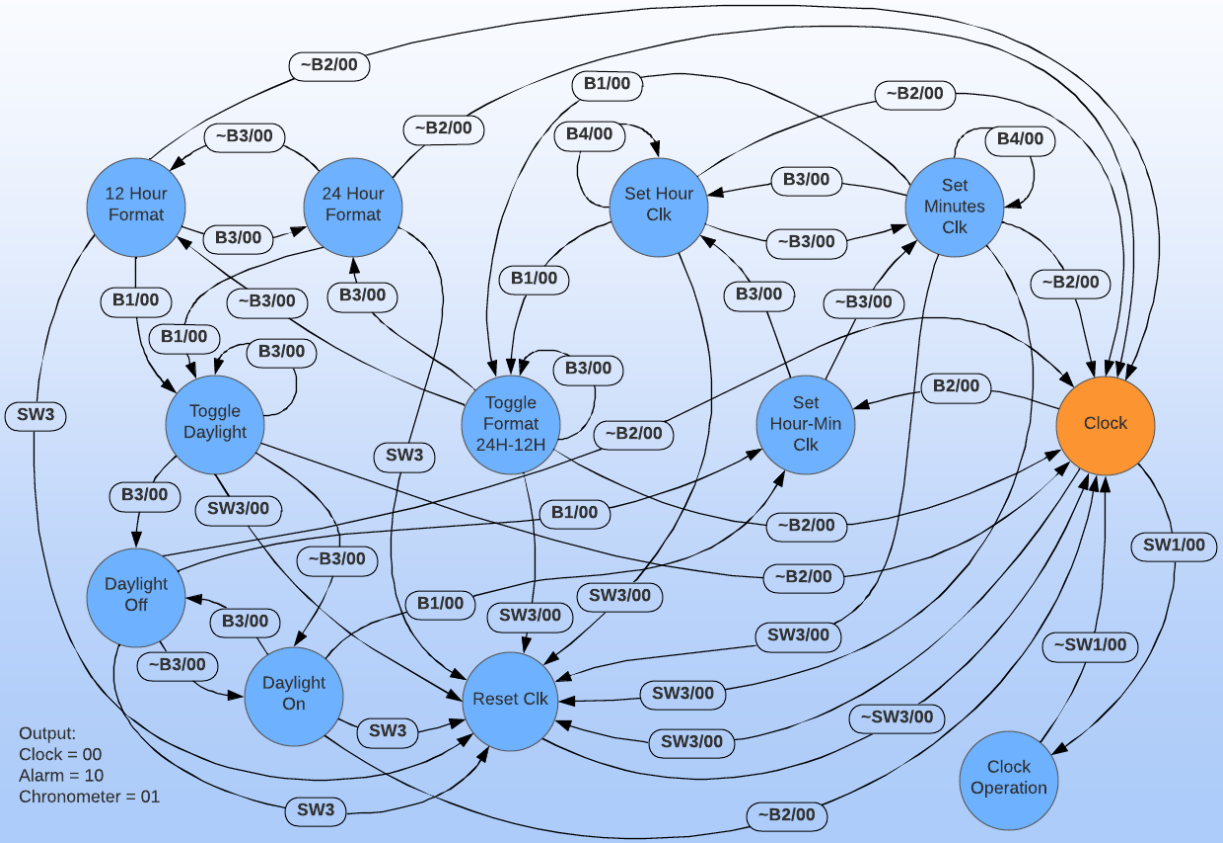
Block Diagram: System Architecture



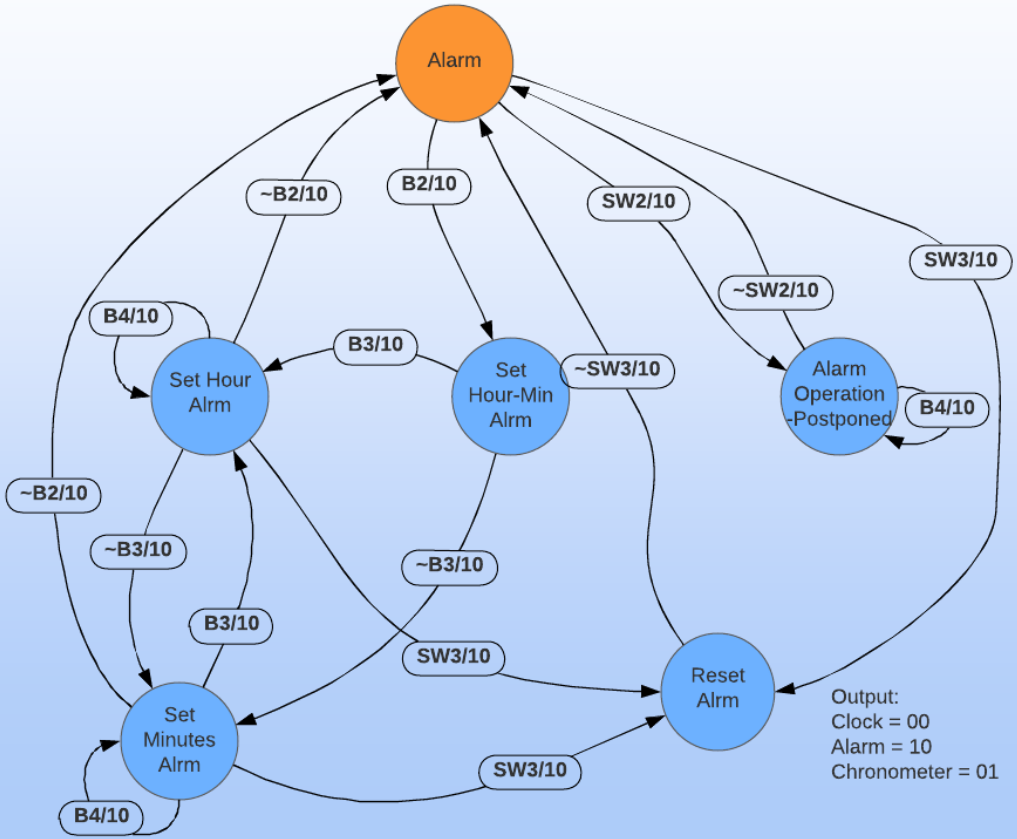
Legend:

- B1 - change to alarm or Chronometer or Clock and if Settings are on it will change to set Hour, Toggle Format Hour and Toggle Daylight Saving Time.
- B2 - On/Off Settings
- B3 - Toggle Hour and minutes Settings. Also, if is in Toggle Format Hour it will toggle 24/12 hours Format and if is inDaylight it will turn off and on the daylight saving
- B4 - Increment if is in set hour or set minute. If is in Alarm state and the settings are turn on, it will postponed the alarm.
- B5 - Start/Stop Chronometer
- SW1 - It will enable/disable the clock
- SW2 - It will enable disable the alarm
- SW3 - reset the clock, alarm or chonometer. It will depend in whic state is it.
- SW4 - It will reset everything

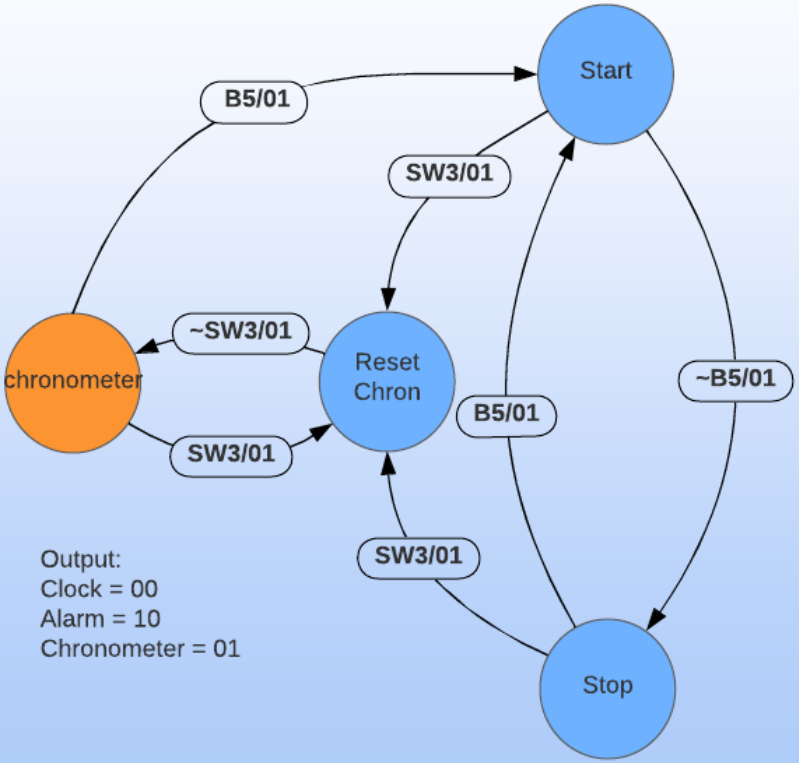
Clock State Diagram



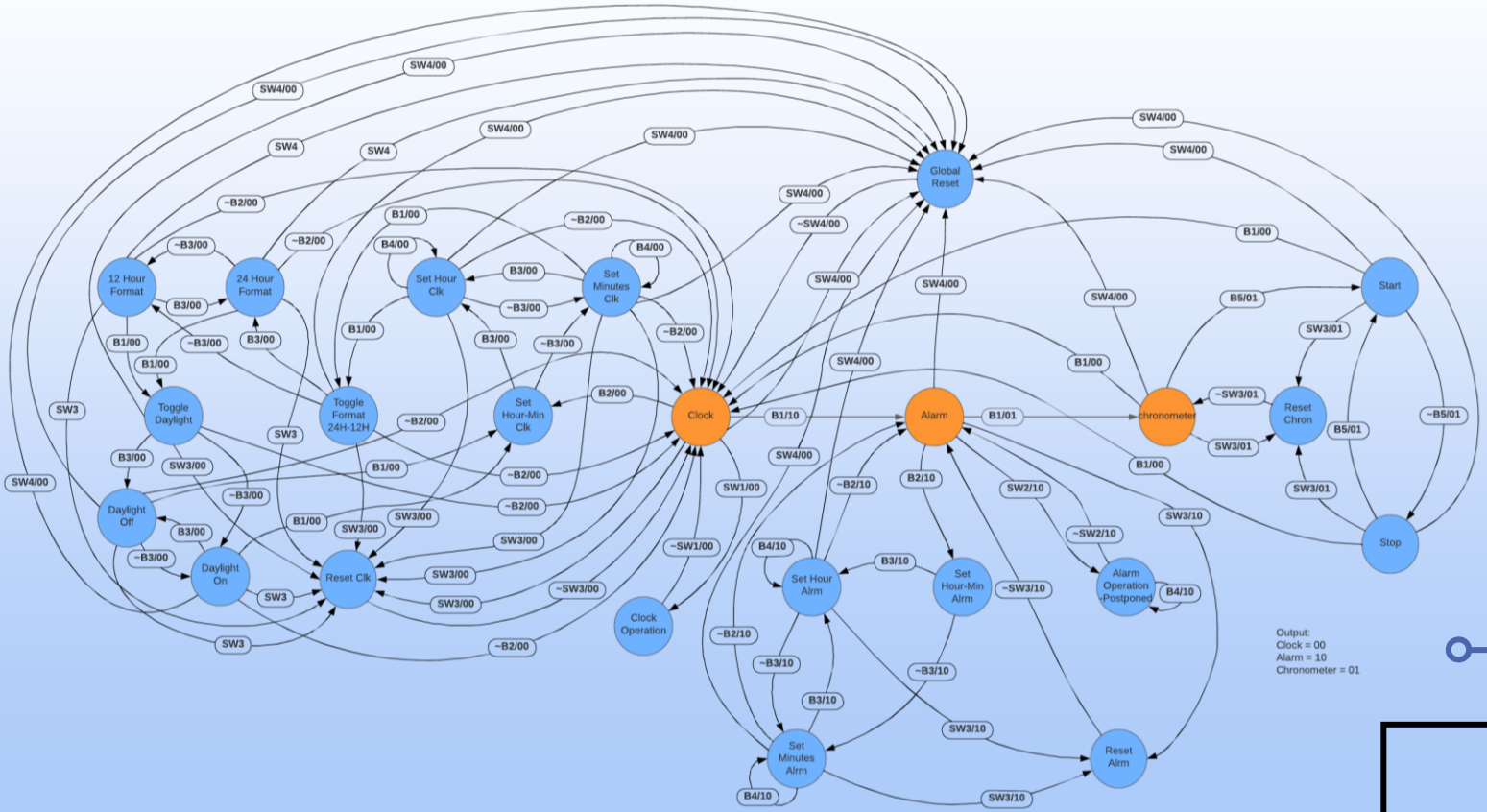
Alarm State Diagram



Chronometer State Diagram



State Diagram



State Table

Present State	Input															
	B1	B2	B3	B4	B5	~B2	~B3	~B5	SW1	SW2	SW3	SW4	~SW1	~SW2	~SW3	~SW4
Clock	Alarm/10	Set Hour-Min Clk/00	-	-	-	-	-	-	Clock Operation/00		-	Global Reset/00	-	-	-	-
Set Hour -Min Clk	-	-	Set Minutes Clk/00	-	-	-	Set Hour Clk/00	-	-	-	-	-	-	-	-	-
Set minutes Clk	Toggle Format 24H-12H/00	-	Set Hour Clk/00	Set Minutes Clk/00	-	Clock/00	-	-	-	-	Reset Clk/00	Global Reset/00	-	-	-	-
Set Hour Clk	Toggle Format 24H-12H/00	-	-	Set Hour Clk/00	-	Clock/00	Set Minutes Clk/00	-	-	-	Reset Clk/00	Global Reset/00	-	-	-	-
Toggle Format 24H-12-H	Toggle Daylight/ 00	-	Toggle Format 24H-12H/00	-	-	Clock/00	-	-	-	-	Reset Clk/00	Global Reset/00	-	-	-	-
24 Hour Format	Toggle Daylight/00	-	-	-	-	Clock/00	12 Hour Format/00	-	-	-	Reset Clk/00	Global Reset/00	-	-	-	-
12 Hour Format	Toggle Daylight/00	-	24 Hour Format/00	-	-	Clock/00	-	-	-	-	Reset Clk/00	Global Reset/00	-	-	-	-
Toggle Daylight	-	-	Daylight Off/00	-	-	Clock/00	Daylight On/00	-	-	-	Reset Clk/00	Global Reset/00	-	-	-	-
Daylight On	Set Hour-Min Clk/00	-	Daylight Off/00	-	-	Clock/00	-	-	-	-	Reset Clk/00	Global Reset/00	-	-	-	-
Daylight Off	Set Hour-Min Clk/00	-	-	-	-	Clock/00	Daylight On/00	-	-	-	Reset Clk/00	Global Reset/00	-	-	-	-
Clock Operation	-	-	-	-	-	-	-	-	-	-	Reset Clk/00	Global Reset/00	Clock/00	-	-	-
Reset Clk	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Clock/00	-
Alarm	Chronometer/10	Set Hour -min Alrm/10	-	-	-	-	-	-	-	Alarm Operation - Postponed/01	Reset Alrm/01	Global Reset/00	-	-	-	-
Set Hour/Min Alrm	-	-	Set Hour Alrm/01	-	-	-	Set Minutes Alrm/01	-	-	-	-	-	-	-	-	-
Set Hour Alrm	-	-	Set Hour Alrm/10	Set Hour Alrm/10	-	Alarm/10	-	-	-	Alarm Operation - Postponed/01	Reset Alrm/01	Global Reset/00	-	-	-	-
Set Minutes Alrm	-	-	-	Set Minutes Alrm/10	-	Alarm/10	Set Minutes Alrm/10	-	-	Alarm Operation - Postponed/10	Reset Alrm/10	Global Reset/00	-	-	-	-
Alarm Operation - Postponed	-	-	-	-	-	Alarm/10	-	-	-	-	Reset Alrm/10	Global Reset/00	-	Alarm /01	-	-
Reset Alrm	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Alarm /01	-
Chronometer	Clock/00	-	-	-	Start/01	-	-	-	-	-	Reset Chron/01	Global Reset/00	-	-	-	-
Start	Clock/00	-	-	-	-	-	-	Stop/01	-	-	Reset Chron/01	Global Reset/00	-	-	-	-
Stop	Clock/00	-	-	-	Start/01	-	-	-	-	-	Reset Chron/01	Global Reset/00	-	-	-	-
Reset Chron	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Chronometer/01	-
Global Reset	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Clock/00
	Next State/Output															

Requirements

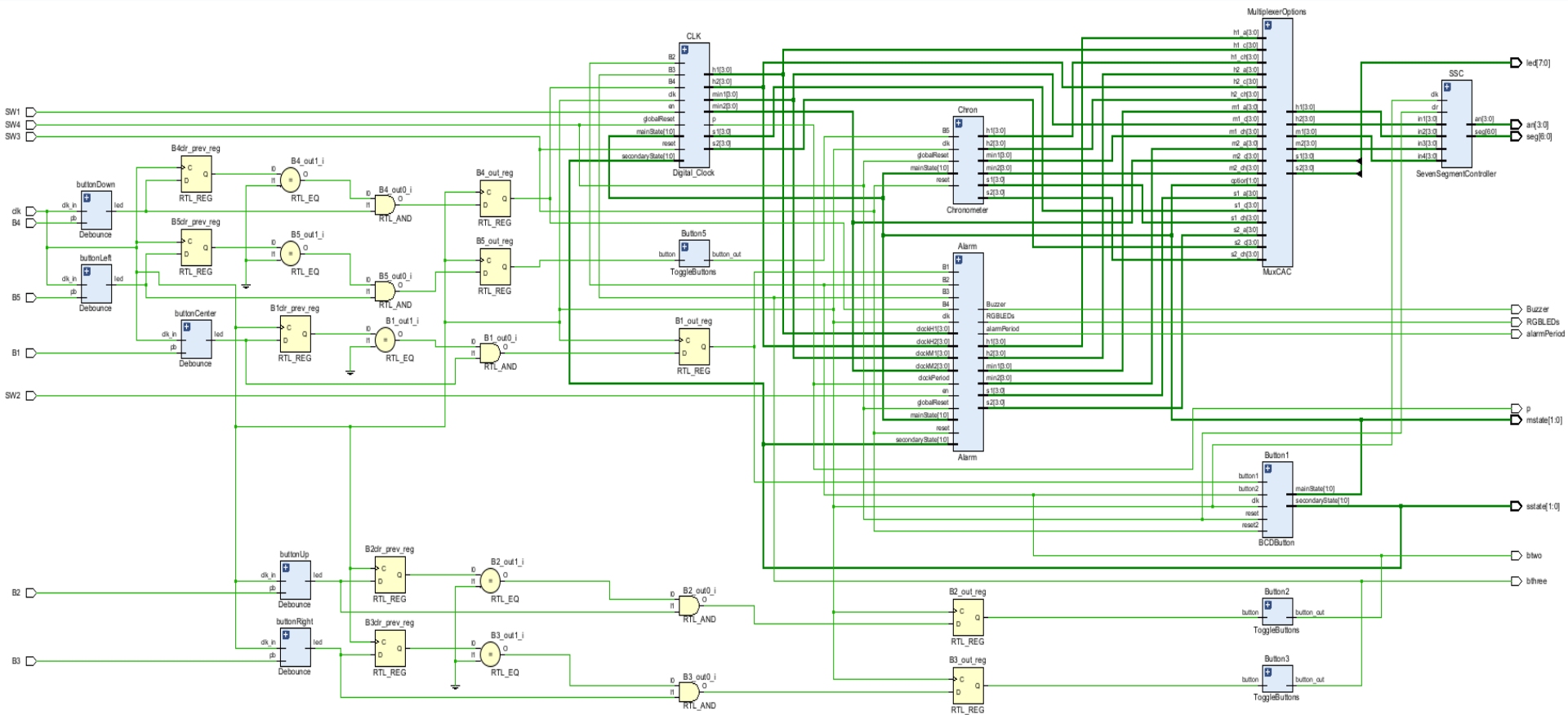
The Basys3 FPGA will be used to process the function of the clock, control, give warning and display the time using the given components:

- **Buttons and Switches:** The buttons & switches will be used to control the functions of the clock like resetting, postponed the alarm, change the hour format, activate the Daylight-Saving feature and others.
- **Seven-Segment Display**: it will display the time.
- **LEDs:** It can be used to display the seconds or to alert the user when the alarm is activated.
- **Ports:** Is going to be used to connect the speaker to the FPGA.
- **Speaker:** It will be used to produce a sound for the alarm.

The Clock functions and its features will be implemented via Hardware Description language and are the following:

- Display the time
- Reset the different states
- Works as an alarm
- Works as a chronometer
- Postpone the alarm for 5 min
- Daylight Saving Feature
- Change the format hours (24 or 12)

Schematic Diagram: Overview



Part List

Part	Part #	Quantity
Basys3 FPGA	2157531	1
Buzzer (Piezo Sounder)	B818	1
Breadboard	424-240-131	1
1kΩ Resistor	CFR-25JB-52-1K	1
LED	MCL056YGW	3

Power Analysis

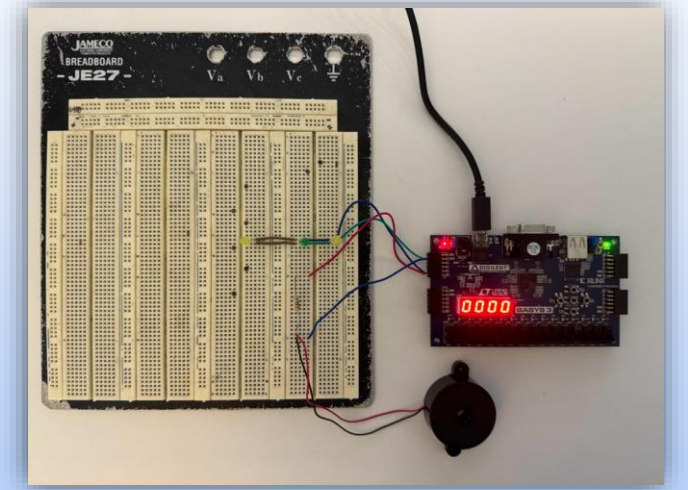
The formula used to get the power consumption per component is:
$W = W \times time(hours).$

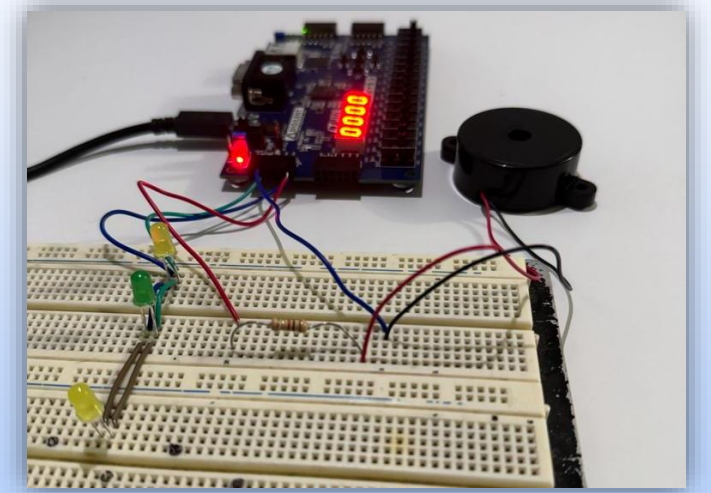
5min = 0.08333 h

If the person snoozes the alarm 6 times at 4 min and 59 sec, the total power consumption would be approximately 99.489mW/h

Component	Power Consumption (W)	Daily Usage Time (hour)	Daily Power Consumption (W/h)
Small Buzzer	0.120W	0.08333h	10mW/h
LED 1	0.018W	0.08333h	1.4994mW/h
LED 2	0.018W	0.08333h	1.4994mW/h
LED 3	0.018W	0.08333h	1.4994mW/h
Resistor	0.025W	0.08333h	2.0833mW/h
Total	0.199W		16.5815mW/h

Project Demostration





Conclusion

Parts done By:
Kevin: Overview, Poster, Chronometer, Requirements
Joseph: Project Description, Alarm, Part List, Power Analysis,
Juan: Block Diagram, Clock, State Table, Debounce, Seven Segment Controller
Group: State Diagram, Multiplexer, BCD Button, Toggle Buttons

Weakness:

- Display of the seconds in clock
- Sometimes the push buttons does not work properly
- You can save one alarm only
- Chronometer does not show the milliseconds and it display the hours in binary

Problems:

- Global button to postponed alarm
- More buttons