DANIEL DELAYO

ddelayo@cs.stonybrook.edu ⋄ danieldelayo.github.io

EDUCATION

Stony Brook University
Second Year PhD Student in Computer Science *May 2021 - Present*
B.S. in Computer Science *August 2017 - May 2021*
College of Engineering and Applied Science Honors {College, CS}, Graduated Summa Cum Laude

PUBLICATIONS

IncrementandFreeze: Every Cache, Everywhere, All of the Time (SPAA 2023)
We design and implement a parallel and cache-efficient algorithm for generating exact LRU cache hit-rate curves that runs many times faster than prior work. As cache usage patterns differ depending on time and place, useful algorithms must be fast and efficient to see widespread and frequent use.

Exact LRU hit-rate curves can be used to optimize the cost to cache content. Reducing this cost can increase the availability and accessibility of content. DOI: 10.1145/3558481.3591085

Automatic Management of High-Bandwidth Memory (SPAA 2022)
High-Bandwidth Memory is an emerging type of memory that does not fit in the standard memory hierarchy; standard caching models do not apply. We present a caching model for High-Bandwidth Memory and verify it on Intel Knight's Landing processors.

We introduce Dynamic Priority, which gives a makespan constant-competitive with optimal and outperforms standard schemes. DOI: 10.1145/3490148.3538570

Write-Optimized IP Indexer for Cyber Security (Cluster Computing 2022)
We designed expiration strategies that allow our system, Diventi, to support IP range queries in external memory with millisecond response times. Diventi automatically expires the oldest IP data without compromising query latency or ingestion rate.

This work was in collaboration with Sandia National Labs. DOI: 10.1007/s10586-021-03463-5

UPCOMING PUBLICATIONS

Efficient and Timely Queries in External Memory for Infinite Streams in Optane PMEM
We design and implement data structures for Optane PMEM to efficiently ingest cyber security data and generate timely and accurate alerts. This work is in collaboration with Sandia National Labs.

Distributed Graph Sketching at RAM bandwidth to Solve Connected Components
We design and implement Landscape, a state-of-the-art graph processor that is able to ingest up to 332 million stream updates per second on a graph of 2^{17} nodes. By leveraging linear sketching, we are able to ingest stream data at near RAM-bandwidth.

TECHNICAL STRENGTHS

Computer Science Algorithms, Data Structures, Parallelism, High-Performance Computing
Languages C++, C, Python; Familiar with Java, Prolog, SML

WORK EXPERIENCE

Stony Brook University Research Assistant Summer 2019 - Present

· Advised by Michael A. Bender on Theory, Memory Architecture, Data Structures and Algorithms.

Sandia National Labs Intern Summer 2021 - Present

· Collaborate with Sandians on the theory and implementation of Write-Optimized Data Structures to solve cyber security challenges.