

ŁÓDŹ UNIVERSITY OF TECHNOLOGY

Faculty of Electrical, Electronic,
Computer and Control Engineering

Department of Microelectronics and Computer Science

Bachelor of Engineering Thesis

**Photovoltaic module maximum power point tracker
enabling operation recording in dynamic states**

**Układ śledzenia punktu mocy maksymalnej modułu
fotowoltaicznego umożliwiający rejestrację działania w
stanach dynamicznych**

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Abstract

The purpose of the project was to enhance and expand on an existing project of maximum power point tracker (MPPT) of the photovoltaic module (PV) and make it possible to record system operation at dynamic states. Certain voltages and currents had to be recorded at high sampling frequency, in order to control the system together with medium complex algorithm of MPPT as well as send the data to external memory connected with a microcontroller. The data was supposed to be sent to the PC (once external memory is full) in order to facilitate the analysis. The entire printed circuit board (PCB) needed a redesign due to the need to refine the measurement system. The project was constructed on two dedicated circuit boards, one for the power system, and the other for the control system, with the communication based on the microcontroller. Further development with the equipment available in the laboratory of Power Devices and Systems should be possible.

All project success criteria were achieved. The measurement system was designed, simulated and implemented. PCB was redesigned, communication with external memory and PC was both implemented and tested in order to be capable of the analysis of the data on the PC. All the modules were combined and the project was confirmed to work in accordance with the assumptions.

The increasingly growing need for electric energy and the extended emphasis on environmental protection made the usage of the solar energy interesting. There is more and more scientific research regarding this topic. The aim of this work was to get acquainted with solar energy harvesting and carry out a project which would gather up disciplines related to bachelor-level studies including: C programming, microcontrollers, power conversion, PCB design, signal processing, and design of the analog and digital circuits.

Streszczenie

Celem niniejszego projektu było udoskonalenie i rozszerzenie istniejącego układu śledzenia punktu mocy maksymalnej (MPPT) modułu fotowoltaicznego oraz umożliwienie rejestracji działania urządzenia w stanach dynamicznych. Pewne napięcia oraz prądy powinny zostać zmierzone z odpowiednio krótkim odstępem czasowym, aby sterować układem używając średnio złożonego algorytmu MPPT. Dane powinny zostać wysłane do pamięci zewnętrznej połączonej z mikrokontrolerem oraz (po jej zapełnieniu) wysłane do komputera w celu ułatwienia analizy. Obwody pomiarowe powinny zostać udoskonalone, a urządzenie powinno być przeprojektowanie. Układ należało skonstruować na dwóch dedykowanych płytach drukowanych - osobnej dla obwody mocy i obwodów pomiarowych i osobnej dla układu sterowania i komunikacji opartego na mikrokontrolerze. Wybrany mikrokontroler powinien umożliwiać późniejszy rozwój oprogramowania z użyciem sprzętu dostępnego w Laboratorium elektroniki mocy.

Projekt został zakończony pomyślnie, spełniając początkowe kryteria. Nowy system pomiarowy został zaprojektowany, zasymulowany oraz zaimplementowany. Płytki drukowane zostały przeprojektowane biorąc pod uwagę potrzebę zmiany w istniejącym projekcie. Komunikacja z pamięcią zewnętrzną została przetestowana oraz zaimplementowana tak, aby umożliwić analizę danych używając komputera. Wszystkie moduły zostały ze sobą połączone, a system pracował zgodnie z początkowymi założeniami.

Ciągła potrzeba energii elektrycznej oraz nacisk na ochronę środowiska sprawiają że zainteresowanie energią odnawialną jest duże, oraz coraz więcej badań naukowych jest prowadzonych dotyczących tego tematu. Celem pracy by zapoznanie się z odborem energii słonecznej, oraz przeprowadzenia projektu, w którym można by zebrać dyscypliny związane ze studiami inżynierskimi takimi jak: programowanie w języku C, mikrokontrolery, przetwarzanie sygnałów, konwersja mocy, projektowanie płyt PCB oraz projektowanie obwodów analogowych.

Table of Contents

1.	Introduction	7
1.1.	Motivation	7
1.2.	General projects assumptions	8
1.3.	Thesis outline.....	8
1.4.	Tools	9
2.	Theoretical background.....	9
2.1.	Photovoltaic module.....	9
2.1.1.	PV electric model	9
2.1.2.	IV curve.....	10
2.1.3.	Series and parallel connection of the solar cells	11
2.1.4.	Effect of temperature on PV.....	11
2.1.5.	Effect of light intensity on PV.....	11
2.1.6.	IV curve & load.....	12
2.1.7.	Bypass diodes.....	13
2.2.	Boost converter.....	14
2.3.	Filters	15
2.3.1.	General information	15
2.3.2.	Stability	16
3.	Solar panel.....	17
3.1.	Repair.....	17
3.2.	Characteristics	17
4.	General system architecture	19
4.1.	Design of the printed circuit board (PCB).....	22
4.2.	DC-DC simulations	24
4.3.	Power supply	26
4.4.	Microcontroller.....	26

4.4.1.	Development board	27
4.4.2.	dsPIC33JF16GS502 specifications	28
5.	Measurement system.....	28
5.1.	Design.....	28
5.2.	Voltage input and output voltage filters	30
5.3.	Current input filter.....	32
5.4.	Current output filter	32
5.5.	Current of the source of the transistor filter	33
5.6.	Additional changes	35
6.	Microcontroller role	36
6.1.	Pulse width modulation (PWM)	37
6.1.1.	Clock provided for PWM	37
6.1.2.	Standard edge-aligned PWM	38
6.1.3.	Time base	38
6.2.	Hardware used for triggering.....	39
6.3.	Analog-to-digital converter (ADC)	41
6.3.1.	Conversion time	41
6.3.2.	Data collection.....	42
7.	Data recording	43
7.1.	External memory	44
7.2.	Sequential mode	45
7.2.1.	Writing	46
7.2.2.	Reading.....	47
7.3.	Coding	49
7.4.	UART - data transmission	50
7.5.	Decoding.....	51
8.	Perturb and observe algorithm (P&O)	53

9.	Tests	55
9.1.	ADC + PWM	55
9.2.	UART - byte by byte	55
9.3.	Memory test	56
9.4.	Transmission test	56
9.5.	ADC and transmission test	57
9.6.	Sequential mode test	57
9.7.	Filtering test	58
9.8.	Results	59
10.	Encountered problems	62
10.1.	Reading from SPI	62
10.2.	Unexpected instability of the opamp	63
10.3.	Unexpected data from the ADC	64
10.4.	Interferences on SPI clk pin	65
10.5.	Design of the current filters	65
10.5.	Single voltage supply	65
11.	Summary and conclusions	66
11.1.	Summary	66
11.2.	Conclusions	66
	Bibliography	67

1. Introduction

1.1. Motivation

Energy consumption is growing every year, and that trend will probably not stop in coming years. According to International Energy Outlook 2013 (IEO2013), an EIA's project (Energy Information Administration) released in 2013, world energy consumption will grow by 56 % between 2010 and 2040. The fastest-growing energy sources are renewable energy and nuclear power, each increasing 2.5 % per year [1].

Renewable energy promotion is highly supported by the European Parliament and of The Council European Union. On January 10, 2007, the European Union commission communicated a strategy to increase overall share of energy from renewable sources to 20 %, and to 10 % for energy from renewable sources in transport. Those targets refer to the context of the 20 % improvement in energy efficiency by 2020 from the “Action Plan for Energy Efficiency: Realizing the Potential” set out in 2006 [2].

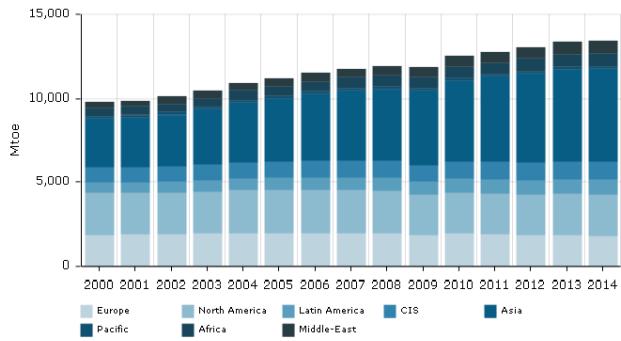


Fig. 1 – Total global energy consumption [3].

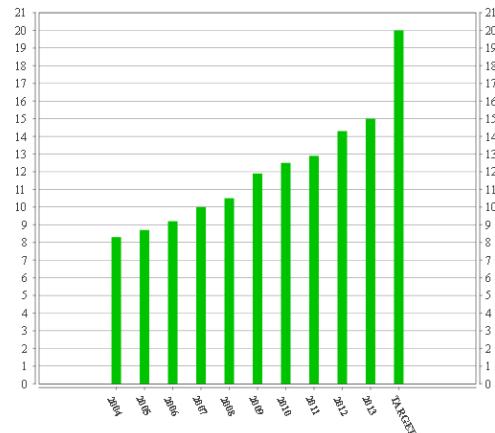


Fig. 2 – Share of renewable energy in gross final energy consumption [%] in EU (28 countries) [4].

Due to the increased interest in renewable energy, further research and investment have been directed to that field, including photovoltaic modules. Many initiatives, competitions, and research projects have been created, included the following:

- The Photovoltaic Technology Platform realizes the European Strategic Research Agenda for PV for the next decade(s);

- The World Solar Challenge is a competition for solar car efficiency (Lodz University of Technology is a participant);
- The Fraunhofer ISE achieved a new world record for both sides-contacted silicon solar cells, reaching 25.1 % efficiency with TOPCon technology [5].

Due to the fact that the European and global energy market is following this trend, I decided to have my final project related to solar energy. Not only is it possible to acquire basic knowledge, but to use learnings from my studies such as electronic power conversion, C programming, microcontrollers, PCB design, signal processing, design of analog and digital circuits in practice.

1.2. General projects assumptions

The purpose of the project was to enhance and expand on an existing project of maximum power point tracker (MPPT) of the photovoltaic module (PV) and make it possible to record system operation at dynamic states. The core of the project is the DC-DC converter that acts as virtual controllable load, together with constantly calculated control PWM signal. The PWM adjusts according to PVs current IV curve. Certain voltages and currents had to be filtered, recorded at high sampling frequency, and converted to the digital values for the further processing. These values are taken as an input for the MPPT algorithm which output appropriately calculated control signal. Concurrently, data together with the current duty cycle value should be sent to external memory connected with a microcontroller. The data had to be sent to the PC (once external memory is full) in order to facilitate the analysis. The entire printed circuit board (PCB) needed a redesign due to the need to refine the measurement system. The project had to be constructed on two dedicated circuit boards, one for the power system, and the other for the control system, with the communication based on the microcontroller. Further development with the equipment available in the laboratory of Power Devices and Systems should be possible.

1.3. Thesis outline

This thesis is divided in two main parts, theoretical and implementation. The theoretical part presents basic information about functioning of photovoltaic module, boost converter, as well as analog filter. The implementation part includes the design, explanation of the functioning of each module, as well as reason for choosing particular elements of solutions. Chapters 9 and 10 are devoted to the conducted tests and encountered problems. Chapter 11 sums up the project and includes the tips for the further data analysis.

1.4. Tools

- MPLAB IDE (C programming)
- PSpice student version (Filters simulations)
Altium Designer (PCB project)
- Scilab (Decoding data from .txt file to a final result)
- RealTerm Capture Program 2.0.0.7.0 (Saving data from external memory in text file)
- Open Office (Data results)
- Lucid chart (Creating schemes)

2. Theoretical background

2.1. Photovoltaic module

A solar cell is an electronic device, which converts sunlight into electricity. This process requires a material able to absorb the light energy in order to transfer it to the electrons. If enough energy is transferred, the electron is capable of escaping from its normal position associated with the atom and move from the solar cell into an external circuit. The electron then dissipates its energy in the external circuit and returns to the solar cell. In the vast majority of cases, the material used for photovoltaic energy conversion has the form of p-n junction [6, 7]. The generation of current is related to two key processes: creation of electron-hole pairs and the collection of these carriers by p-n junction. The former involves the absorption of the incident photons, and the latter prevents the recombination of the electron-holes pairs by using a p-n junction to spatially separate the electron and the hole [8].

2.1.1. PV electric model

Equivalent circuit models define the entire IV curve of a cell, module, or array as a function under specified conditions. One basic equivalent circuit model is the single diode model:

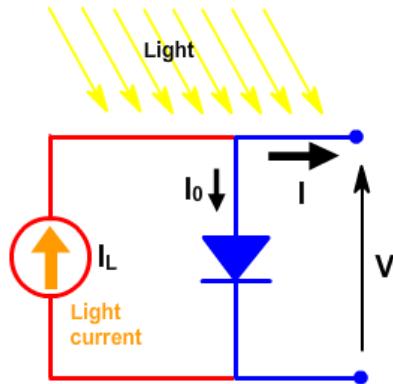


Fig. 3 - Equivalent circuit model of PV [9].

$$I = I_L - I_0 e^{\frac{qV}{nkT} - 1}$$

Eq. 1 - The equation for the IV curve in the first quadrant [9].

2.1.2. IV curve

The IV is characterized by set of points. The most important include:

- I_{sc} - the short-circuit current, highest electric current for given conditions;
- V_{oc} - the open-circuit voltage, highest electric voltage for given conditions;
- MPP - maximum power point, highest power possible for given conditions.

For a determined conditions (temperature/ irradiance), photovoltaic module (PV) exhibits specific current vs. voltage (IV curve). Due to the IV curve shape, there is always present a maximum power point (MPP) for a specific voltage V_{mpp} . Proximity of the PVs operation to the MPP is essential, because of low efficiency of conversion from solar into electrical power (around 25 %) [21].

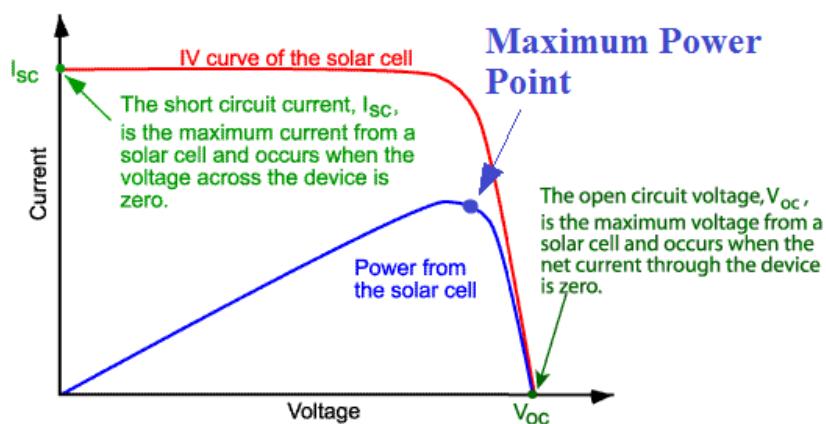


Fig. 4 - IV curve [10].

2.1.3. Series and parallel connection of the solar cells

Normally solar cells are connected to each other in series and in parallel in order to increase the possible power transfer. In series connection the voltages will be added up. When connecting panels in parallel, the voltage will remain the same, and the currents will be summed [11]. The total current is the current of an individual cell multiplied by the number of cells in parallel. The total voltage is the voltage of an individual cell multiplied by the number of cells in series [12].

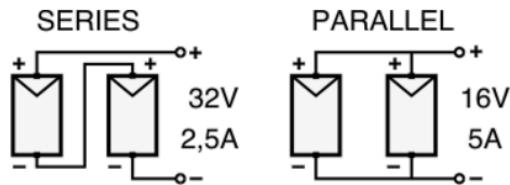


Fig. 5 - An example of two PVs (16V/2.5A) [11].

2.1.4. Effect of temperature on PV

PVs are sensitive to changes in temperature. An increase in temperature reduces the band gap of a semiconductor, which means that lower energy is needed to break the bond [13]. That will lead to a decrease in the electric field in the p-n junction and, consequently, a reduction in the voltage across the terminals of the PV.

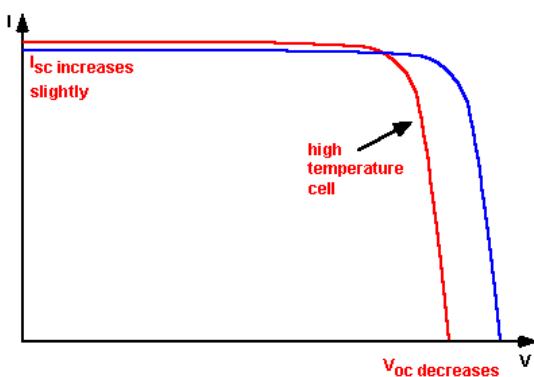


Fig. 6 - The effect of temperature on the IV characteristics of a solar cell [13].

2.1.5. Effect of light intensity on PV

Changes in the light intensity incident on a solar cell influences cells parameters. A higher light intensity produces a higher output current, and it also affects the open-circuit voltage [13].

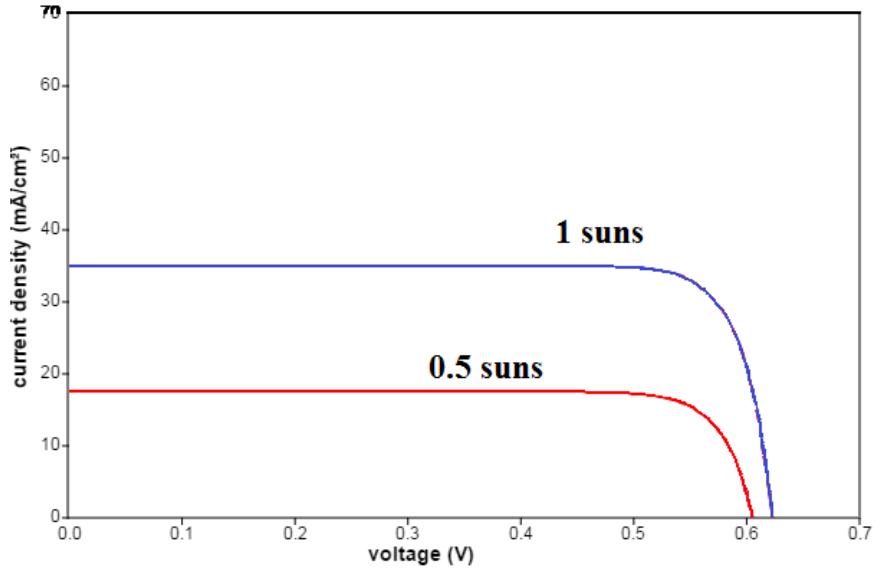


Fig. 7 - The effect of light intensity on the IV characteristics of a solar cell [13].

1 sun corresponds to standard illumination at AM1.5, or 1 kW/m^2

2.1.6. IV curve & load

If a load is connected across the terminals of a PV cell, the operating point is described by the intersection of the resistor's characteristics and the PV cell's curve (for the specific conditions). Because the IV curve of the PV is highly susceptible to many factors such as light intensity or temperature, it is impossible to adjust one specific load that would be ideal for the photovoltaic module, and it would be highly inconvenient and costly to change the load every time the PV's conditions changes. For that reason, a set of electronic circuitry may be applied that would perform the same function as a controllable, variable load. For the purpose of this project, a step-up converter is used, described further in section 4. general system architecture and 2.2. boost converter.

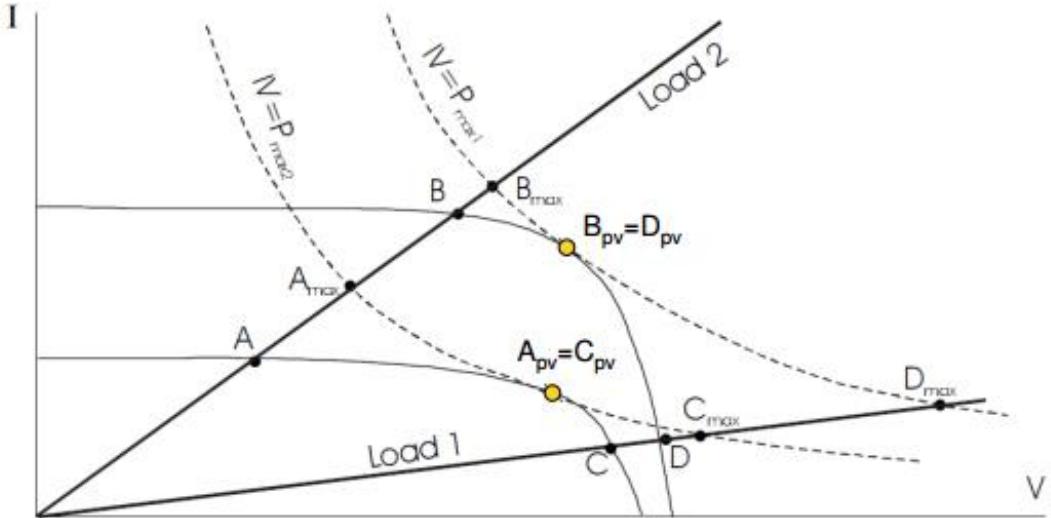


Fig. 8 - Basic PV cell operation [14].

2.1.7. Bypass diodes

For a large cell array, mismatch losses may be a serious problem under certain conditions. Match losses are caused by the interconnection of solar cells or modules which do not have identical properties or which experience different conditions. For instance, when one solar cell is shaded while the others are not. It can lead to power dissipation in the shaded cell and result in local heating that may cause irreversible damage to the module [12]. One shaded cell reduces the current through all the cells connected in the series, causing them to produce voltage that can often reverse bias the shaded cell. In order to prevent the destructive effects of hot-spot heating, one can connect bypass diodes in parallel, with opposite polarity to the solar cell. Under normal operation, each solar cell is forward biased and therefore the bypass diode will be reverse biased and behave as an open circuit. However, if a solar cell is reverse biased due to a mismatch in short-circuit current between several series connected cells, then the bypass diode conducts, allowing the current from the properly working solar cells to flow into the external circuit [15].

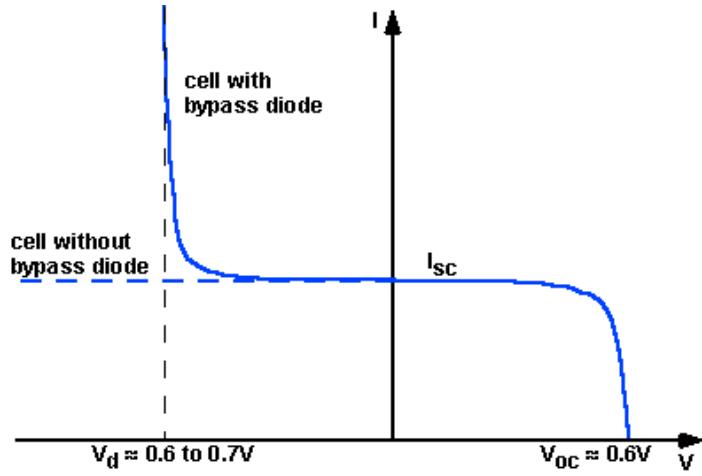


Fig. 9 - The effect of a bypass diode on an IV curve [15].

2.2. Boost converter

A boost converter is a DC-to-DC power converter with an output voltage greater than its input voltage. It is a popular non-isolated power stage topology, sometimes called a step-up power stage [16].

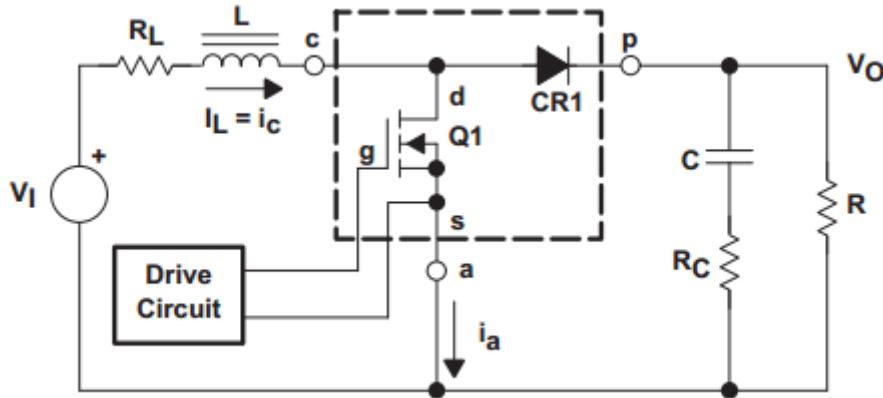


Fig. 10 - Boost power stage general schematic [16].

During the normal operation transistor is repeatedly switched on and off by control circuitry. The process can be divided into two separate stages.

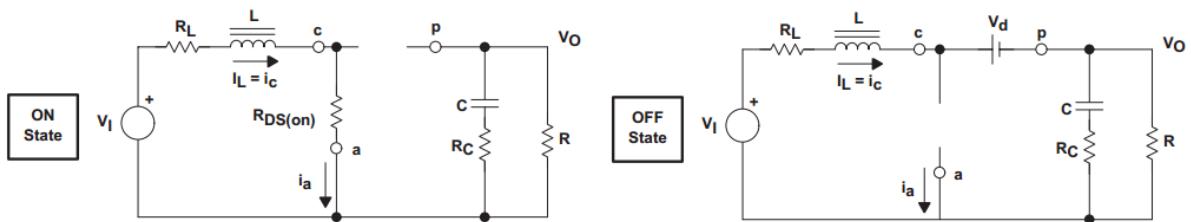


Fig. 11 - Boost power stage states [16].

When the switch is on, the diode is reverse biased, therefore acts as open circuit, isolating the output stage. The input charges the inductor. When the switch is off, the output stage receives the energy from the inductor as well as from the input. The output filter capacitor acts as a low pass filter and is assumed to be very large to ensure a constant output voltage [17].

2.3. Filters

2.3.1. General information

A filter is a device that passes electric signals at certain frequency ranges while preventing the passage of others. The most common type of filters is a low pass filter. It passes the low frequencies and attenuates the high frequency signals starting from a particular frequency, called the cut-off frequency. Unfortunately, ideal filters do not exist, and if they did, they would eliminate signals above the cut-off frequency and perfectly pass signals below. Therefore, the cut-off frequency is defined as the frequency where output power has dropped to half.

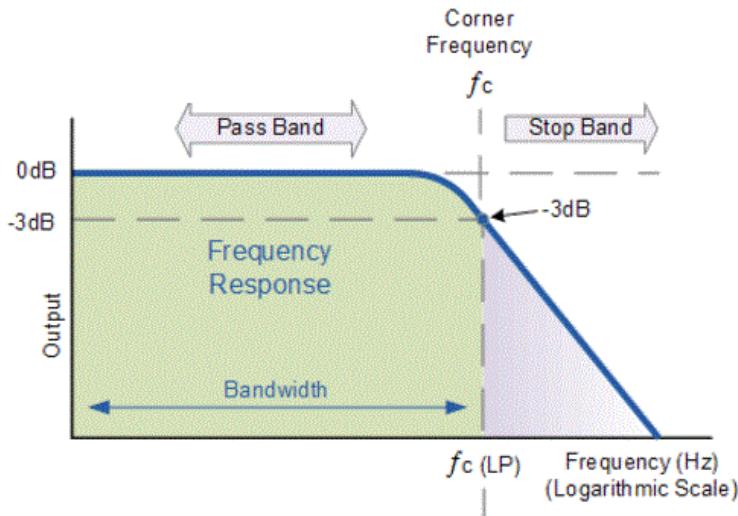


Fig. 12 - Frequency response of low-pass filter [18].

There are a vast number of possible filters types and implementations. The most common difference is the presence of opamp (operational amplifier), which is an active filter, versus topologies that consist of only passive components, such as inductors, resistors, and capacitors. Another common division is the filter order, which is linked to the shape of the filter frequency response [19].

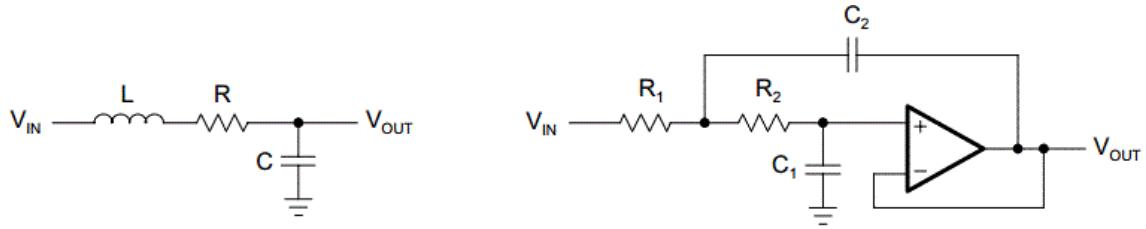


Fig. 13 - Second-order passive low-pass and second-order active low-pass [19].

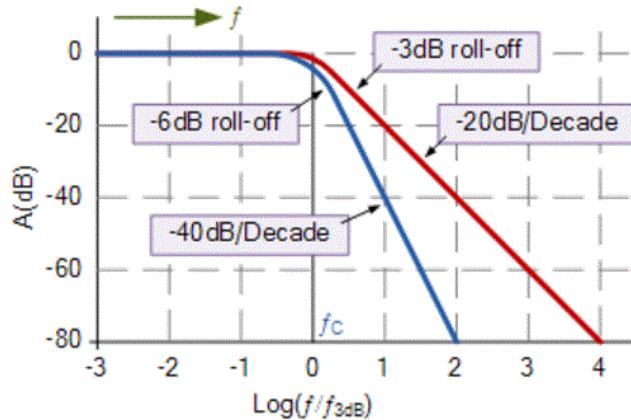


Fig. 14 - Normalized frequency response of low-pass filters [18].

Blue line - first order filter, red line - second-order filter.

In general, the frequency response of the second order filter is the same as that for a first-order filter. The difference is the steepness of the roll-off which is -40 dB/decade in the stop band, in comparison to the -20 dB/decade for the first order filter. However, a filter can exhibit a variety of responses depending on many circuits' parameters such as dumping factor [19].

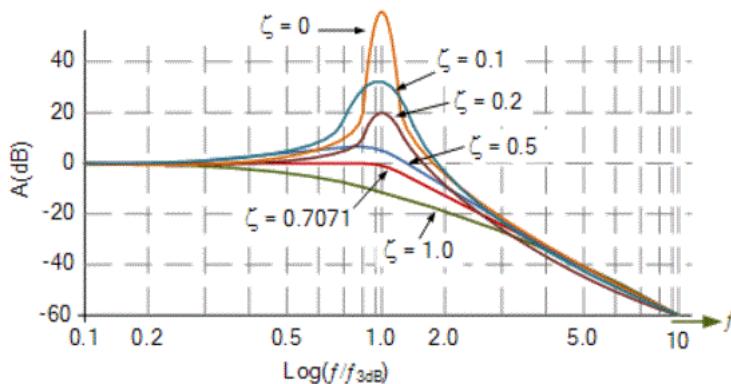


Fig. 15 - Normalized frequency response of second order low pass filters for different values of damping factor [18].

2.3.2. Stability

In order to determine whether the filter is stable, one may use bode plots – finding the gain and phase margins, measures of relative stability.

Phase margin is the difference between -180° and the actual phase angle of the frequency response function, measured at the frequency where the magnitude of the frequency response function is equal to one (0 dB).

Gain margin is the amount of gain that one can add to move the 0 dB crossing to occur at the same frequency at the -180° crossing [20].

3. Solar panel

The solar panel used in the project is an already present designed panel, which required repairs during the course of this project. It consists of 18 (3x6) photovoltaic cells that were provided by the faculty. Bypass diodes seen at the bottom of the figure 17 provide a path for photoelectric current in case the cells are not uniformly illuminated (due to shadows, for example). Thanks to diodes, additional experiments may be performed. However, the main purpose of the project is to enable to research phenomena rather than conduct the experiments themselves.

3.1. Repair

Some of the photovoltaic cells were crushed, that is why the panel has to be repaired. In order to do that, following steps were conducted:

- 1) Extraction of crushed cells.
- 2) Removal of the copper rest with air ejector and tinned copper.
- 3) Usage of dissolver in order to remove the glue residue.
- 4) Spread solder flux over the pad+ area.
- 5) Placement of thin layer of copper on the pad+ area.
- 6) Positioning the cell.
- 7) Stabilization of the cell to minimize movement.
- 8) Application of extreme heat (350°C) for 10 seconds.
- 9) Connection of the pad- with the path on the bottom of the cell using a silver-plated copper solder and a soldering iron.

3.2. Characteristics

A measurement of the IV curve for two different light intensity was performed, using the DC electronic load, Chroma 63103A. Before the measurement, the solar panel was heated by the

lamps for around 4 minutes, until the temperature reached the point when measured voltage was stabilized.

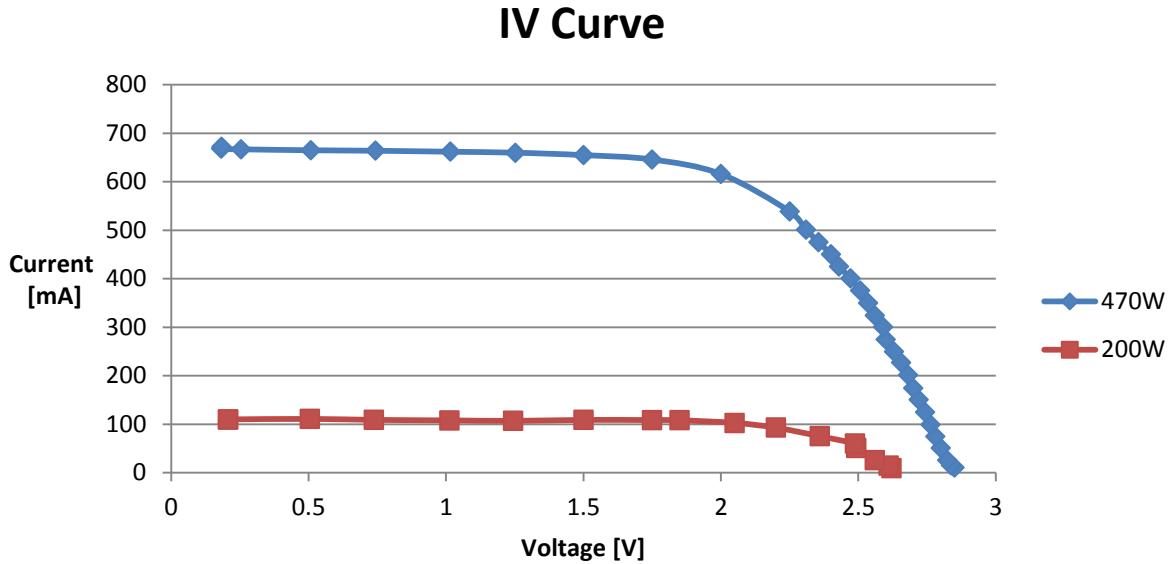


Fig. 16 - IV Curve of the PV.

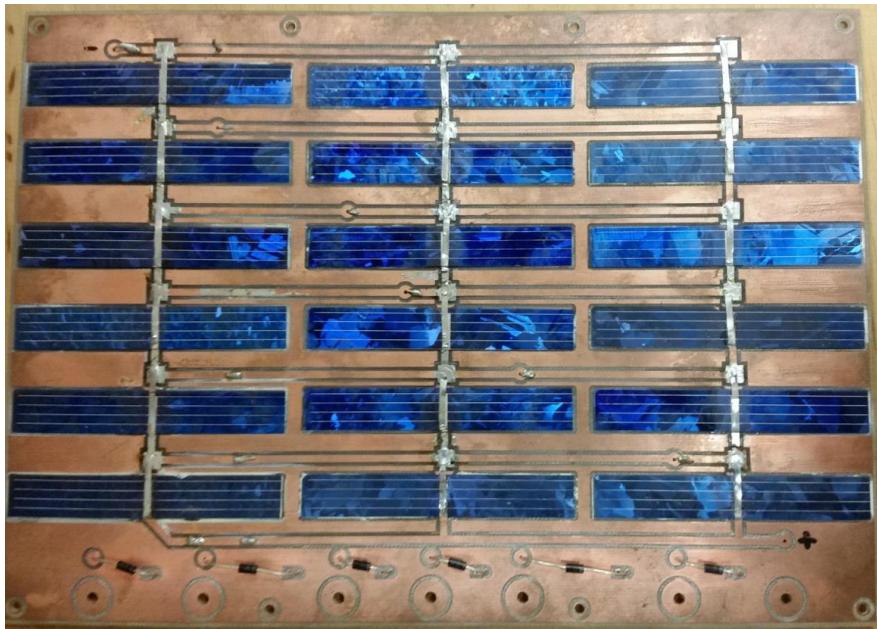


Fig. 17 - Photovoltaic module.

The module was illuminated with artificial light in order to perform experiments independently of weather conditions. An array of twelve 50-watt, 230-volt halogen lamps have been used because their light spectrum is relatively similar to the sun light spectrum. The lamps distribute fairly uniform irradiation across the surface, enabling illumination of PV modules with rectangular dimensions up to 35 cm × 30 cm. Light can be applied constantly or

in short pulses, preventing the module from being heated. The halogen lamps are cooled by a fan [21].



Fig. 18 - Photovoltaic module illuminated by the lamps.

4. General system architecture

Figure 19 presents the overall scheme of the whole system. The main part of the project is the DC-DC converter that, acts as a maximum power point tracker (MPPT) together with constantly calculated PWM control signal. The photovoltaic module acts as a varying voltage source that can output varying current, according to its IV curve. In this scenario, the DC-DC converter changes the lower voltage (from the PV) into higher voltage, acting as virtual varying load that can adjust automatically to the conditions of the PV (temperature/light etc.) The control signal PWM is constantly calculated out of a few measured voltages that represent input current, input voltage, output current, output voltage and current of the source of transistor. Measured signals are filtered in the block presented as analog filters and converted into digital values by the microcontroller. Not all of the measurements are needed for the MPPT algorithm that calculates the PWM control signal. However, all of them, together with the current duty cycle value, are coded and sent at first to the external memory. Once the external memory is full, the coded measurements are automatically sent to the PC and decoded in order to facilitate the analysis.

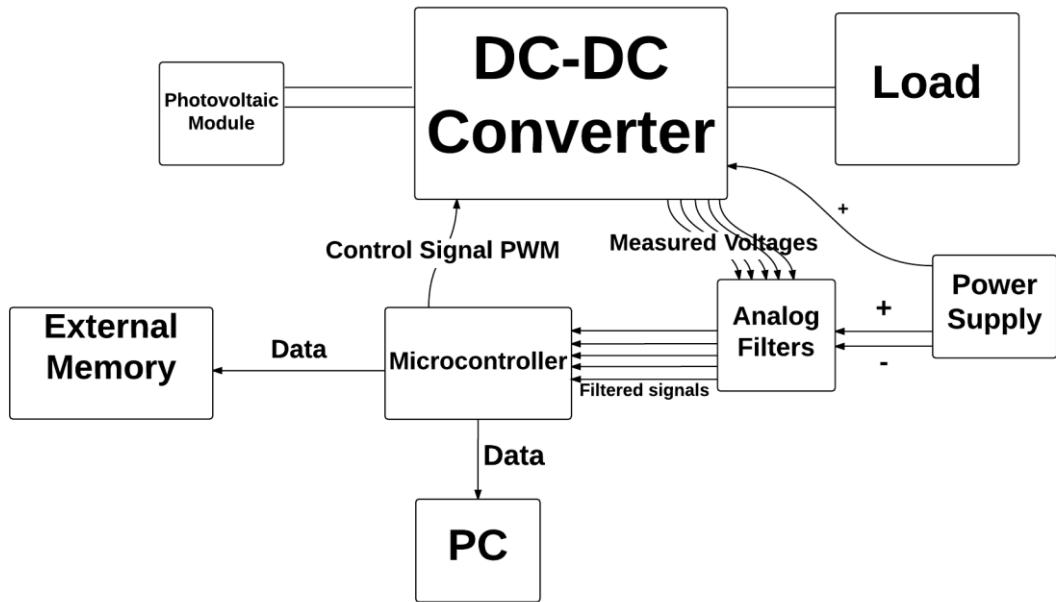


Fig. 19 - General block diagram.

The DC-DC converter was designed and constructed in the previous project, therefore the choice of the switching frequency, and electronic elements were out of the scope of this project. The aim for this project was redesigning the existing converter, taking into account any necessary changes, as well as optimizing it.

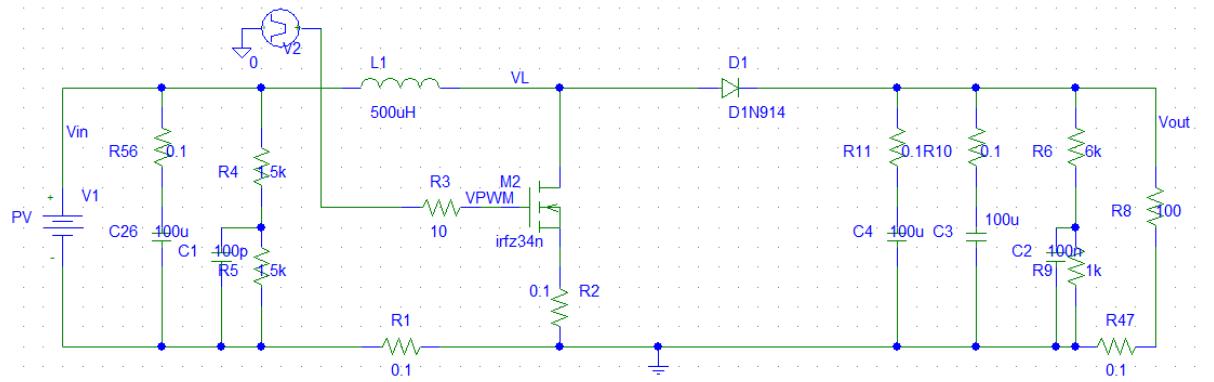


Fig. 20 - DC-DC converter, electrical scheme.

Previously chosen characteristics and electronic elements are listed below

- Switching frequency - 100 kHz
- Transistor - IRFZ34N
- MOSFET Drivers - TC4420

- Rectifying diode - 1N5820
- Inductor - 500 μH
- Input/output capacitors - 100 μF
- Shunt resistors - 0.16 Ω

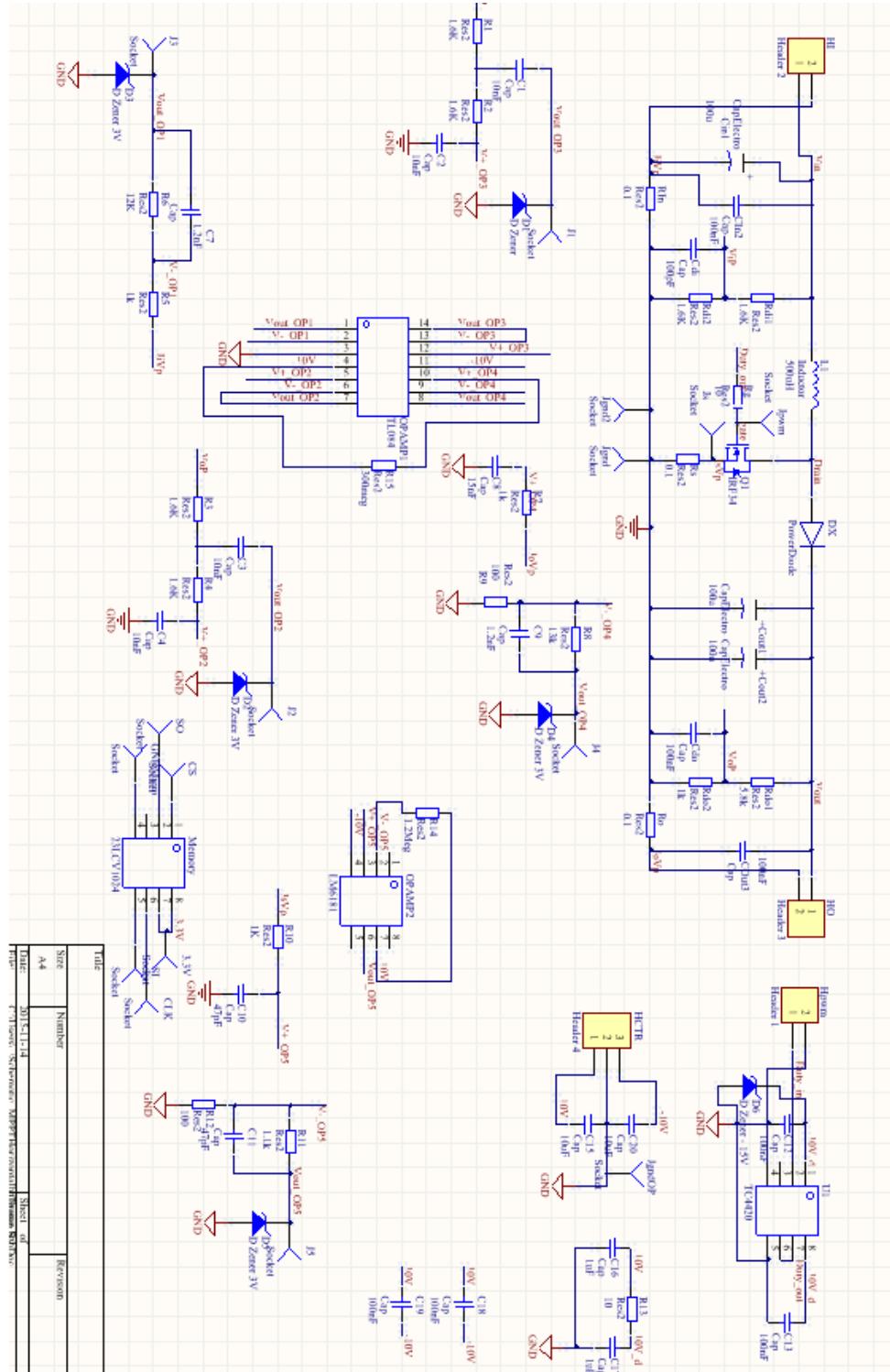


Fig. 21 - Electrical scheme.

4.1. Design of the printed circuit board (PCB)

The PCB was entirely redesigned, as many new elements were added. Excluding the inductor (upper left corner) and external memory plane (upper right corner), the PCB is divided into two major blocks: the power plane and the signal plane. The power plane, placed in the center of the PCB, is for the DC-DC converter. The electrical current flowing on this plane is relatively large (up to ~ 2.5 A). The remaining portion of the PCB consists of the signal plane. The principal difference between the signal plane and the power plane is the pouring option (discussed below).

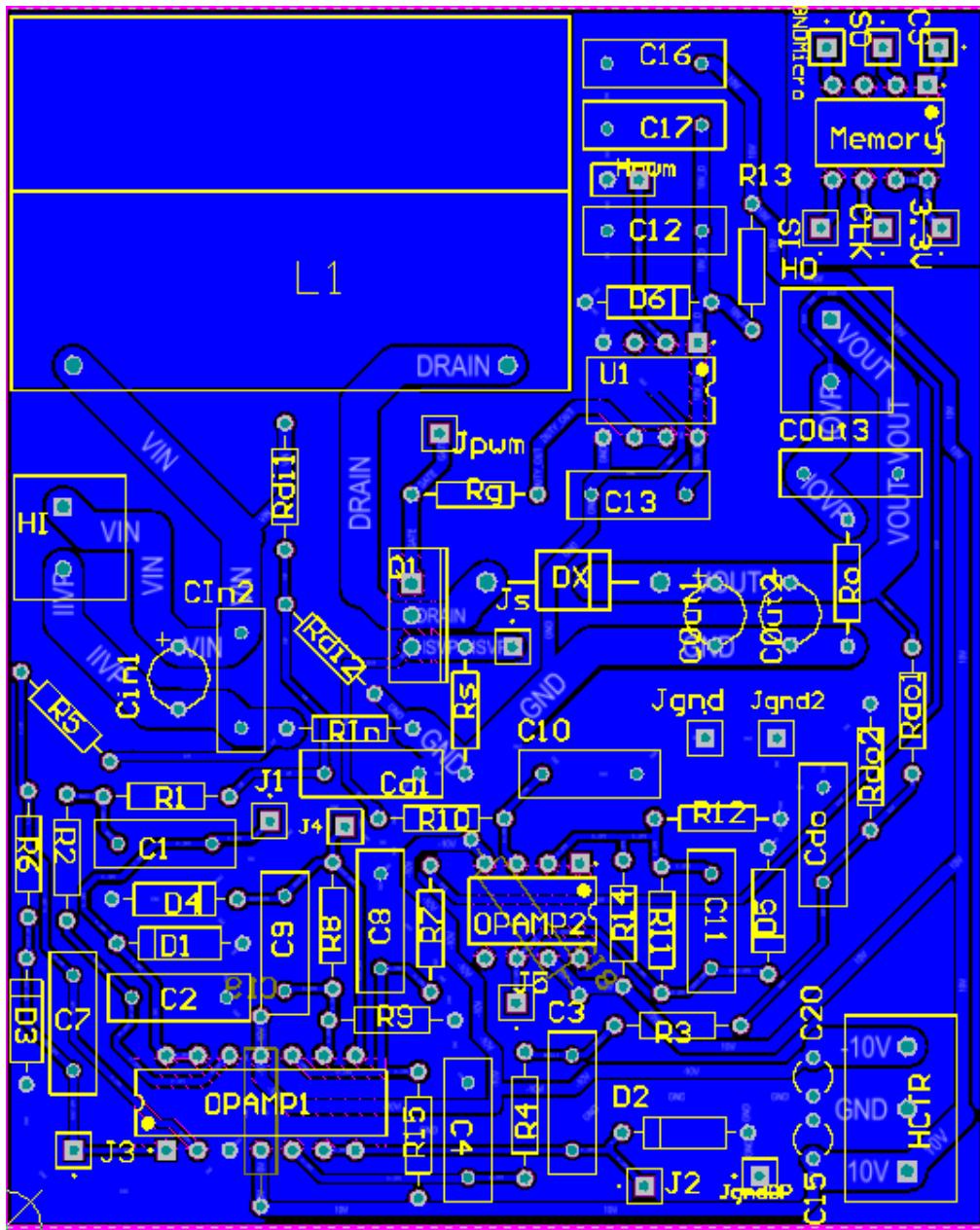


Fig. 22 - PCB topology.

Ideally, both power plane and measurement paths would be as short as possible. However, it was necessary to prioritize. The path connecting the inductor did not have to be short, nor did the paths for the input and output, given that these will be connected by cables. Electric current is measured by the voltage drop across the resistors. In order to diminish the power loss, the resistors were selected to be as small as possible, though this also increases vulnerability to noise. Due to this vulnerability, it was necessary to focus on short current paths first and foremost, particularly for the current source of the transistor. Because, the opamps for the V_{in} , V_{out} , I_{in} , I_{out} , are gathered in one chip, it was impossible to design short path for every single input. V_{in} and I_{in} were prioritized over V_{out} and I_{out} , because of space availability. The PCB was designed to be as small as reasonably possible while avoiding the need for excessively difficult soldering.

Following path width were chosen: power plane: 3 mm; signal plane: 1 mm. A clearance of at least 0.3 mm is adequate for this particular application. According to [22] 0.3 mm clearance is enough for $V_{pk} = 500$ V.

Additional changes

1. Adding Zener diode on the output of PWM to protect the pins of the microcontroller.

2. Dividing polygons into 4 types:

- SignalPlane (Pour over all same net object option);
- PowerPlane (Pour over all same net polygons only option);
- ExtMemPlane (Pour over all same net object option);
- InductorPlane (Pour over all same net polygons only option).

The aim was to isolate the signal plane from the power plane in order to diminish noises. It is crucial for the measurement system.

3. Eliminating cross connection between the pads by filling the clearance.

4. Adding space for rectifying diode.

5. Increased the hole size for the terminal block.

6. Reduced shunt resistors to 0.1Ω , 1 % accuracy, to reduce power loss.

7. Relocated shunt resistor for I_{out} measurement (detailed in the Measurement section).

Disadvantages of the design

- Long I_{source} path (measurement) due to space restrictions (particularly regarding the C_{di} capacitor).

- Long power path connected to R_s resistor in order to maintain short distances to output capacitors C_{out1} and C_{out2} .
- I_{out} and V_{out} measurement paths are very long due to the topology of the analog filters. If only one integrated circuit is chosen for 4 filters, then at least 2 paths would have to be further away.

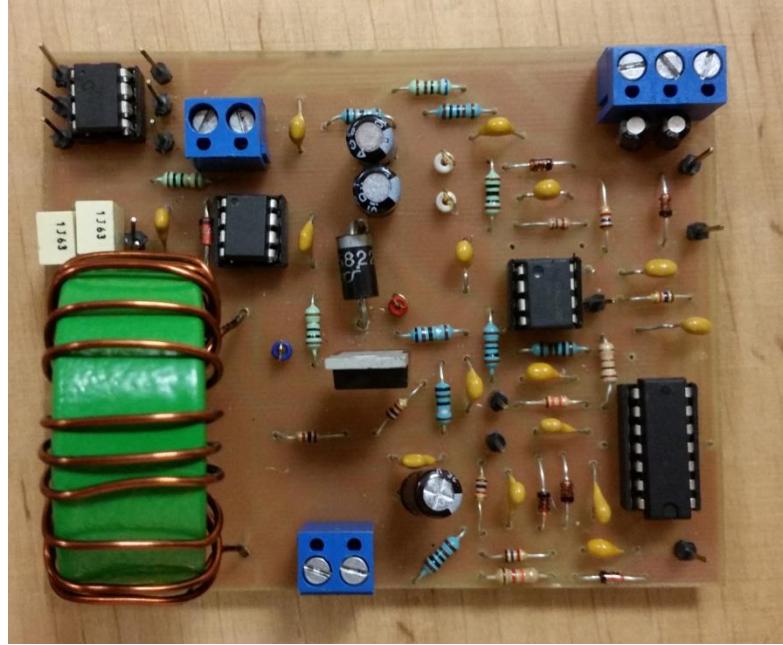


Fig. 23 - PCB after soldering.

4.2. DC-DC simulations

The DC-DC converter was thoroughly tested, for use with analog filters, through repeated simulations (transient analysis). This increased the probability that the filters would function according to the intended design and allowed for the identification of an error of the cut-off frequency of one of the filters, which was adjusted accordingly.

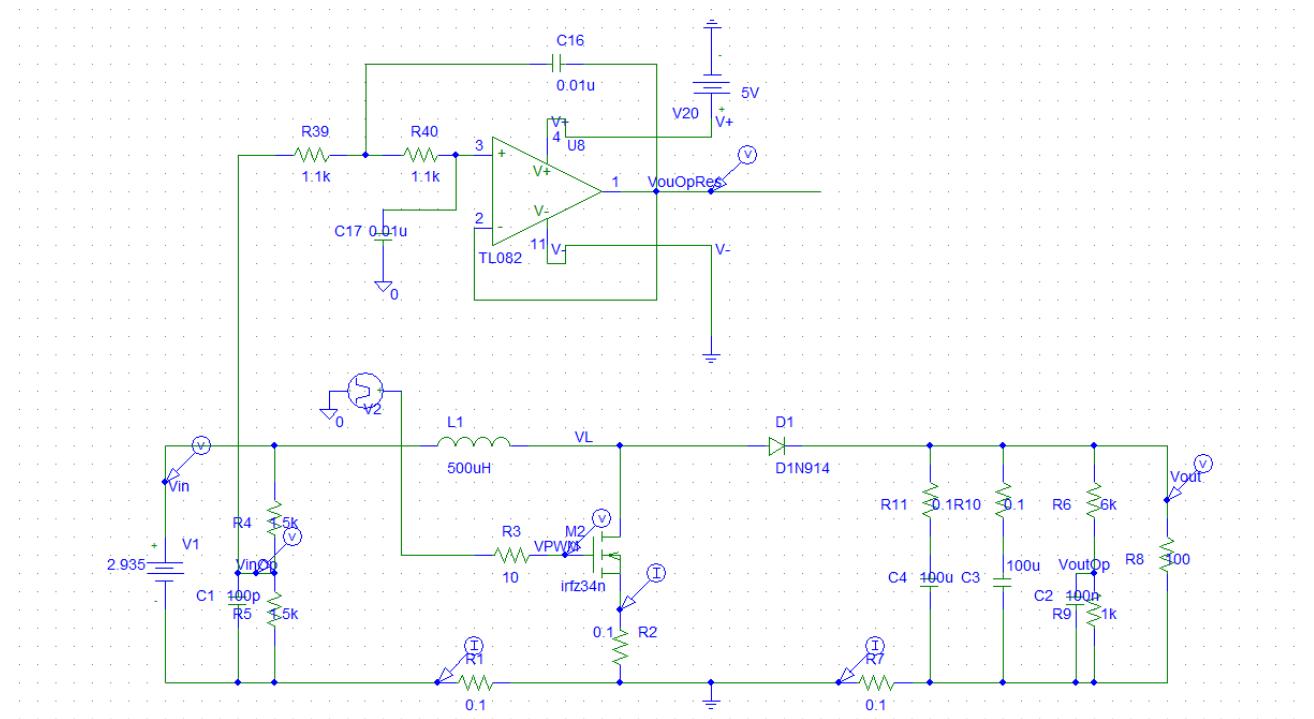


Fig. 24 - Simulation example of V_{in} filter, electrical scheme.

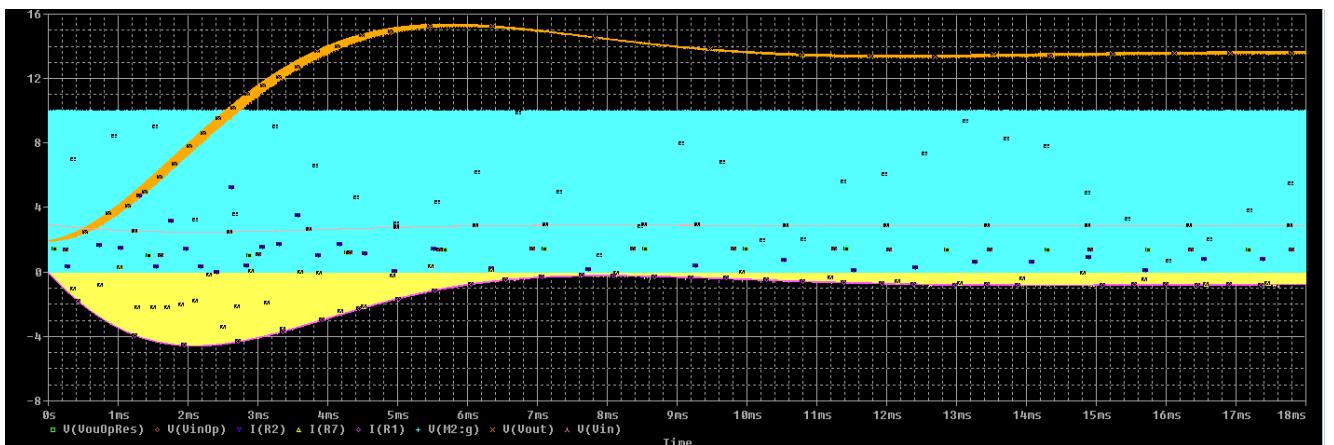


Fig. 25 - Simulation example of V_{in} filter, $V(M2:g)$ - PWM.

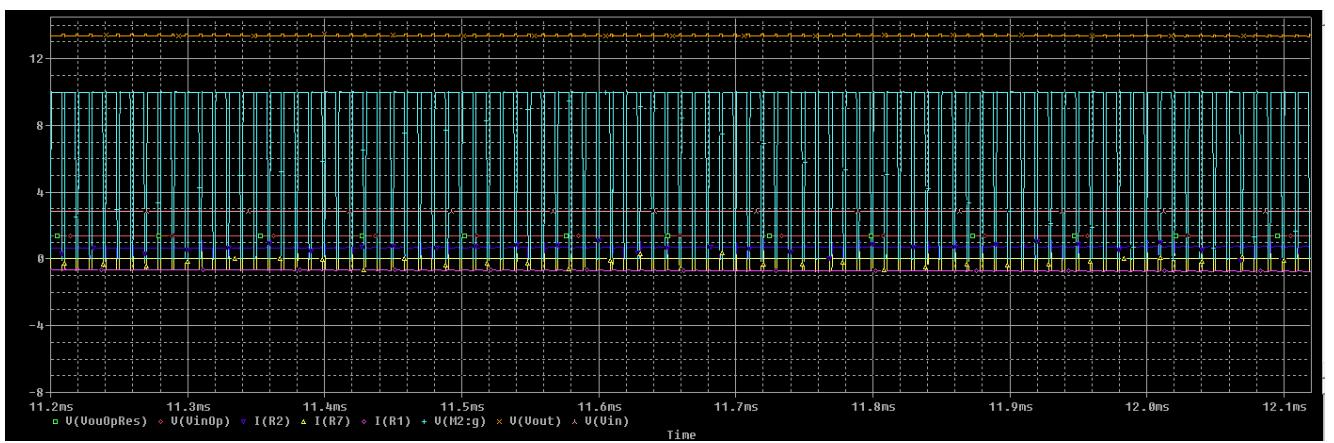


Fig. 26 - Simulation example of V_{in} filter, zoom.

Unfortunately, every single simulation of DC-DC converter had to be conducted separately, because of the limited number of parts in the student version of PSpice. Consequently, the DC-DC part remained the same, and the measurement parts were added for each input.

4.3. Power supply

The system is powered from two different sources. Several modules need power supply.

Module	Part	Voltage [V]	Source	Description
DC-DC converter	MOSFET driver	10	Power supply	MOSFET driver is needed for the separation of the DC-DC converter from the power supply (previously designed)
Analog filters	opamps	10/-10	Power supply	Originally planned for single supply only, but redesigned later on (discussed in the section 10.5. Single voltage)
Microcontroller	-	3.3	PC	Connected together with the UART transmission, USB connection

Table 1 - Power supply description.

4.4. Microcontroller

Microcontroller is the core of the project. It carries out various functions:

- Converting the analog measurement into digital values.
- Digital data processing.
- Processing the MPPT algorithm.
- PWM generation.
- Communicating with external memory and PC.

The microcontroller used for this project was dsPIC33JF16GS502 together with 16-bit 28-pin Starter. The reasons for choosing this specific microcontroller were that:

- 1) it was available in laboratory;
- 2) it was equipped with:

- High-speed PWM module;
- ADC, more than 5 channels;

- SPI or IC2 module;
- UART communication;
- The programming language is C, which I was already acquainted with.

3) development board was available;

4) the programmer was available.

4.4.1. Development board

The first part of the project was becoming familiar with the software environment and writing simple programs, such as a program that blinks the diode with a given frequency. The next stage was to develop the program to control each of the additional modules of the future project, such as: ADC, PWM, and UART etc. Most of the information about the functioning of the modules was provided by the microcontroller producer (Microchip), which, in combination with the specifications, made the programming much easier.

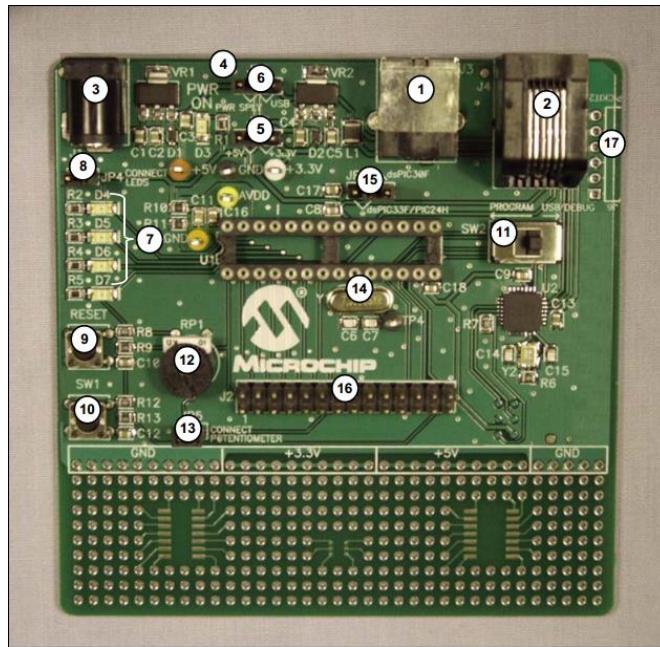


Fig. 27 - 16-bit 28-pin starter development board [23].

No.	Name	Description
1	J3	USB Port
2	J4	MPLAB® ICD 2 Connector
3	J1	Power Supply Connector
4	D3	Power-on Indicator
5	JP2	+5V or +3.3V Jumper
6	JP1	Power Supply or USB Jumper
7	D4-D7	LED Indicators
8	JP4	LED Connect Jumper
9	RESET	Reset Button
10	SW1	Switch 1
11	SW2	Switch 2
12	RP1	Potentiometer
13	JP5	Potentiometer Connect Jumper
14	Y1	Oscillator
15	JP3	Device Selection Jumper
16	J2	I/O Header
17	J6	PICkit™ 2 Connector

Fig. 28 - 16-bit 28-pin starter development board hardware features [23].

4.4.2. dsPIC33JF16GS502 specifications

- Up to 40 MIPS operation at 3.0 - 3.6 V. (used voltage +3.3 V)
- Internal fast RC (FRC) oscillator at a frequency of 7.37 MHz
- Phase-locked loop (PLL) with 120 MHz VCO
- Output pins can drive voltage from 3.0 V to 3.6 V
- 16 mA Source/Sink on all PWM pins.
- 5 V tolerant digital input pins (except RB5)
- Flash program memory (16 Kbytes)
- Data SRAM (2 Kbytes)
- PWM frequency resolution of 1.04 ns
- SPDIP [2]

5. Measurement system

5.1. Design

The measurement was one of most important parts of the project. The purposes for conducting measurements were noise removal and an adjustment of the voltage output to the ADC input (0-3.3 V).

Gain

The goal was to provide the voltage output that will be smaller than the maximum ADC pin input voltage, which is equal to 3.3 V. A small margin was taken into account (about 0.3 V). $R_{divider}$ represents the proportion between the resistances (for voltage measurement), and the

multiplier of the voltage across the resistor that diminishes respective current flowing through it for the current measurement. Expected output should be always slightly smaller than 3.3 V, with an exception of the analog filter output of the V_{in} measurement, because this output will not change significantly throughout the entire operation. For that reason, the output of the V_{in} measurement was set to the half of the range that ADC pin can accept.

Measured voltage			Resistance manipulation			Expected output		
Filter	Min [V]	Max [V]	$R_{divider}$	Min [V]	Max [V]	Proposed Gain	Min [V]	Max [V]
V_{in}	2.65	3.02	1/2	1.325	1.508	1	1.325	1.508
V_{out}	3.16	19.33	1/6.8	0.452	2.761	1	0.452	2.761
I_{in}	0.05	2.54	0.1	0.005	0.254	12	0.054	3.048
I_{out}	0.04	0.24	0.1	0.004	0.024	130	0.481	3.081
I_{source}	0.05	2.54	0.1	0.005	0.254	12	0.054	3.048

Table 2 - Gain calculation.

Measured voltage was taken from [21].

Cut-off frequency

All filters are low-pass, and they pass the signal up to the desired frequency (cut-off frequency). This allows for the attenuation of noise present in all of the frequencies above. For all of the filters, cut-off frequency was set to be 10 times smaller than the switching frequency, except from the filtering of the current of the source of transistor. For I_{source} , the cut-off frequency was set to be greater, because, unlike the other filters, in which the average was needed, the I_{source} filter required the switching waveform. This specific cut-off frequency was chosen based on the transient simulation of the DC-DC converter.

Filter	Switching Frequency	Proposed cut-off frequency	Finally set	Simulation result
V_{in}	100 kHz	10 kHz	10 kHz	10 kHz
V_{out}	100 kHz	10 kHz	10 kHz	10 kHz
I_{in}	100 kHz	10 kHz	10 kHz	10.9 kHz
I_{out}	100 kHz	10 kHz	10 kHz	6 kHz
I_{source}	100 kHz	1 MHz	3 MHz	3 MHz

Table 3 - Cut-off frequency calculation.

Simulations

In order to record all the necessary data, one has to be sure that the measurements are taken correctly. In the previous project, the measurement system was present, but it was poorly developed, and not calibrated for connection to the ADC module. All the filters were designed, simulated, and implemented. AC and DC simulations were performed for each filter. However, as the results were very similar from filter to filter, only one representative AC and DC set of simulations is shown below. For the rest of the filters, only scheme, equations and calculations will be present. For the purpose of this, for the current simulations, voltage source was substituted by the current source.

5.2. Voltage input and output voltage filters

Sallen-Key topology was chosen because it is a second-order active filter that is very simple to construct. The chip TL084, was not changed because it fulfills all the needed requirements.

Chip - TL084

- Supply voltage= $\pm 18 V$
- Input voltage (2) = $\pm 15 V$
- Unity-gain bandwidth = $3 MHz$
- 4 x opamps in one chip/integrated circuit
- DIP [25]

Note: For simulation, TL082 is used because it is the model used for 5 terminals opamp of TL084.

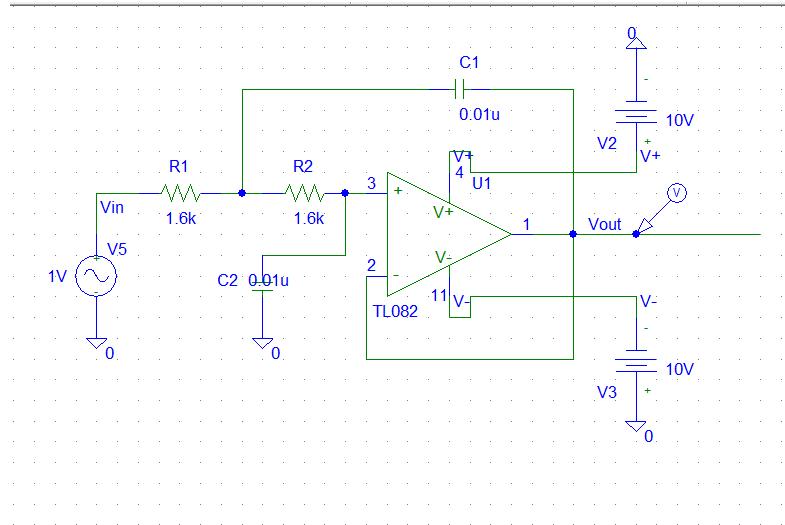


Fig. 29 - V_{in} filter, electrical scheme.

$$F_c = \frac{1}{2\pi\sqrt{R_1C_1R_2C_2}} \quad (1)$$

Assuming that $R_1=R_2$ and $C_1=C_2$

$$F_c = \frac{1}{2\pi RC} \quad (2)$$

Gain = 1 (for 0 DC frequency) (3)

*Note: To a limited extent, the gain may be regulated for a circuit with an additional resistor.
(Further discussed in section 10.4. Design of the current filters)*

Calculations

Choosing $C = 0.01 \mu F$, the R was calculated.

$$R = \frac{1}{2\pi F_c C} = 1591 \Omega, \text{ design series} = 1.6 k\Omega \quad (4)$$

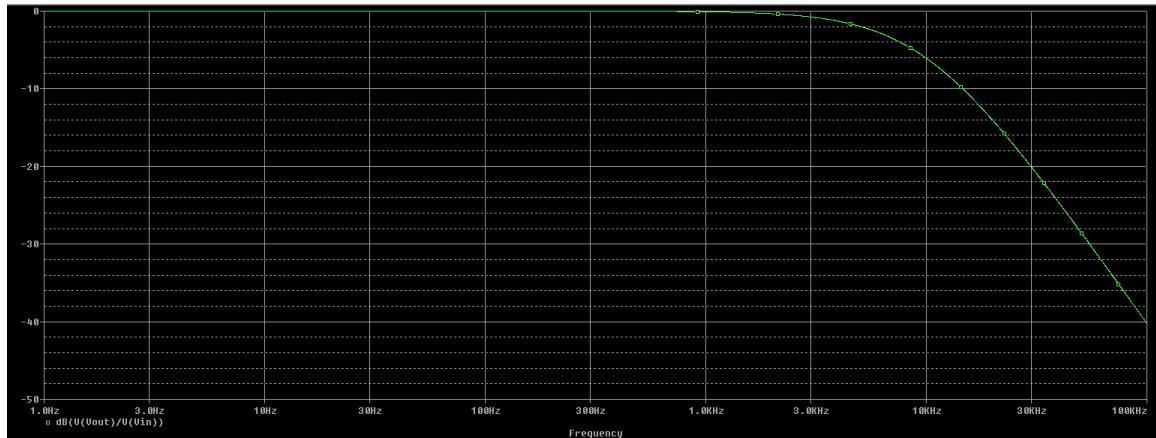


Fig. 30 - V_{in} filter, AC simulation.

AC simulation gave expected result, in accordance to the theoretical assumptions. Cut-off frequency is presented in table 2.

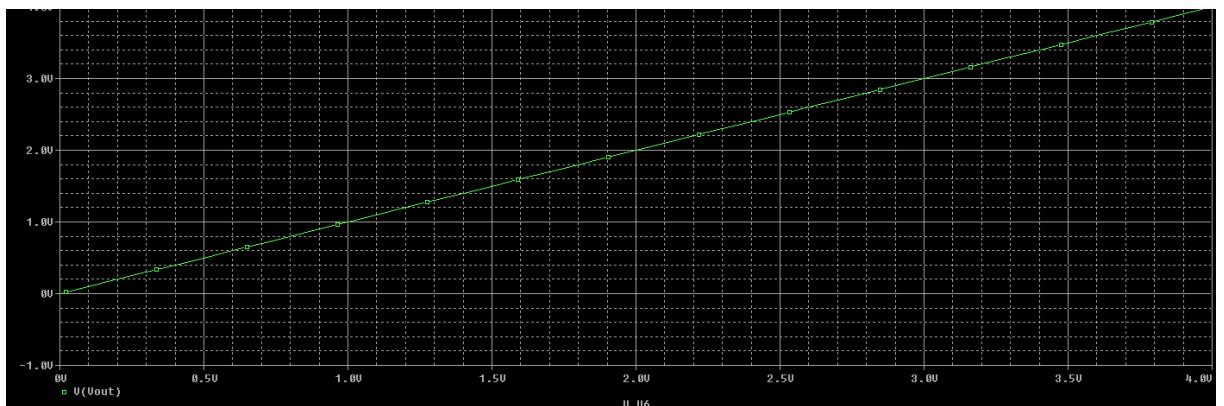


Fig. 31 - V_{in} filter, DC simulation.

DC simulation gave expected result, in accordance with theoretical assumptions. The characteristics are linear, and the derivative is constant. The voltage offset is negligible.

5.3. Current input filter

First order, inverting topology was chosen. The TL084 chip was not changed because it fulfills all the requirements.

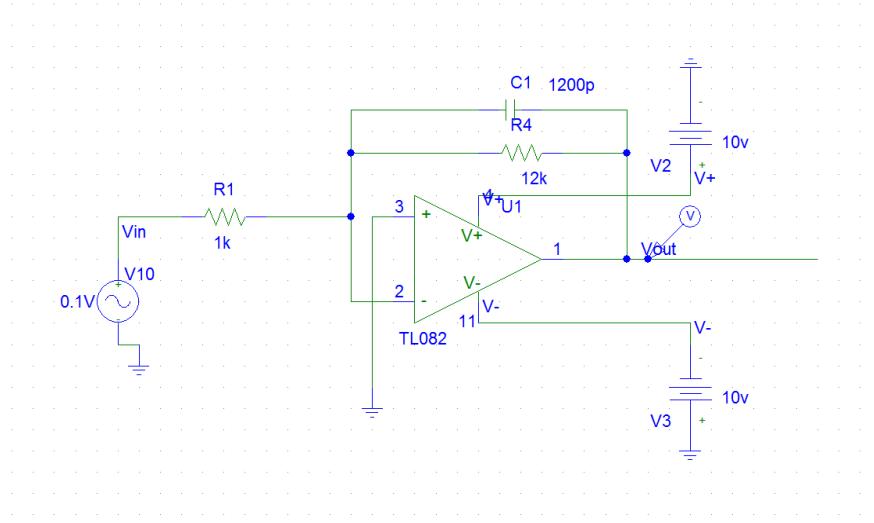


Fig. 32 - I_{in} filter, electrical scheme.

$$F_c = \frac{1}{2\pi RC} \quad (5)$$

$$G = \frac{R_2}{R_1} \quad (\text{For DC frequency}) \quad (6)$$

Calculations

Choosing $R_1=1 k\Omega$, the R_2 was calculated.

$$R_2 = R_1 G = 12 k\Omega \quad (7)$$

$$C = \frac{1}{2\pi F_c R_2} = 1.33 nF, \text{ design series} = 1.2 nF \quad (8)$$

5.4. Current output filter

First order, noninverting topology was chosen. Due to the fact that the gain cannot be smaller than 1 for this topology, an additional RC filter was implemented. The TL084 chip/IC, was not changed because it fulfills all the requirements.

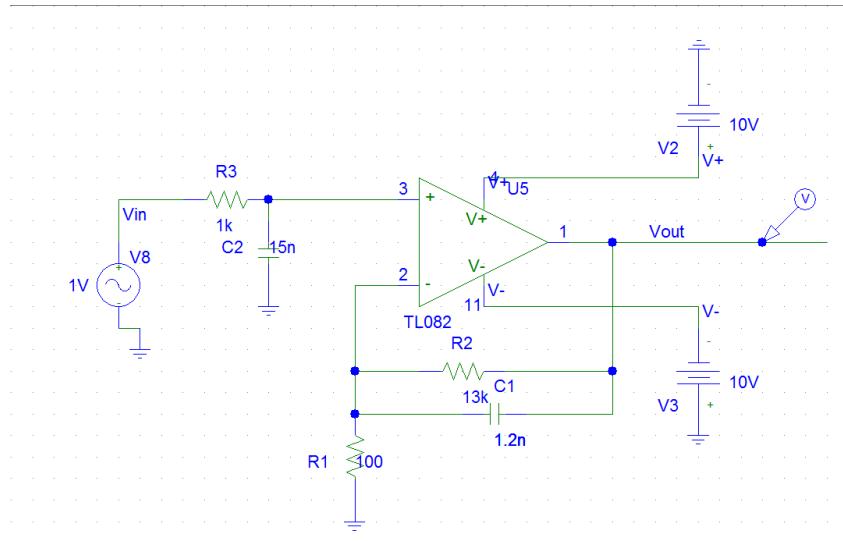


Fig. 33 - I_{out} filter, electrical scheme.

Noninverting filter

$$F_c = \frac{1}{2\pi R_2 C} \quad (9)$$

$$G = 1 + \frac{R_2}{R_1} \quad (\text{for DC frequency}) \quad (10)$$

Calculations

Choosing $R_1 = 100 \Omega$, the R_2 was calculated.

$$R_2 = R_1(G - 1) = 12.9 k\Omega, \text{ design series} = 13 k\Omega \quad (11)$$

$$C_1 = \frac{1}{2\pi F_c R_2} = 1.29 nF, \text{ design series} = 1.2 nF \quad (12)$$

RC filter calculations

Choosing $R_3 = 100 \Omega$, the C_2 was calculated.

$$C_2 = \frac{1}{2\pi F_c R_3} = 15.9 nF, \text{ design series} = 15 nF \quad (12)$$

5.5. Current of the source of the transistor filter

First order, noninverting topology was chosen. Due to the fact that the gain cannot be smaller than 1 for this topology, an additional RC filter was implemented. The LM171 chip, was used.

LM171

- Supply voltage = $\pm 15 V$
- Unity-gain bandwidth = $100 MHz$
- DIP

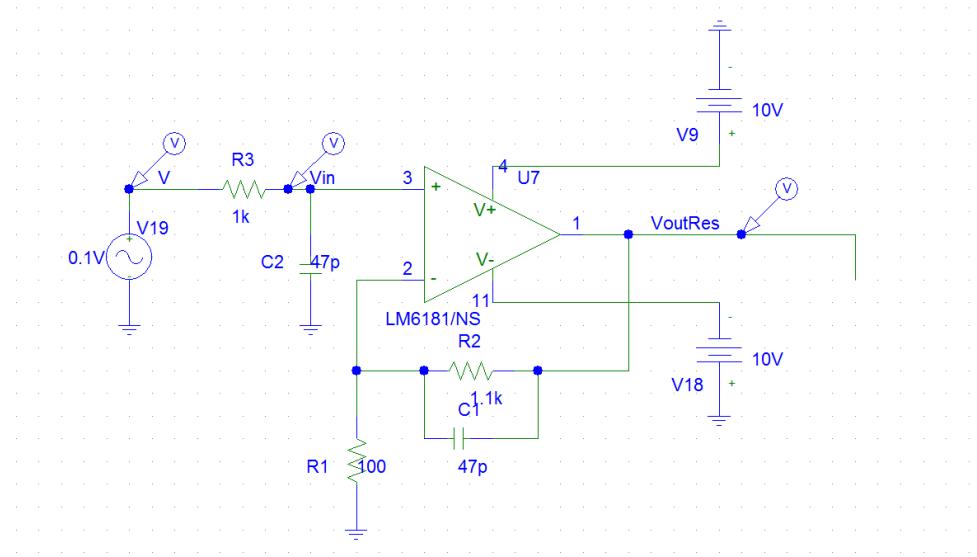


Fig. 34 - I_{source} filter, electrical scheme.

Noninverting filter

$$F_c = \frac{1}{2\pi R_2 C_2} \quad (13)$$

$$G = 1 + \frac{R_2}{R_1} \quad (\text{for DC frequency}) \quad (14)$$

Choosing $R_1=100 \Omega$, the R_2 was calculated.

$$R_2 = R_1(G - 1) = 1.1 k\Omega, \text{ design series} = 1.1 k\Omega \quad (15)$$

This time the element values were chosen experimentally using DC-DC converter simulation, both for the opamp topology and the RC filter. When increasing the C and R, the cut-off frequency will decrease.

$$C_1=47 \text{ pF}$$

RC filter

$$C_2=47 \text{ pF}$$

$$R_3=1 \text{ k}\Omega$$

Filter	Gain	Cut-off frequency	Gain-bandwidth product	Unity gain-bandwidth product	Topology	Inverting /Noninverting
V_{in}	1	10 kHz	10 kHz	3 MHz	Sallen-key	Noninverting
I_{in}	12	10 kHz	120 kHz	3 MHz	First order	Inverting
V_{out}	1	10.9 kHz	10 kHz	3 MHz	Sallen-key	Noninverting
I_{out}	130	6 kHz	1.3 MHz	3 MHz	First order	Noninverting
I_{source}	12	3 MHz	36 MHz	100 MHz	First order + RC	Noninverting

Table 4 – Summary of filters specifications.

Unity gain-bandwidth product is a very important parameter of the opamps. Gain-bandwidth product of the design filters should always be smaller than this parameter. This requirement was taken into account while choosing each opamp.

DC simulations for I_{out} and I_{source} did not yield an entirely satisfactory result. The characteristics are linear, and the derivative is constant, but there was a voltage offset present. For that reason, additional resistance was added between noninverting input of the opamp and the positive voltage of the power supply. Finally, the resistor was not added to the circuit because the results turned out to be satisfactory without it.

5.6. Additional changes

1. Additional investigation for the placement of shunt resistors was conducted.

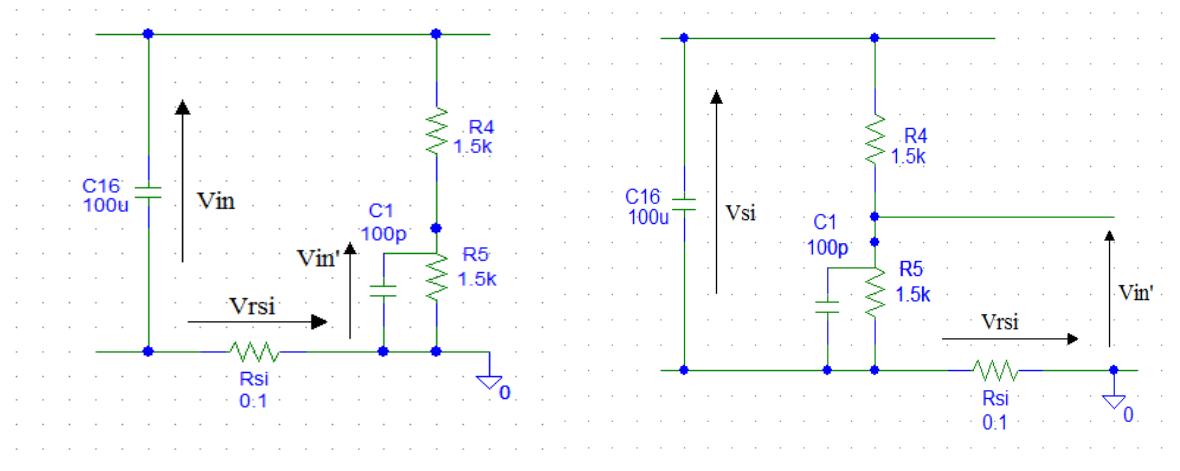


Fig. 35 - Topology of the R_{si} placement 1.
(C_1 and R_5 directly connected the ground)

Fig. 36 - Topology of the R_{si} placement 2.
(C_1 and R_5 separated from the ground with R_{si})

Equation for the topology 1:

$$V_{in}' = (V_{in} - V_{rsi}) \frac{R_5}{R_4 + R_5} \quad (16)$$

Equation for the topology 2:

$$V_{in}' = (V_{in} \frac{R_5}{R_4 + R_5}) - V_{rsi} \quad (17)$$

From the point of the view of the I_{source} measurement, both topologies are equivalent, because the same current will flow through the R_{si} resistor. From the point of view of the V_{in} and V_{out} (The topology for V_{out} is analogical) measurement topology does matter because V_{in}' should be affected as little as it possible by the V_{rsi} factor. Topology 1 was selected for both V_{out} and V_{in} . In the previous project, placement of the resistor R_{si} was arbitrary (both of topologies were used). After the investigation, topology for V_{out} measurement was changed.

2. The shunt resistors were changed from 0.16Ω to 0.1Ω with 1 % of accuracy in order to minimize power losses.

6. Microcontroller role

The core component for controlling the process of MPPT. When triggered by appropriate hardware, ADC converts the filtered voltage into the digital values, converts all analog data into digital, processes it, records it, and sends it to both external memory and to the PC. The control signal PWM is produced by the implemented algorithm. After the measurement is done, the microcontroller also sends data to the PC via UART.

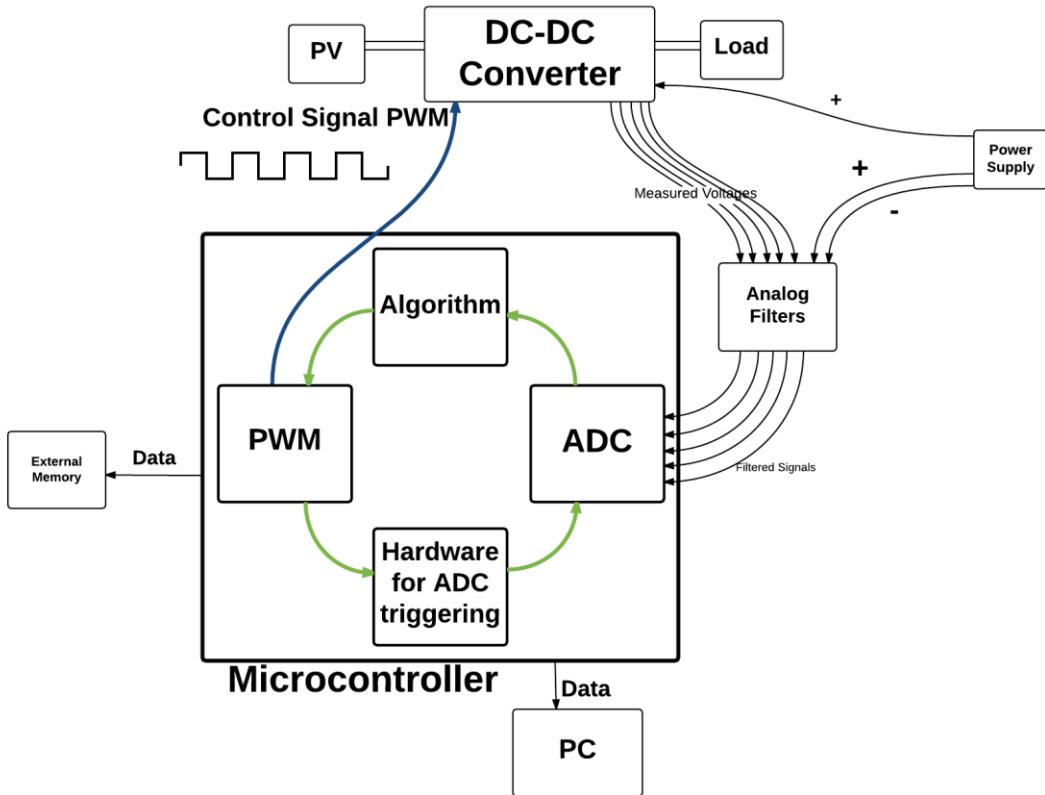


Fig. 37 - Microcontroller general diagram.

6.1. Pulse width modulation (PWM)

6.1.1. Clock provided for PWM

Setting up the auxiliary PLL for the PWM is needed, because the resolution of the PWM duty cycle is dependent on the clock provided for PWM. The higher the clock frequency, the higher resolution of duty cycle. This is particularly important for high PWM frequencies.

$$ACLK = (REFCLK * M)/N$$

where,

$REFCLK$ = Internal FRC clock frequency (7.37 MHz) if the Internal FRC is selected as clock source

$REFCLK$ = Primary Oscillator Clock frequency (POSCCLK) if the primary oscillator is selected as clock source

M = 16 if the auxiliary PLL is enabled by setting the ENAPLL (ACLKCON<15>) bit

M = 1 if the auxiliary PLL is disabled

N = Postscaler ratio selected by the Auxiliary Postscaler (APSTSCLR<2:0>) bits in the Auxiliary Clock Control (ACLKCON<2:0>) register.

Fig. 38 - Clock frequency provided for PWM module calculations [24].

$$\text{Frequency} = \frac{\text{FRC} \cdot 16}{\text{APSTSCLR}} = \frac{7.37 \text{ MHz} \cdot 16}{1} = 117.9 \text{ MHz} \quad (18)$$

Voltage controlled oscillator (VCO) output frequency must meet the following requirements:

- The PFD input frequency must be in the range of 0.8-8.0 *MHz*.
- The VCO output frequency must be in the range of 100-200 *MHz* [24].

```

ACLKCONbits.FRCSEL = 1;           // FRC provides input for Auxiliary PLL (x16)
ACLKCONbits.SELACLK = 1;          // Auxiliary Oscillator provides clock source for PWM
ACLKCONbits.APSTSCLR = 7;         // Divide Auxiliary clock by 1
ACLKCONbits.ENAPLL = 1;           // Enable Auxiliary PLL

```

Fig. 39 - Part of the function initiating PWM generation.

6.1.2. Standard edge-aligned PWM

To create PWM with a given period and duty cycle two registers are used: one involves a timer that counts upward from zero to a specified value; the other contains the duty cycle value, which is constantly compared to the timer value. The PWM output signal is asserted when the duty cycle value is less than or equal to the timer value, and the signal is deasserted when the duty cycle value is higher than the timer value. The timer resets itself at the end of each period [24].

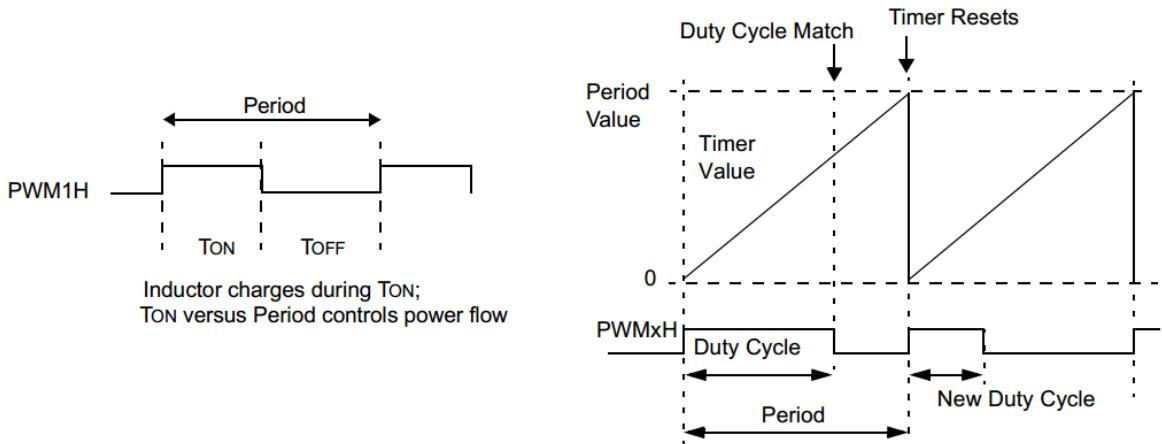


Fig. 40 - Standard edge-aligned PWM [24].

6.1.3. Time base

Master Time Period PTPER register defines the switching frequency of the PWM pulses. In order to set the PWM frequency to 100 kHz, PTPER register had to be configured.

$$\text{PTPER} = \frac{\text{REFCLK}}{7.37 \text{ MHz}} \frac{\text{Desired PWM period}}{1.04 \text{ ns} * \text{PWM Input Clock Prescaler}} = \frac{1}{1} \frac{10 \mu\text{s}}{1.04 \text{ ns} * 1} = 9615 \quad (19)$$

REFCLK = FRC oscillator

Desired PWM frequency = 100 *kHz*

PWM input clock prescaler = 1 (PTCON2bits.PCLKDIV)

```

PTCON2bits.PCLKDIV = 0; // Divide by 1, maximum PWM timing resolution
PTPER = 9615;
MDC = MDCSTART; // Duty cycle = 75 (part of PTPER register) Duty Cycle in that case
IOCON2bits.PENH = 1; // PWM1H is controlled by PWM module
IOCON2bits.PENL = 1; // PWM1L is controlled by PWM module
IOCON2bits.POLH = 0; // PWMxH pin is active-high
IOCON2bits.POLL = 0; // PWMxL pin is active-high
IOCON2bits.PMOD = 1; // PWM I/O pin pair is in the Complementary Output mode
IOCON2bits.FLTDAT = 0; // PWM1H and PWM1L are driven LOW on occurrence of Fault and Current limit
PWMCON2bits.FLTSTAT = 0; // cleared so no interrupt pending
PWMCON2bits.CLSTAT = 0; // cleared so no interrupt pending
PWMCON2bits.TRGSTAT = 0; // cleared so no interrupt pending
PWMCON2bits.FLTIEN = 0; // Fault Interrupt DISabled
PWMCON2bits.CLIEN = 0; // Current Limit Interrupt DISabled
PWMCON2bits.TRGIEN = 0; // Trigger event interrupts disabled
PWMCON2bits.ITB = 0; // PTPER register provides timing for PWM1 generator
PWMCON2bits.MDCS = 1; // MDC provides duty cycle information
// Center-Aligned mode is disable
PTCONbits.PTEN = 1; // Enable the PWM Module

```

Fig. 41 - Part of the function initiating PWM module.

6.2. Hardware used for triggering

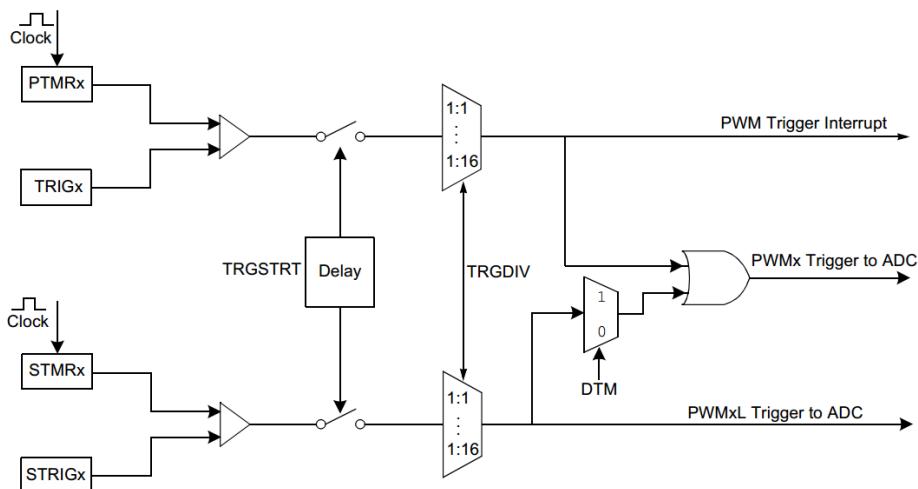


Fig. 42 - ADC Triggering [24].

The TRIG1 register sets the triggering point for the PWM output. The ADC trigger signal is generated every time that the Independent Time Base Counter register value is equal to the value of TRIG1 register. For that reason, it is possible to trigger the measurement time with

respect to the PWM period. The TRIG1 was eventually set to be equal 50. That is 1.92 ms after the start of PWM cycle. The purpose was to avoid triggering ADC at the same time as the change of PWM state, due to the presence of oscillations.

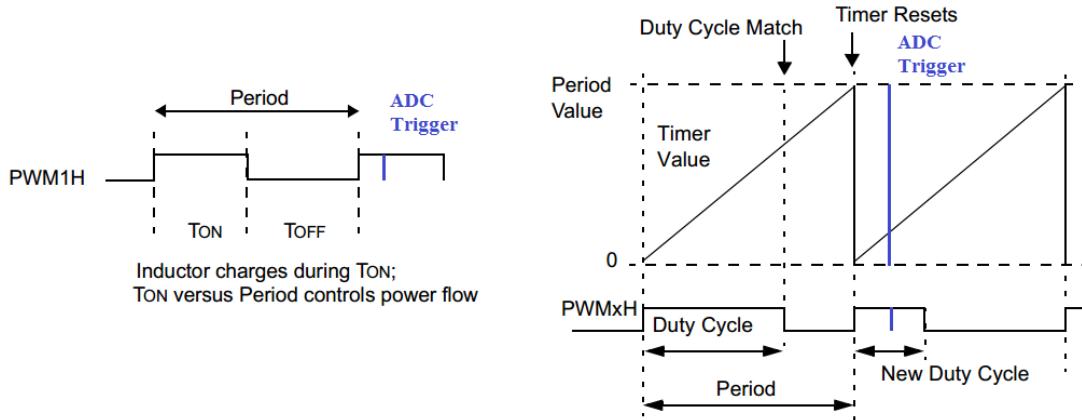


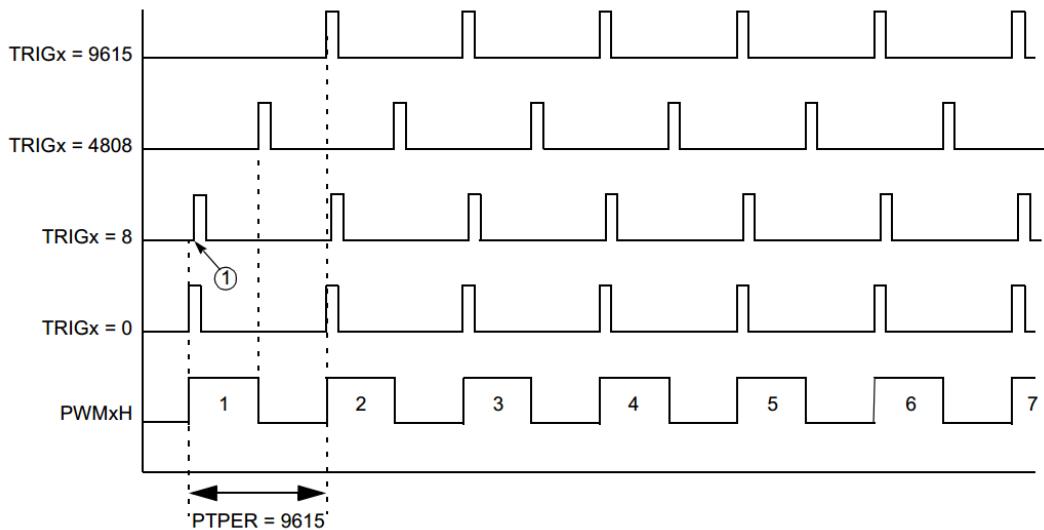
Fig. 43 - ADC Triggering [24].

```

ADCPC0bits.TRGSRC0= 0b00100;           //ADC Pair 0 triggered by PWM period match
ADCPC0bits.TRGSRC1= 0b00100;           //ADC Pair 1 triggered by PWM period match
ADCPC1bits.TRGSRC2 = 0b00100;          //ADC Pair 2 triggered by PWM period match
TRGCON1bits.DTM=0;                     // no dual trigger
TRGCON1bits.TRGDIV = 0x1111;           // Trigger generated every PWM cycle
TRGCON1bits.TRGSTRT = 0;               // enable Trigger generated after 0 PWM cycles
TRIG1bits.TRGCMPl=50;                  // Primary trig compare value.
    
```

Fig. 44 - Part of the function initiating ADC.

Despite the fact that the ADC module is triggered during every single PWM period, the actual duty cycle change, as well as data recording, is slowed down by the software.



Note 1: This trigger is offset by 8 counts (TRIGx = 8).

Fig. 45 - ADC Triggering [24].

Triggering circuitry allows for the triggering of the ADC using the Trigger Postscaler Start Enable Select bits in the PWM Trigger Control (TRGCON1) register. Generation of the first trigger with respect to the number of PWM cycles is adjustable. However, the default setting was used for this project because trigger delay would not have a critical impact on project results.

6.3. Analog-to-digital converter (ADC)

6.3.1. Conversion time

Conversion from voltage to a digital number, which accounts for a significant portion of the time it takes to record and store measurements, requires two steps: acquisition and conversion. The former includes the connection of the analog input pin to the sample and hold amplified (SHA) and, after specified time, disconnecting the pin in order to provide sample input voltage for the conversion process. When the sample voltage is equivalent to the input, the second process is performed. During the conversion the analog sample voltage is converted into a binary representation [27]. dsPIC33FJ16GSX02 is equipped with 2 SARs (Successive approximation ADC) [26].

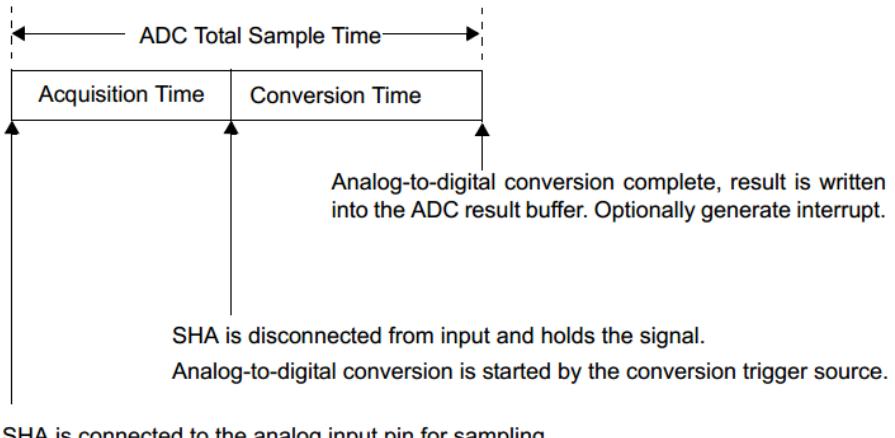


Fig. 46 - ADC sample/conversion sequence [27].

Clock Parameters						
AD50b	TAD	ADC Clock Period	35.8	—	—	ns
Conversion Rate						
AD55b	tconv	Conversion Time	—	14 TAD	—	—

Table 5 - 10-bit high-speed A/D module timing requirements [26].

An interval of at least 1 T_{AD} should be allowed between conversions for the acquisition time [27].

Calculations

$$T_{ad\ min} = 35.8 \text{ ns}$$

$$F_{ad\ max} = 27.93 \text{ MHz}$$

$$T_{conv\ min} = (14+1) * T_{ad} = 537 \text{ ns}$$

$$F_{conv\ max} \sim 1.19 \text{ MHz}$$

Clock frequency = 80 MHz

Prescaler (ADCS) = 4

$$T_{ad\ used} = 500 \text{ ns}$$

$$T_{ad} > T_{ad\ min}$$

$$T_{conv} = 15 * 500 \text{ ns} = 7500 \text{ ns} = 7.5 \mu\text{s}$$

$$T_{dc-dc\ converter} = 10 \mu\text{s}$$

$$T_{conv} < T_{dc-dc\ converter}$$

Default value of the prescaler meets the requirements. Total time of conversion is smaller than the period of the DC-DC converter.

```
ADCONbits.FORM = 0;           //Integer data format
ADCONbits.ADCS = 3;           //ADC clock = FADC/4 = 80MHz / 4 = 20MHz
```

Fig. 47 - Part of the function initiating ADC.

6.3.2. Data collection

10 bit ADC was used. The analog reference voltage is defined as the device supply voltage (AVDD/AVSS) [26]. AVDD = 3.3 V. Every single measurement point is connected to a different analog pin that is connected to ADC channels. dsPIC33FJ16GSX02 has 3 pairs of analog inputs (AN1,AN0), (AN3,AN2)... and 5 inputs are used for the project. Every time the ADC module is triggered, voltage on a certain pin is measured and saved in a corresponding buffer. For instance, the measurement of input voltage and input current is saved in buffer ADCBUF1 and ADCBUF2, that corresponds to pair (AN2, AN3).

```

// pair (AN2, AN3)
ADPCFGbits.PCFG2 = 0;           //select CH2 as analog pin
ADPCFGbits.PCFG3 = 0;           //select CH2 as analog pin
IFS6bits.ADCP1IF = 0;          //Clear ADC Pair 1 interrupt flag
IPC27bits.ADCP1IP = 4;         //Set ADC Pair 1 interrupt priority
IEC6bits.ADCP1IE = 1;          //Enable the ADC Pair 1 interrupt DISABLE/ENABLE ADC
ADSTATbits.P1RDY = 0;           //Clear the data is ready in buffer bits

```

Fig. 48 - Part of the function initiating ADC.

```

void __attribute__((__interrupt__,no_auto_psv)) _ADCP1Interrupt ()
{
    IFS6bits.ADCP1IF=0;
    adc[1] = ADCBUF1; //Vin
    adc[2] = ADCBUF2; //Iin
    ADSTATbits.P1RDY = 0;
    flagADCChannel1++;
}

```

Fig. 49 - ADCP1Interrupt, example of data collection.

7. Data recording

One of the main objectives of the project was to record the work of the whole system. Data is organized in packages, which include all the measurements and information about the duty cycle, saved in the registers of the microcontroller. At the completion of a set of measurements, the data package is coded and sent to the external memory. When the external memory is full, all data is sent back to the microcontroller and then to the PC via UART. Data is then saved using a terminal software, and recovered in order to facilitate the analysis.

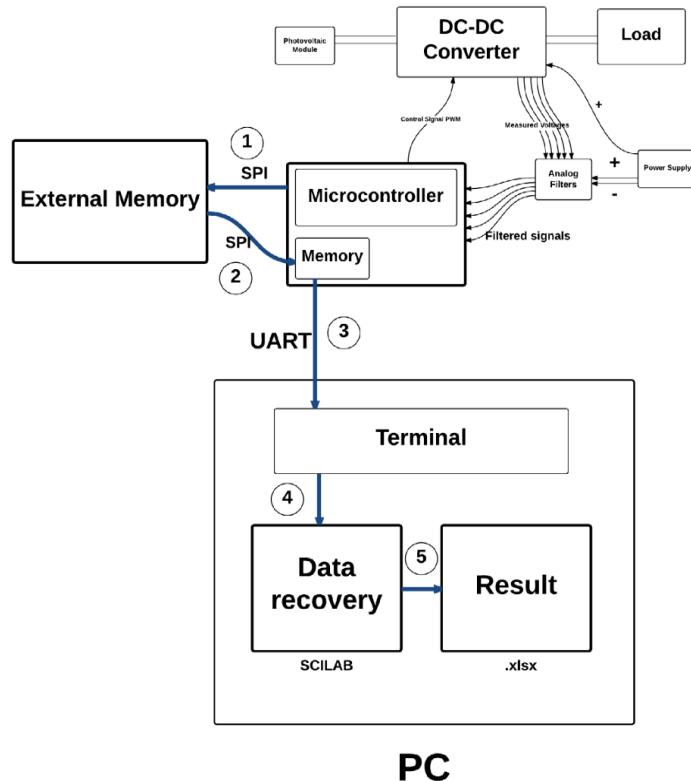


Fig. 50 - Coding and decoding, general diagram.

7.1. External memory

The external memory stores all recorded data. For this project, 23LCV1024 was chosen, as it meets the following requirements:

- achieve maximum memory storage capacity;
- achieve highest reasonable speed;
- supply voltage within the range of the 3.3 V (start board, power supply voltage);
- DIP (preferred to simplify soldering);
- ability to communicate via SPI or I²C.

Specifications

- 1 Mbit
- SRAM
- VCC Range: 2.5-5.5 V
- SPI/SDI mode
- PDIP packages
- 20 MHz clock rate
- Sequential operation

Memory can store up to 131065 bytes. Every package of data (5 channels + current duty cycle) is eight byte long. Therefore, the measurement set is 16383 lines long.

```
IFS0bits.SPI1IF = 0; // Clear the Interrupt Flag
IEC0bits.SPI1IE = 0; // Disable the Interrupt
SPI1CON1bits.DISSCK = 0; // Internal Serial Clock is Enabled
SPI1CON1bits.DISSDO = 0; // SDOx pin is controlled by the module
SPI1CON1bits.MODE16 = 0; // Communication is byte-wide (8 bits)
SPI1CON1bits.MSTEN = 1; // Master mode Enabled;
SPI1CON1bits.SMP = 0; // Input data is sampled at the middle of data
SPI1STATbits.SPIROV = 0; // Clear the Receive Overflow Flag bit
SPI1CON1bits.CKE = 1; // #Pierwsze zbocze narastajace w polowie bitu danych
SPI1CON1bits.CKP = 0; // Idle state for clock is a low level, active state is a high level
//In Master mode, the system clock is prescaled and then used as the serial clock with PLL.
//Do not set both primary and secondary prescalers to a value of 1:1.
SPI1CON1bits.SPRE = 0b110; //Secondary prescale 2:1
SPI1CON1bits.PPRE = 0b10; //Primary prescale 4:1
SPI1STATbits.SPIEN = 1; // Enable SPI module
```

Fig. 51 - Part of function initializing SPI module.

7.2. Sequential mode

While the byte mode was originally used in order to test the communication, and the functionality of the memory, the sequential mode was selected for system operations due to its higher efficiency. Sequential mode requires much less data (additional addresses), which accelerates communication. Sequential operation allows the entire array to be written to and read from.

7.2.1. Writing

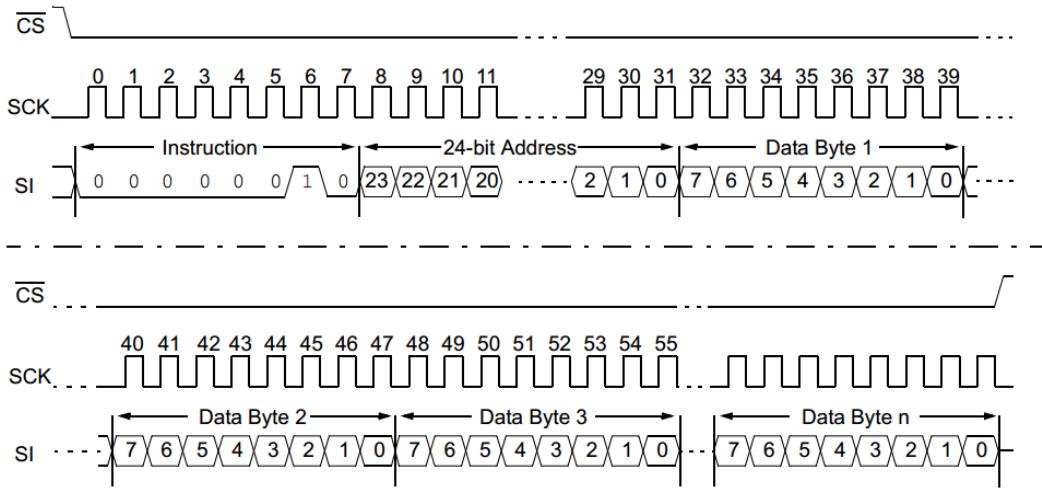


Fig. 52 - Sequential write sequence [29].

After setting CS signal low, one has to send the 1 byte of instruction (write) and 3 bytes of the address. After that, data may be sent on the SI pin. Throughout the entire operation, the clock has to be adjusted to match the bit signal. At the end of transmission, CS has to be set high. Data is sent byte by byte [29].

```

void WriteSPISequentional(unsigned char adress0, unsigned char adress1, unsigned char adress2)
//writing single memory shot to memory (5channel measurement - bytes)
{
    SPIChipSelect = 0;
    WriteSPIByte(0x02);      // WRITE INSTUCTION FOR 23LCV1024
    WriteSPIByte(adress0); //adress (24bit)
    WriteSPIByte(adress1); //adress
    WriteSPIByte(adress2); //adress
    for(i=0;i<8;i++) //send info from 5 channels
    {
        WriteSPIByte(adcToSPI[i]);
        if(pointer1SPI==0xFF && pointer0SPI==0xFF)
        {
            pointer0SPI=0x00;
            pointer1SPI=0x00;
            pointer2SPI++;
        }
        else if(pointer0SPI==0xFF)
        {
            pointer0SPI=0x00;
            pointer1SPI++;
        }
        else
            pointer0SPI++;
    }
    __delay32(SPIPrescaler*8); // 1 byte = 8 bits #Have to wait the last byte always.
    SPIChipSelect = 1;
    CheckStopCondition();
}

```

Fig. 53 - Write function using SPI.

7.2.2. Reading

After setting CS signal low, one has to send the 1 byte of instruction (read), and 3 bytes of the address. After that, data may be sent on the SO pin. Throughout the entire operation, the clock has to be adjusted to match the bit signal. At the end, CS has to be set high. Data is sent byte by byte. The rest of the data is sent without providing any additional address, however, the CS signal must be set low during the whole operation [29].

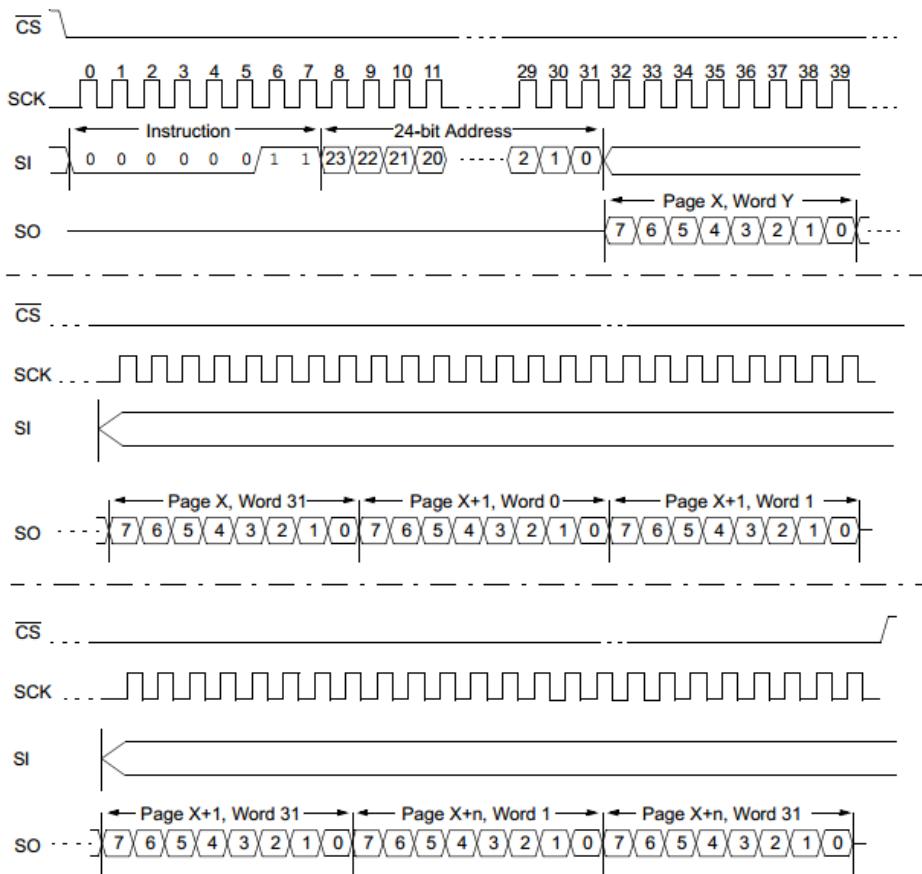


Fig. 54 - Sequential read sequence [29].

```

unsigned char ReadSPISequentionalFirstInstruction(unsigned char adress0, unsigned char adress1,
unsigned char adress2)
{
    unsigned char data;
    SPIChipSelect = 0;
    WriteSPIByte(0x03); //READ INSTUCTION FOR 23LCV1024
    WriteSPIByte(adress0); //adress (24bit)
    WriteSPIByte(adress1); //adress
    WriteSPIByte(adress2); //adress
    data = ReadSPIByte();
    return data;
}

```

Fig. 55 - Function reading the first byte.

Function `ReadSPIByte()` will be further discussed in the 10.1. Reading from SPI

```

while( U1STAbits.UTXBF == 0 ) //optimization of the transferring data, always sth in the buffer
{
    value=ReadSPIByte();
    U1TXREG = value;
}

```

Fig. 56 - Reading the rest of the data.

7.3. Coding

The data must be coded and decoded in order to be transmitted via UART and SPI. The communication modules require multiples of 8 bits, whereas the ADC is 10 bit precision. Therefore, data has to be cut before sending and restored after receiving. The measurement set starts after pressing button SW1. Every data package is saved in the function SendPackage, and sent via SPI protocol to the external memory. Data is coded in accordance with the figure 57, to allow for efficient memory usage and faster communication. The last byte is current duty cycle information.

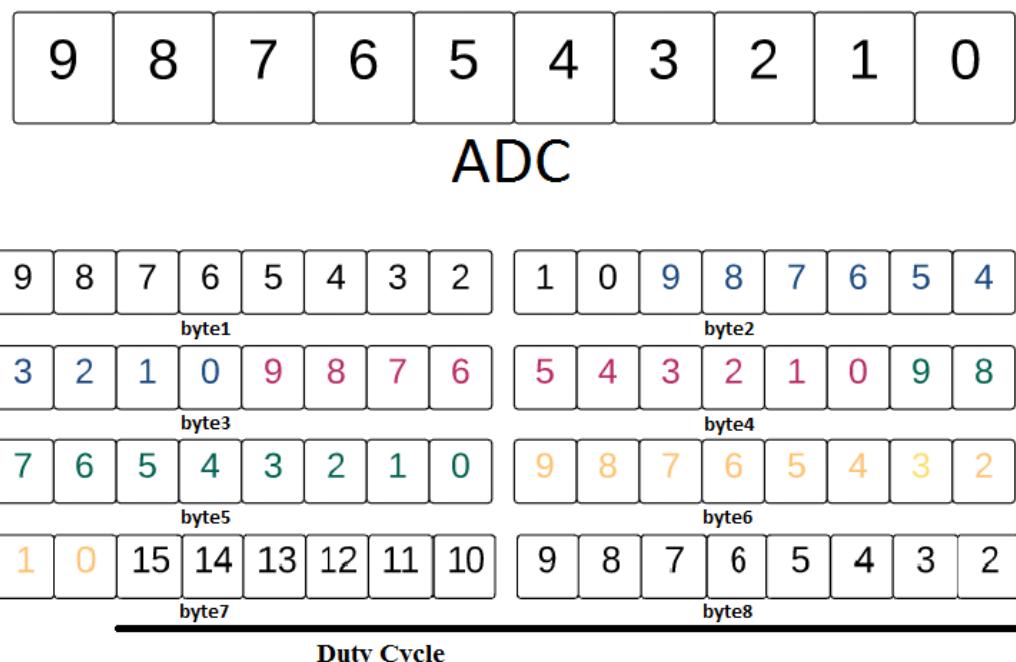


Fig. 57 - ADC coding, conversion 10 bit numbers into bytes.

```

void SendPackage(void)
{
    adcToSPI[0]=(unsigned char)((adc[0]>>2) & 0xFF);
    adcToSPI[1]=(unsigned char)((adc[0]<<6) & 0b11000000)+((adc[1]>>4)& 0b00111111)& 0xFF);
    adcToSPI[2]=(unsigned char)((adc[1]<<4) & 0b11110000)+((adc[2]>>6) & 0b00001111)& 0xFF);
    adcToSPI[3]=(unsigned char)((adc[2]<<2) & 0b11111100)+((adc[3]>>8) & 0b00000011)& 0xFF);
    adcToSPI[4]=(unsigned char)((adc[3]) & 0xFF);
    adcToSPI[5]=(unsigned char)((adc[4]>>2) & 0xFF);
    adcToSPI[6]=(unsigned char)((adc[4]<<6) & 0b11000000)+((CurrentMDC>>8) & 0b00111111)& 0xFF);
    adcToSPI[7]=(unsigned char)(CurrentMDC & 0xFF);
    WriteSPISequential(pointer2SPI,pointer1SPI,pointer0SPI);
}

```

Fig. 58 - function coding the shot of data.

7.4. UART - data transmission

```

IFS0bits.U1TXIF = 0; // clear TX interrupt flag
if(flagDisableADC==0)
{
    IEC6bits.ADCP0IE = 0;      //DISABLE ADC pair0
    IEC6bits.ADCP1IE = 0;      //DISABLE ADC pair1
    IEC7bits.ADCP2IE = 0;      //DISABLE ADC pair2
    flagDisableADC=1;
}

while(U1STAbits.UTXBF == 0) //optimization of the transferring data
{
    value=ReadSPIByte();
    U1TXREG = value;
}
if(flagUARTEN==MAXUART)
{
    SPIChipSelect = 1;
    U1MODEbits.UARTEN = 0; // Disable UART
    U1STAbits.UTXEN = 0;   // Disable UART TX
}
flagUARTEN++;

```

Fig. 59 - UART interrupt.

After one measurement set (when the external memory is full, approximately 5 minutes), ADC is disabled, and the data is read from the external memory and sent to PC via UART.

Baud rate calculations

$$\text{Baud Rate} = \frac{F_{CY}}{16 \times (UxBRG + 1)} \dots\dots(1)$$

$$UxBRG = \frac{F_{CY}}{16 \times \text{Baud Rate}} - 1 \dots\dots(2)$$

Note: F_{CY} denotes the instruction cycle clock frequency ($\text{Fosc}/2$).

Fig. 60 – Equations for baud rate [30].

Baud rate was set to the maximum functional rate of 57600. For higher values, the terminal was not able to receive the data correctly.

```
#define FCY 40550400
#define BAUDRATE 57600
```

Fig. 61 - Defining baud rate constants.

Besides the regular UART initialization, such as setting the parity bits and adding stop bits to the number of bits in each transmission, there is an additional setting that is worth mentioning. It is Transmission Interrupt Mode setting.

bit 15,13	UTXISEL<1:0> : Transmission Interrupt Mode Selection bits
11	= Reserved; do not use
10	= Interrupt when a character is transferred to the Transmit Shift register, and as a result, the transmit buffer becomes empty
01	= Interrupt when the last character is shifted out of the Transmit Shift register; all transmit operations are completed
00	= Interrupt when a character is transferred to the Transmit Shift register (this implies there is at least one character open in the transmit buffer)

Fig. 62 - Transmission Interrupt Mode setting [26].

Because the UART transmission is based on interrupts, it is important to set the appropriate interrupt time for triggering. It was decided to choose the mode in which each interruption is generated to the Transmit Shift register. This means that the interruption is generated before the transmission, which allows the data transmission to operate faster.

7.5. Decoding

After the data is present in the PC, it still has to be decoded. If it is not returned to the pre-coded state, the data is impossible to analyze. All the data is transferred via one of the microcontroller's pins. The start board is equipped with single UART communication channel via USB bridge. The dsPIC30F/dsPIC33F and PIC24 devices use an on-board PIC18 and USB interface for UART communications. There is a switch in the start board that allows the

PIC18 device to communicate with the target device through the UART module [23]. PIC18 is connected to the PC by UART cable, and the data is gathered using the terminal software - RealTerm Capture Program 2.0.0.7.0. The software enables the data to be saved in a text file. The raw data from the measurement set can be processed further. The software used for additional processing is called Scilab, which was already available in the laboratory; however, it could have been done in any environment.

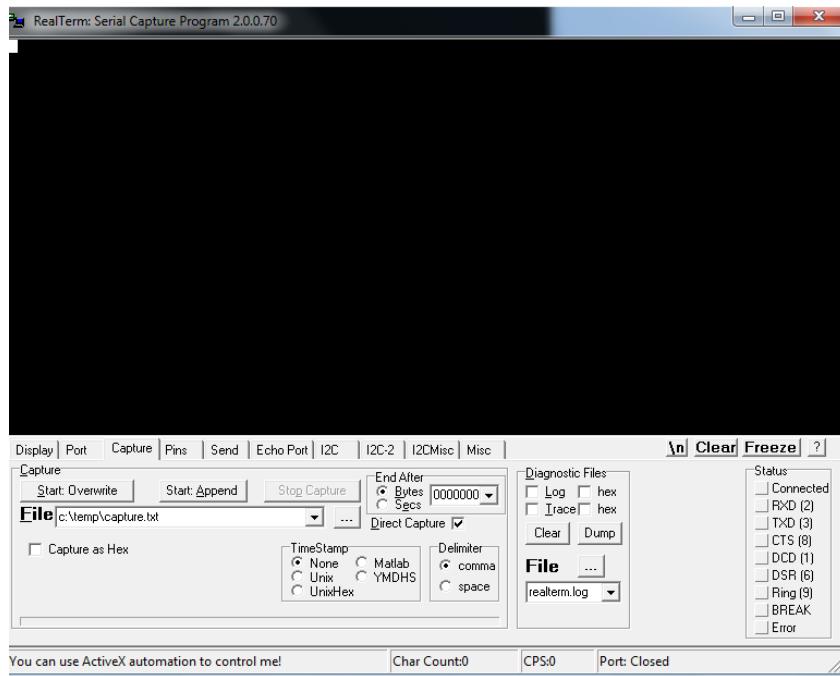


Fig. 63 - RealTerm Capture Program 2.0.0.7.0.

```

for i = 1:LineSpace
    M(i,j) = bitand(((data(j+k)*2^2)+data(j+k+1)/2^6), uint16(1023)); //0b0000001111111111
    M(i,j+1) = bitand(((data(j+k+1)*2^4)+data(j+k+2)/2^4), uint16(1023));
    M(i,j+2) = bitand(((data(j+k+2)*2^6)+data(j+k+3)/2^2), uint16(1023));
    M(i,j+3) = bitand(((data(j+k+3)*2^8)+data(j+k+4)), uint16(1023));
    M(i,j+4) = bitand(((data(j+k+5)*2^2)+data(j+k+6)/2^6), uint16(1023));
    if s(1,2)>k+7 then k=k+7; end;
    count1=count1+1;
end;

```

Fig. 64 – Part of the program decoding the data (Scilab).

A	B	C	D	E	F	
1	Duty cycle	Channel0 - I _{source} [mA]	Channel1 - V _{in} [V]	Channel2 - I _{in} [mA]	Channel3 - V _{out} [V]	Channel4 - I _{out} [mA]
2	0.482371	111.767578	3.231680	103.784180	5.233277	36.355168
3	0.482371	111.767578	3.231680	103.784180	5.233277	36.355168
4	0.482371	125.073242	3.206133	111.767578	5.211563	37.337740
5	0.482371	114.428711	3.225293	106.445313	5.254992	36.355168
6	0.482371	111.767578	3.231680	106.445313	5.233277	36.355168
7	0.482371	111.767578	3.231680	103.784180	5.233277	36.355168
8	0.482371	111.767578	3.225293	106.445313	5.233277	36.355168
9	0.482371	103.784180	3.244453	98.461914	5.233277	35.863882
10	0.482371	109.106445	3.225293	103.784180	5.233277	36.355168

Fig. 65 - Example of raw data ready for analysis.

8. Perturb and observe algorithm (P&O)

P&O is one of the simplest and most frequently used algorithms for MPPT. PV operating voltage is set by modifying converter duty cycle. Both increasing voltage on the left side of the MPP and decreasing voltage on the right side of the MPP will increase power. After performing an increase in the panel operating voltage, the algorithm compares the current power reading with the previous one. If the power has increased, it keeps the same direction and increases voltage, otherwise it changes direction and decreases voltage. This process is repeated until the MPP is reached and algorithm oscillates around the correct value. The size of the step determines the size of the deviation while oscillating about the MPP and the speed of achieving it.

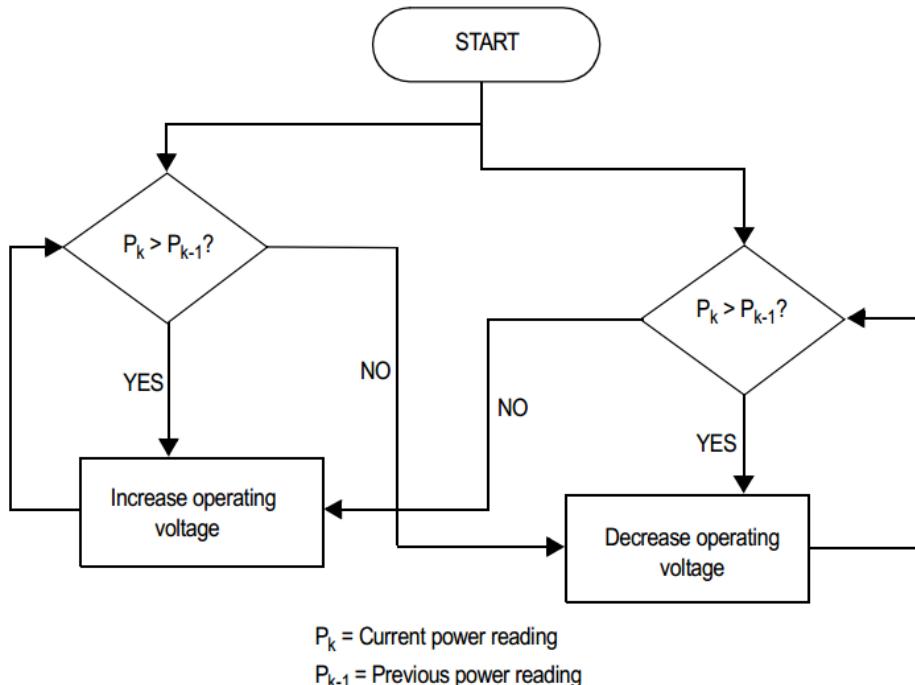


Fig. 66 – Perturb and observe algorithm, block diagram [28].

Input: V_{in} , I_{in}

Output: PWM duty cycle

```

Pin=Vin*Iin; Pins = Pins + Pin; c++;
if(c==10000) //Slowing down the process
{
    c=0;
    Pinm=Pins/10000;
    DPin = Pinm - Pinb;
    DMDC = MDC - MDCb;
    MDCb = MDC;
    if((DPin > 1)&&(MDC<8500))
    {
        if (DMDC>=0)
            {MDC = MDC+50;} // Increment of 5%
        else
        {
            if(MDC>950)
                {MDC = MDC-50;} // Decrement of 5%
        }
    }else if((DPin < -1)&&(MDC>950))
    {
        if (DMDC>0)
            {MDC = MDC-50;} // Decrement of 5%
        else
        {
            if(MDC<8500)
                {MDC = MDC+50;} // Increment of 5%
        }
    }
    Pinb = Pinm;
    Pins = 0;
}

```

Fig. 67 - Implemented algorithm, code.

Variables description:

V_{in} - Input voltage measurement

I_{in} - Input current measurement

P_{in} - Input power

P_{ins} - Accumulated input power

P_{inm} - Average input power

P_{inm} - Post average input power (auxiliary variable)

DP_{in} - Change of Input input power

MDC - Current duty cycle

MDC_b - Post duty cycle (auxiliary variable)

c - counter

It is worth mentioning that the fixed 5 % step of the duty cycle change is a very important characteristic of the algorithm. The smaller the step, the faster MPP point will be found. However, a smaller step also results in higher losses from the oscillations. The step value should be further investigated in the future. The other fixed value, 10000 for the c variable (which slows down the process), may also be changed. There are also minimum and maximum values for duty cycle to be set. It is inextricably linked to the functioning of the DC-DC converter. Crossing this value may cause the DC-DC converter to stop working or to work improperly. The algorithm itself is not the most significant part of the project. For that reason, the basic algorithm „Perturb and Observe” was implemented. The goal of this project was to facilitate further analysis of the algorithms and their effect on efficiency of the MPPT. Data analysis is out of scope. Any other algorithm can be implemented that uses any measured data [28].

9. Tests

9.1. ADC + PWM

The first test, besides the diode blinking, was to check if ADC and PWM module are working correctly. On the development board there is a potentiometer connected directly to one of the ADC channel pins. Thanks to that, it was easy to make a function where the input is the measurement of the voltage from the potentiometer, and the output is the duty cycle of the PWM. Turning the potentiometer knob produced a change in the duty cycle, so that the minimum potentiometer setting resulted in a low state of pin voltage, the middle setting of the knob gave an output of 50 % duty cycle, and the maximum setting resulted in a high state of pin voltage. Unfortunately the potentiometer has broken, so it was not possible to check that later on. However, since it worked the first time, it would likely produce the same result in the future.

9.2. UART - byte by byte

The purpose of the test was to check if the UART transmission as well as terminal software were working correctly. The idea was to send constantly one byte of data e.g. "a" character coded in ASCII. The result was positive.

9.3. Memory test

The memory test was one of the most important and difficult tests at the same time, because it is impossible to check separately data writing and reading. One had to check both of these functions at the same time. For simplicity, the first attempt was to establish communication with the external memory using the byte mode (not sequential). Fortunately, after small changes in the initializing function of SPI, and the way of receiving data from the external memory (further discussed in the section 10.1. reading from SPI), communication was established. The data sent and received was checked in the oscilloscope together with the clock and CS signal. The data was also compared with the data received in the terminal.

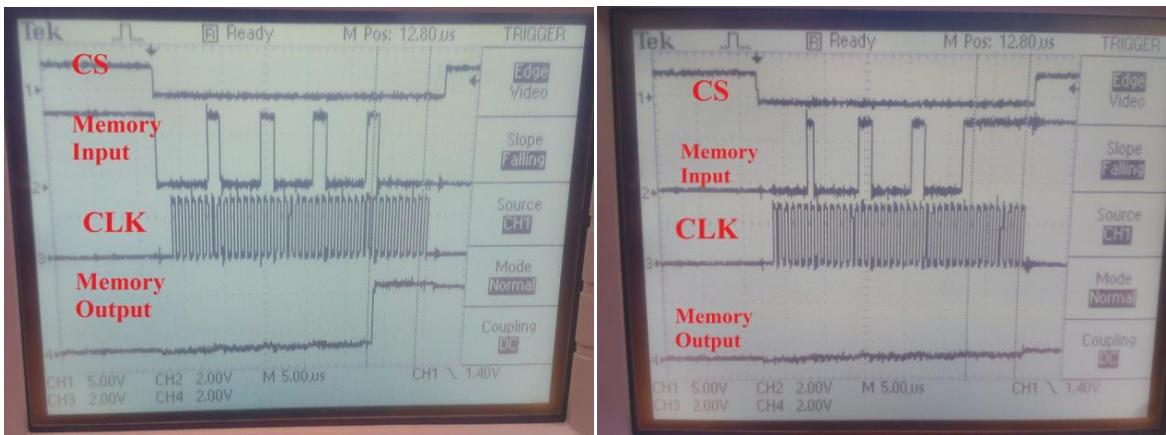


Fig. 68 - Data reading from memory.

Fig. 69 - Data writing to memory.

Figures 68 and 69 present oscilloscope readings from data reading and writing. In this case, data is 0xFF because it is easy to present, however, more values were tested. For both cases, CS is lower during the operation, and the clock is pulsing. For memory input, the first byte is different, because for one operation the Read (0x03) or Write (0x02) were sent. The next 3 bytes are the same, it is the address (0x03, 0x03, 0x03) which was chosen to be different from 0x00, 0x00, 0x00 for the purpose of representation. The last byte is the actual data (0xFF). For the memory output, it is low all the time, besides the last byte for memory reading, which is the data read.

9.4. Transmission test

The next test was for checking if every single byte can be sent correctly. The other reason was to check the terminal software limitation. Every single character from 0x00 to 0xFF was sent to the external memory, read, and sent via UART. Data was received and saved in HEX format using the Real Term Capture Program 2.0.0.7.0. It turned out that the data saved as a text file was correct. Thanks to that test, one could be sure that there is no limitation of the

characters set while sending, and that there were no errors with the coding or decoding module.

9.5. ADC and transmission test

This test was checking the synchronization of the ADC module together with the reading and writing to the external memory, as well as sending coded data to the PC via UART and decoding it using Scilab software. The measurement was taken from the five resistors of equal value of resistances connected in series, where one end was connected to the reference voltage (3.3 V), and the other end was connected to the ground. The voltages were measured with a multimeter and then compared with the values received from the microcontroller.

	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5
Multimeter	3,27	2,36	1,45	0,84	0,42
% of reference voltage	100,00 %	72,17 %	44,34 %	25,69 %	12,84 %
Expected value	1023	738	454	263	131
Received value	1023	736	443	281	115
Error (Exp. Value - Received value)	0	2	11	-18	16
Relative error [%] (Error/maximum ADC result [1023])	0,00 %	0,23 %	1,04 %	-1,78 %	1,60 %

Table 6 - ADC and transmission test results.

The test results are satisfactory, proving that the whole module works. There is a discrepancy between expected value and received value, due to the fact that both the ADC and multimeter are encumbered with error. Maximum relative error is less than 2 %, therefore the results are acceptable.

9.6. Sequential mode test

Next step was to change the byte mode of SPI communication to sequential, described in the section 7.2. This test was very similar to the ADC + transmission. This time a small fluctuation of the received data could be easily seen while sending bigger amount of measurements. It was the proof that the measurement is not ideal, with a small relative error (< 2 %).

9.7. Filtering test

The output from all the filters was checked using the oscilloscope. More than one duty cycle value was checked, however, only the value of 75 % is presented. Channel 1 is a PWM signal, and channel 2 is the output described in below every figure.

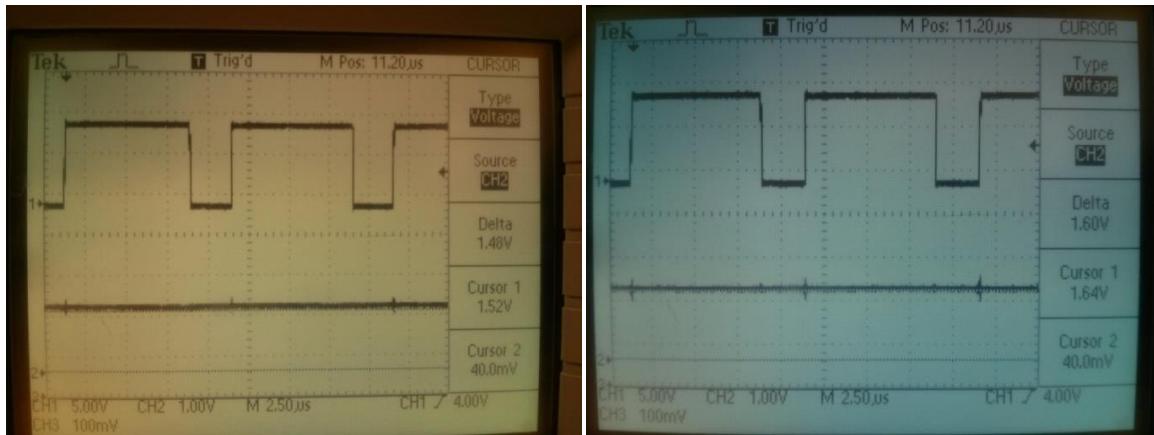


Fig. 70 - Filtered V_{in} , for duty cycle = 75 %. Fig. 71 - Filtered V_{out} , for duty cycle = 75 %.

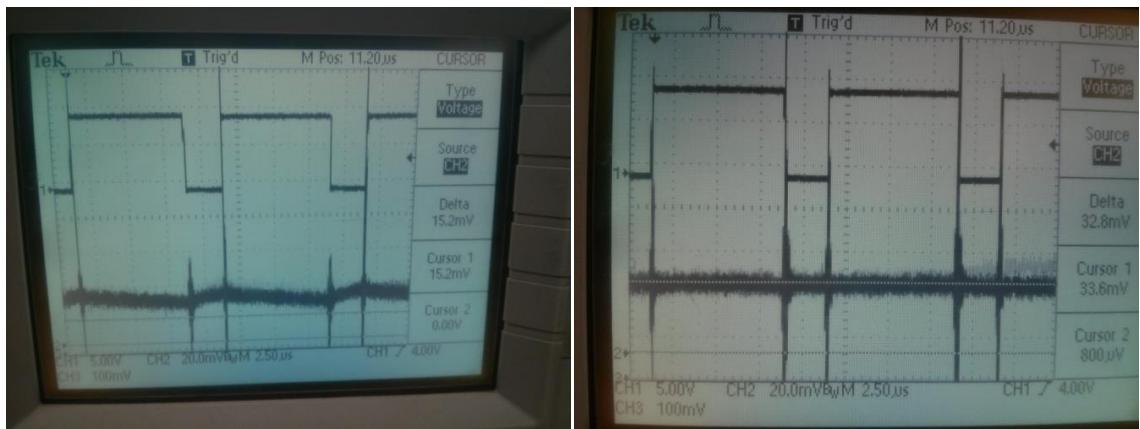


Fig. 72 - Filtered I_{in} , for duty cycle = 75 %. Fig. 73 - Filtered I_{out} , for duty cycle = 75 %.

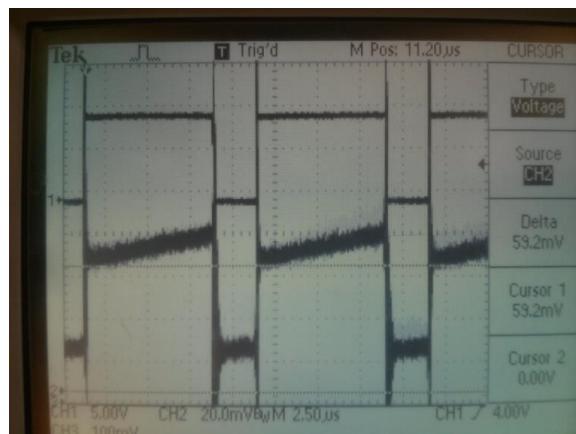


Fig. 74 - Filtered I_{source} , for duty cycle = 75 %.

9.8. Results

A number of measurements were performed in order to check the overall functionality of the system. An example data depicted below is a measurement of two different irradiation (470 W and 200 W). The algorithm starts from certain duty cycle, in that case is equal to 0.5 and starts to track MPP. Data is divided into 5 regions, according to the order of the data collection.

1. 470 W tracking the point - tracking the point of 470 W, starting from the duty cycle equal to 0.5.
2. 470 W stabilization - stabilization at point 470 W, the number of data is much greater than the number of data of the previous region.
3. 470 W → 200W - dynamic change of the irradiation, corresponding to the change of the power of the array of halogen lamps from 470 W to 200 W.
4. 200 W tracking the point - tracking the point of 200 W.
5. 200 W stabilization - stabilization at point 200 W, the number of data is much greater than the number of data of the previous region.

Additionally, the IV curves of the module were added. Unfortunately, the conditions of the measurement of IV curve and the conditions during the measurements of the entire system are not identical (e.g. temperature may be different), however, IV curves of the PV were also presented in the figures, because they can work as a reference.

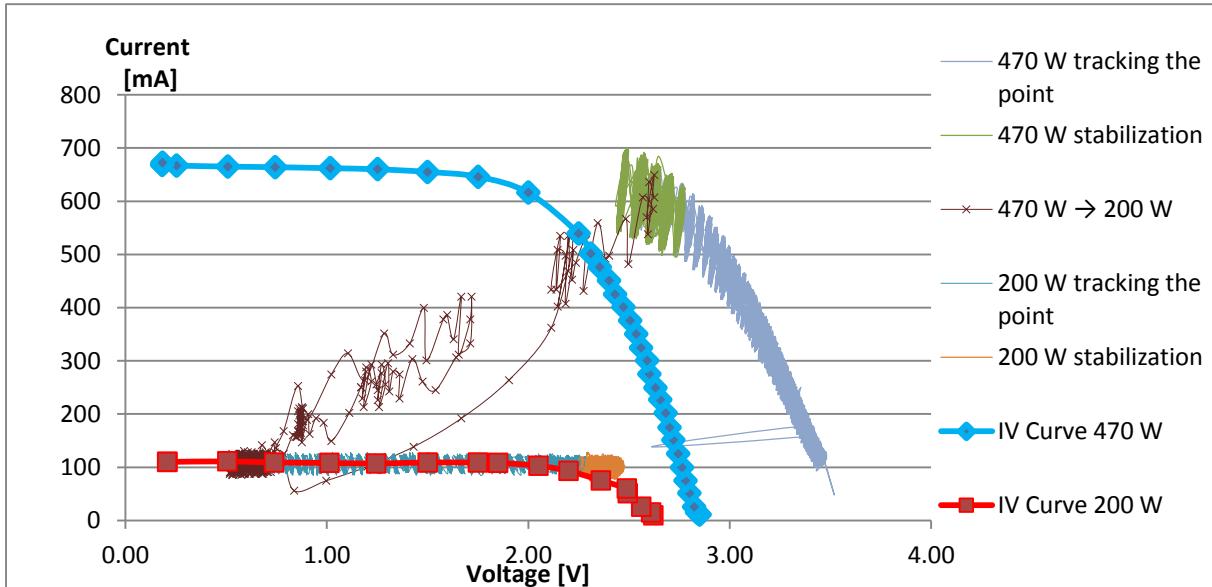


Fig. 75 - Example data, $I_{in} = f(V_{in})$.

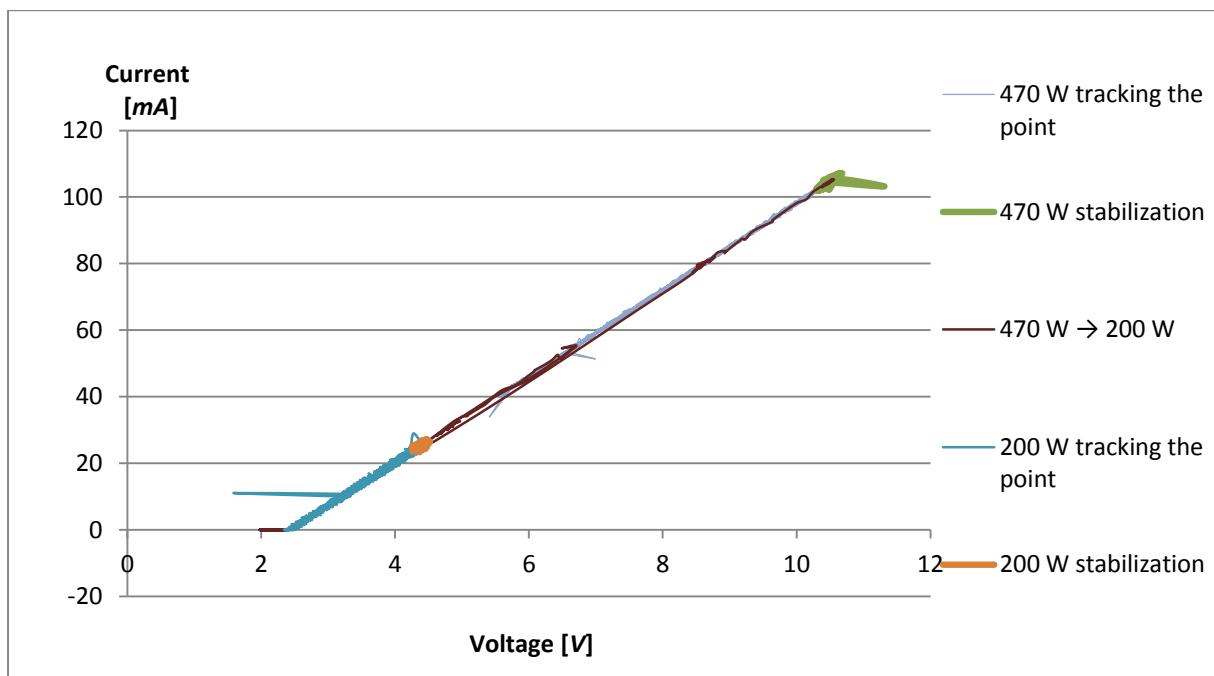


Fig. 76 - Example data, $I_{out} = f(V_{out})$.

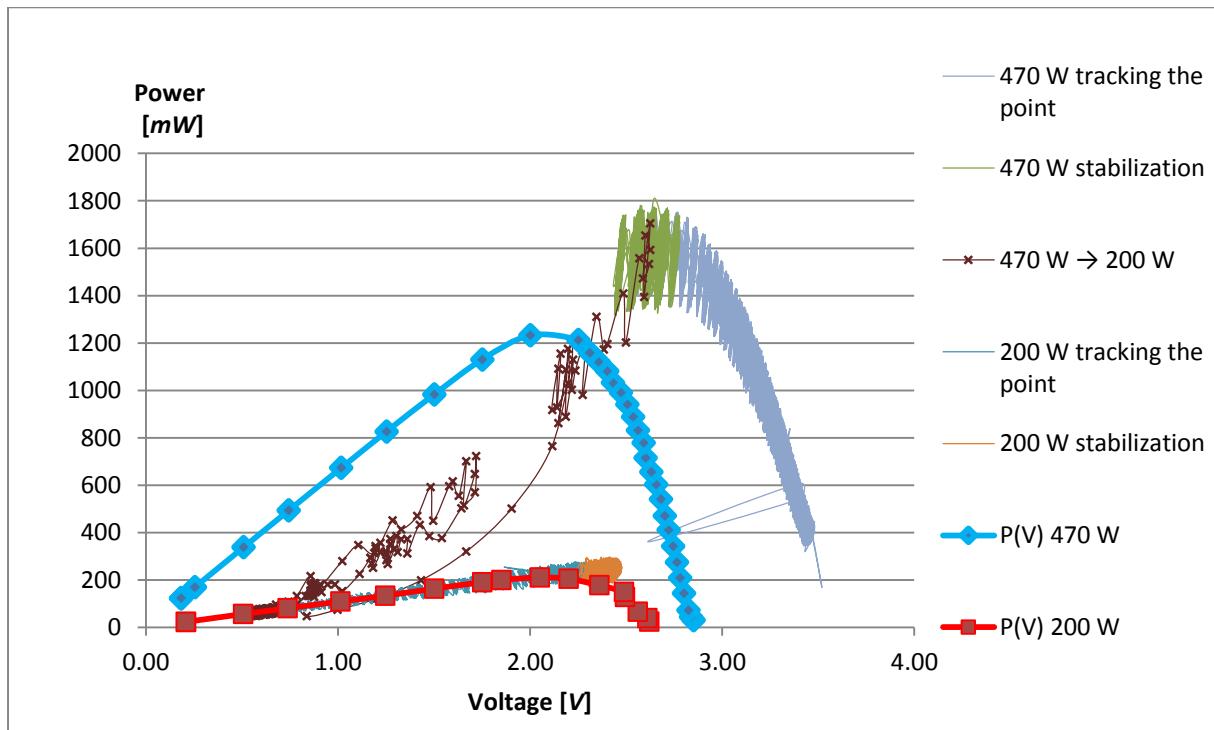


Fig. 77 - Example data, $P_{in} = f(V_{in})$.

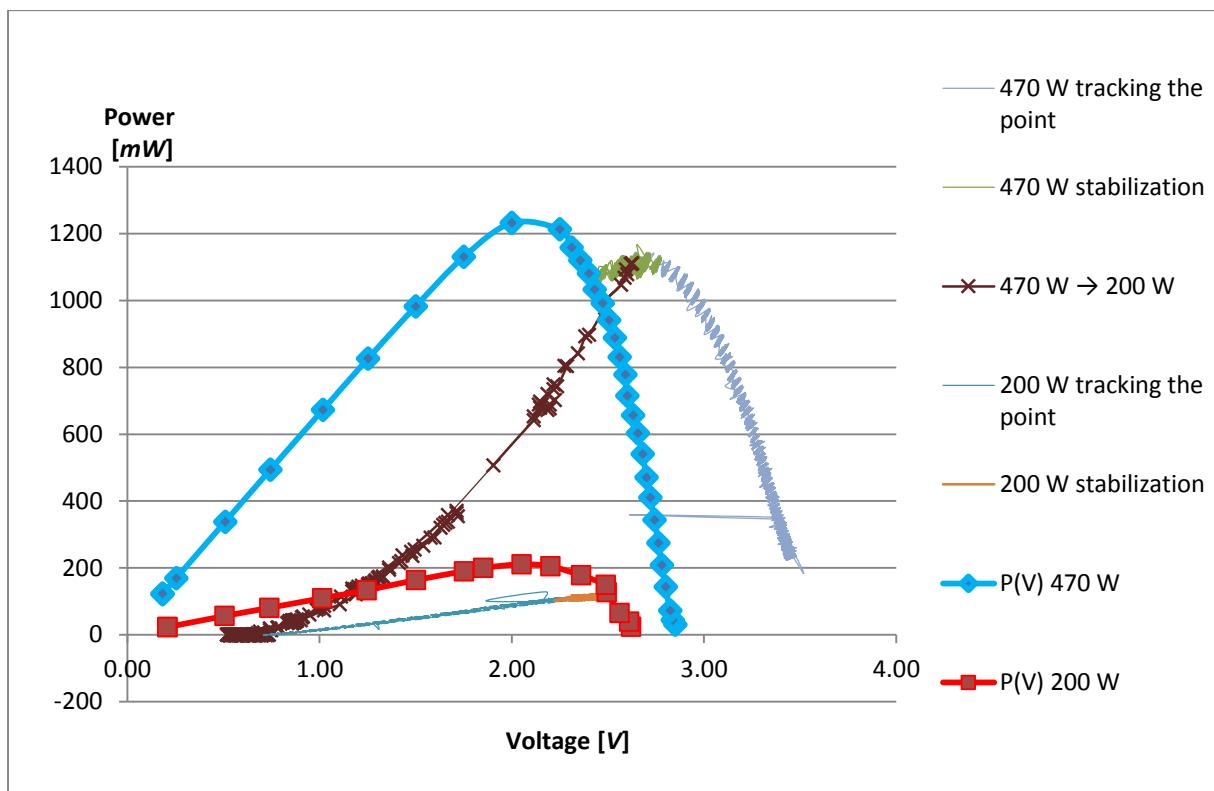


Fig. 78 - Example data, $P_{out} = f(V_{in})$.

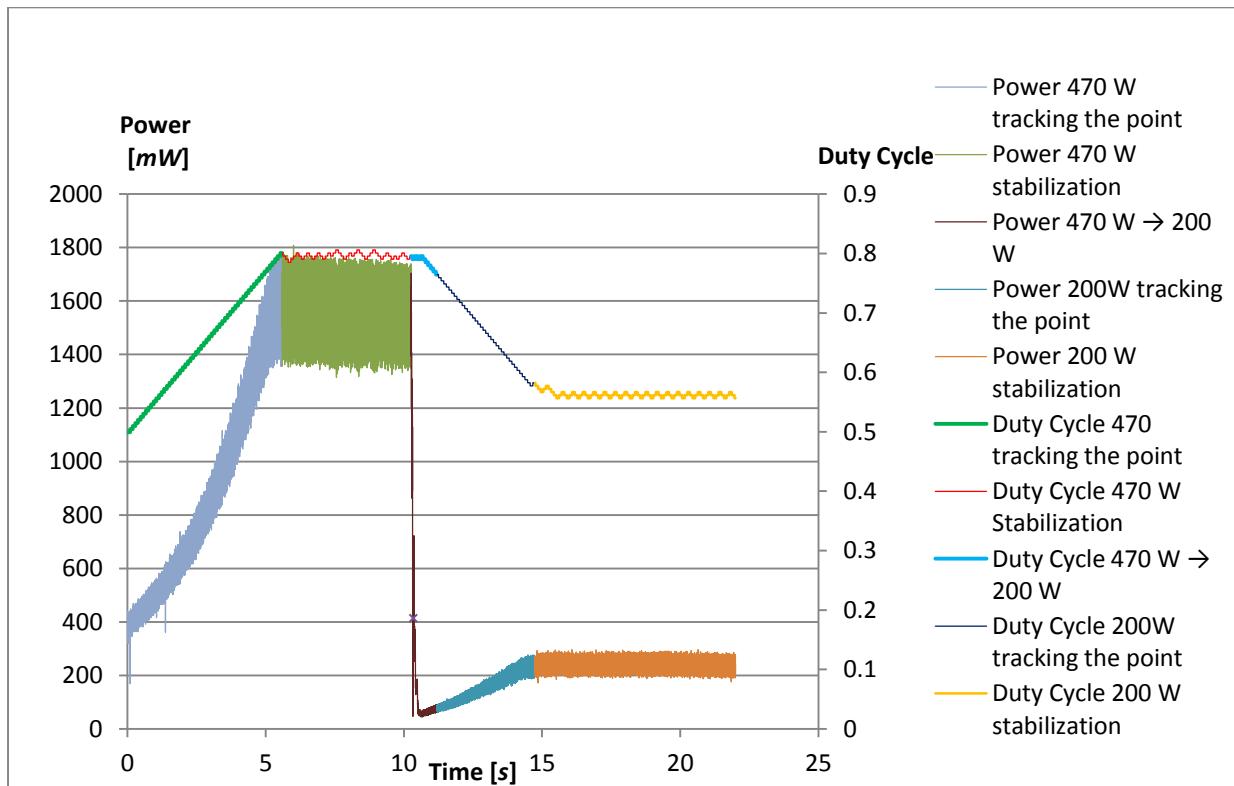


Fig. 79 - Example data, $P_{in} = f(t)$, $\text{Duty Cycle} = f(t)$.

The results prove that the entire systems works correctly. The MPPT function performs tracking of maximum power point and the data is recorded at a high sampling rate.

10. Encountered problems

10.1. Reading from SPI

For some reason the microcontroller was not able to receive the data from the external memory, despite the fact that the signals on the oscilloscope of SI, SO, CLK, CS, and power supply seemed to be correct. It turned out that function for reading the byte was wrong.

```
unsigned char ReadSPIByte(void)
{
    unsigned char  data;
    SPI1BUF=0x00;
    while(SPI1STATbits.SPITBF);
    data = SPI1BUF; // read, in order to avoid overflow when the new data comes
    SPI1STATbits.SPIROV=0;
    while(!SPI1STATbits.SPIRBF);
    if(SPI1STATbits.SPIRBF)
        {return SPI1BUF;}
    return -1;
}
```

Fig. 80 - ReadSPIByte function (improved).

Unfortunately, it was impossible to read the measured value from ADC with one simple instruction. Figure 80 above is the result of many attempts to produce a program properly reading the byte. The program includes checks for multiple flags, which increased the complexity of the writing process. The SPI1 Data Receive/Transmit Buffer register (SPI1BUF) is comprised of two separate internal registers: the Transmit Buffer (SPI1T1B) and the Receive Buffer (SPI1R1B). These two unidirectional, 16-bit registers share the SFR address of SPI1BUF. If a user writes data to the SPI1BUF address, the data is written internally to the SPI1TXB register. When the user reads the data from SPI1BUF, the data is read internally from the SPIxR1B register [31].

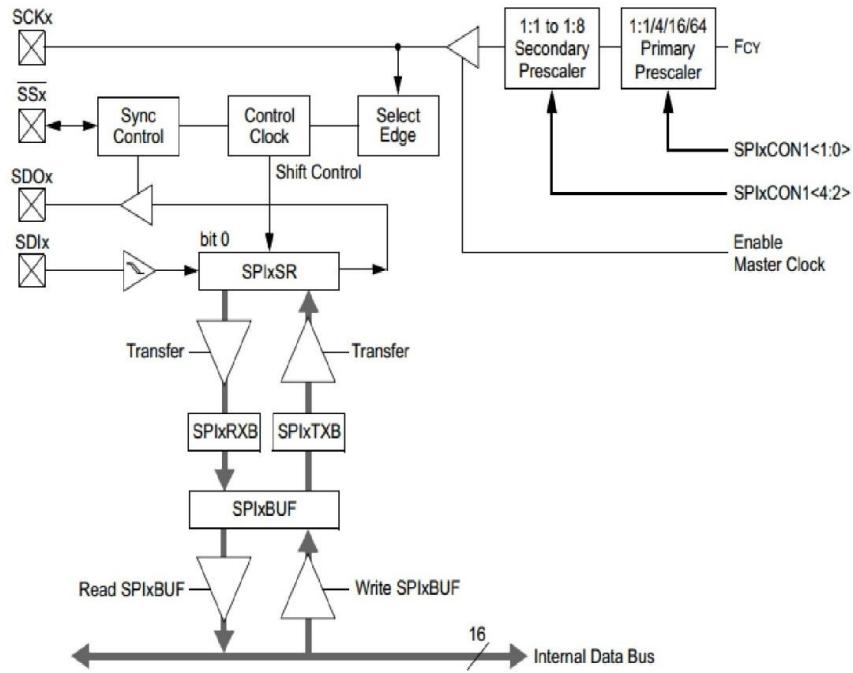


Fig. 81 - SPI module block diagram [31].

It turned out that function ReadSPIByte had to check SPITBF flag bits twice. At first, one had to read the SPI1BUF flag and set SPIROV (Receive Overflow Flag bit) to "0" in order to be sure that there is no overflow. After that, one can wait for the data to come in a while loop, where SPIRBF bit is checked (Reception complete), which means that SPI1RXB is full. Only then, can the data be saved.

10.2. Unexpected instability of the opamp

For unknown reasons, the I_{source} filter was unstable. The output was highly oscillated, and values of voltage were unexpected, in spite of the PSpice simulation for a given model of opamp.

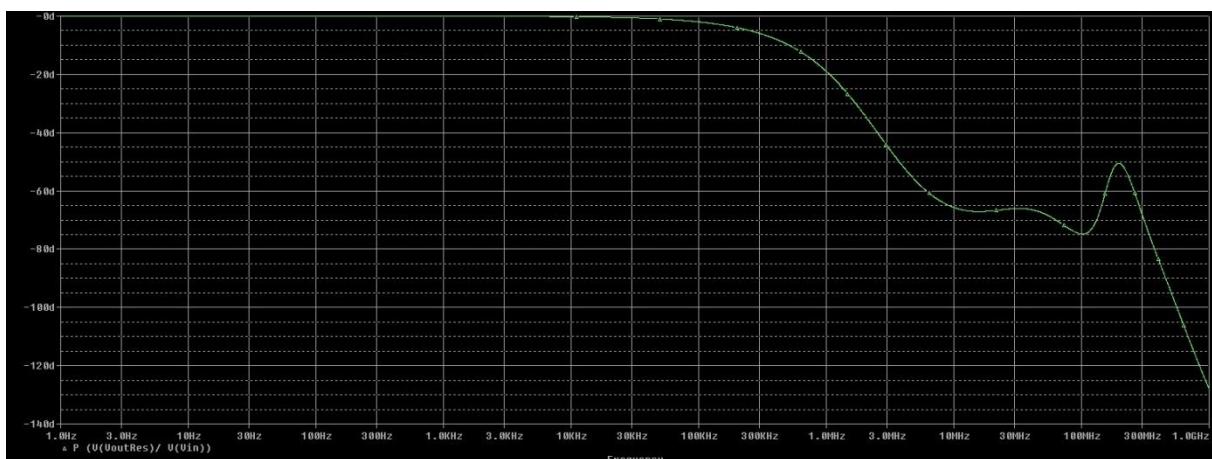


Fig. 82 - AC simulation, phase shift, I_{source} filter, LM6181.

Up to 1GHz, the phase shift does not cross 180 degrees, which means that the circuit should be stable up to that frequency. Unfortunately, it was instable in practice. The solution of the problem was choosing an opamp with very similar features. The chip was changed to LM617, which worked without any additional simulation.

11.3 Unexpected data from the ADC

While using five channels, usage of flags for each interrupt was needed. Due to the fact that all ADC interrupts are triggered by PWM exactly at the same time, one has to be sure that the source of data read from the buffer is appropriate. In order to check the correctness of the ADC interrupt frequency occurrence, the additional instruction blinking the diode was added to each interrupt, and the frequency was slowed down. Unfortunately, frequencies of various diodes linked to the interrupts were not appropriate. While using the counter, the frequency of each was not equal, and not expected. The counter had to be substituted by the flags flagADCChannel0, flagADCChannel1, and flagADCChannel2.

```
void __attribute__((__interrupt__,no_auto_psv)) _ADCP0Interrupt ()
{
    (...) //Reading from ADC
    flagADCChannel0++;

}

void __attribute__((__interrupt__,no_auto_psv)) _ADCP1Interrupt ()
{
    (...) Reading from ADC
    flagADCChannel1++;

}

void __attribute__((__interrupt__,no_auto_psv)) _ADCP2Interrupt ()
{
    (...) Reaading from ADC + Algorithm
    flagADCChannel2++;

    if(flagADCChannel0 & flagADCChannel1 & flagADCChannel2)
    {
        flagADCChannel0=0;flagADCChannel1=0;flagADCChannel2=0;
        (...) Sending Data to external memory
    }
}
```

Fig. 83 - ADC interrupts.

10.3. Interferences on SPI clk pin

After soldering the external memory 23LCV1024, and after performing the tests for the external memory that gave positive results, additional problems with the data reception occurred. For some reason, the received data was encumbered with periodically repeating errors. It was not the case of completely wrong data, but the change of a few bits every 50-100 bytes. An additional check for the connections of the cable was performed, changing the moment of ADC triggering (TRGCM register) and the coding/decoding code. No flaws were encountered. The next attempt was remapping the input, output and clk pin of the SPI on the side of the microcontroller, which solved the problem. The reason was unexpected interferences on pin 18 used as a clk pin.

10.4. Design of the current filters

At first, all filters were thought to be second-order filters, due to the obvious advantage of better filtration (40 -dB/decade vs -20 dB/decade attenuation). When it came to voltage filtration, where the gain was supposed to be equal to one, there were no problems with implementation of Sallen-Key topology. However, that could not have been done with the current filters because of the higher gain. Maximum gain for Sallen-Key topology is 3 [18]. Other second-order filters were much more complicated. Simplicity and reliability were prioritized over complexity, therefore first order filters were implemented.

10.5. Single voltage supply

Due to the fact that the DC-DC converter needed only a positive voltage from the power supply (MOSFET driver), the idea was to power analog filters only with positive voltage. This would have produced a simpler system. However, the simulation demonstrated that the system would not work with only positive voltage. Additional elements were required in order to center the opamp's output voltage at mid-supply. In addition, single supply opamp circuits exhibit additional problems, such as a large input common-mode voltage or high vulnerability to reverse voltage breakdown [32]. When the output current of opamp is large, instability is likely to occur. In this scenario, the large output current is causing large signal voltages on the supply line. Instability results from the large signal voltages fed back to the opamp from the supply line, as this is the reference source for the opamp's non-inverting input [33]. It would be possible to use single voltage, but the circuitry would be too complex and may be not as

reliable as dual supply. Once again, the simplicity and reliability was a priority over complexity, therefore first order filters were implemented.

11. Summary and conclusions

11.1. Summary

All project success criteria were achieved. The measurement system was designed, simulated, and implemented. PCB was redesigned, and communication with external memory and PC were both implemented and tested in order to be able to perform the analysis of the data on PC. All the modules were combined, and the project was confirmed to work in accordance with the assumptions.

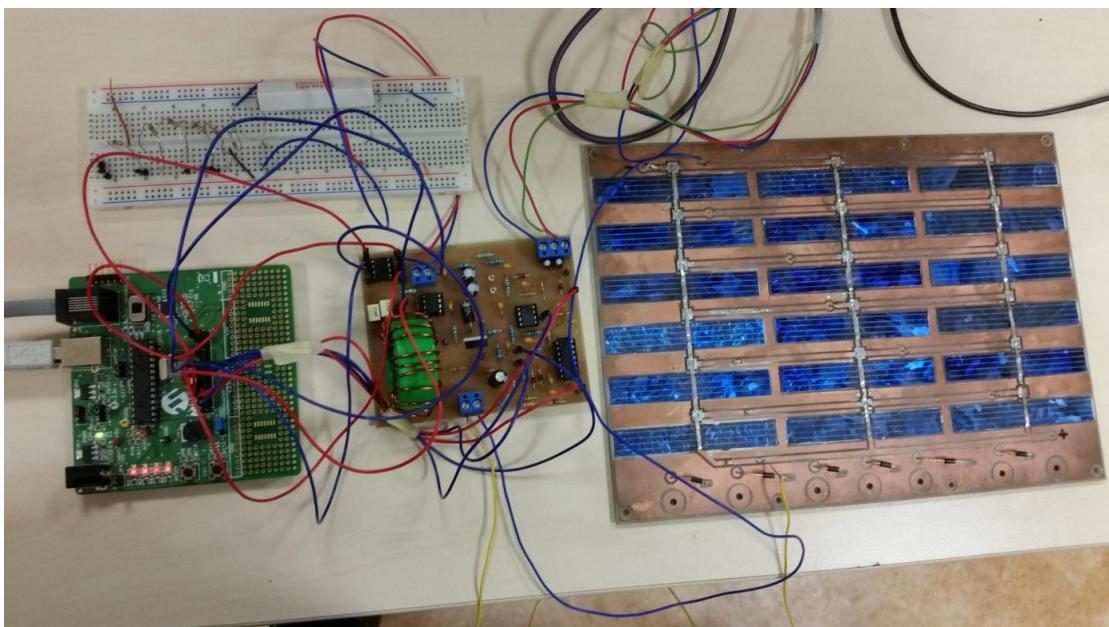


Fig. 84 - Final system.

11.2. Conclusions

Maximum power point tracker of photovoltaic module is ready to operate and it is possible to record its operation in dynamic states. Data analysis from input current, input voltage, output current, output voltage and current of the source of transistor can be performed, together with the current duty cycle value. The system is prepared for the implementation of various algorithms in order to control MPPT and for enabling their comparison. Many parameters of the system can be changed, such as: time for change of duty cycle value, frequency of the PWM control signal, duty cycle step, time for change of ADC trigger, and period that each data package is sent, in order to check the efficiency of the applied algorithm for the boost converter.

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Oświadczam, że poinformowano mnie o zasadach dotyczących kontroli oryginalności pracy dyplomowej w systemie antyplagiatowym.

Wyrażam zgodę na przetwarzanie^{*)} mojej pracy dyplomowej, a także na przechowywanie jej w celu realizowania procedury antyplagiatowej w bazie danych systemu antyplagiatowego.

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^{*)} Przez przetwarzanie pracy rozumie się porównywanie przez system antyplagiatowy jej treści z innymi dokumentami (w celu ustalenia istnienia nieuprawnionych zapożyczeń), generowanie Raportu Podobieństwa oraz przechowywanie pracy w bazie danych systemu antyplagiatowego.

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*) Wpisać odpowiednio: inżynierska, magisterska.

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