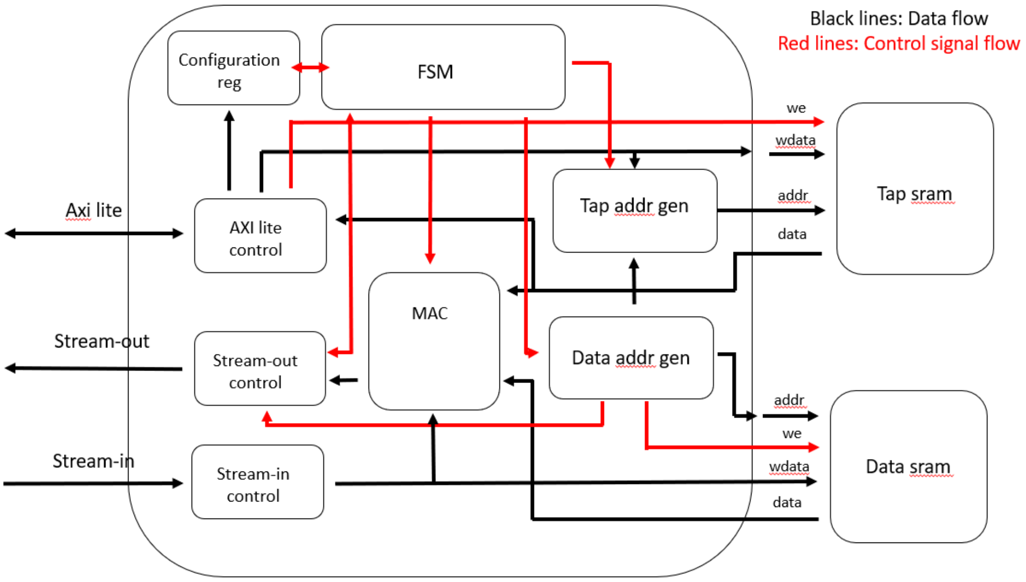
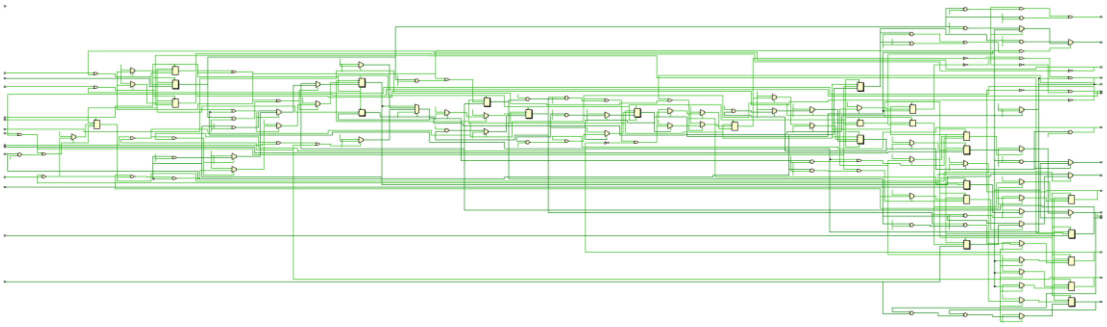
# Lab3 Report

## 1. Block diagram:





## 2. Operation

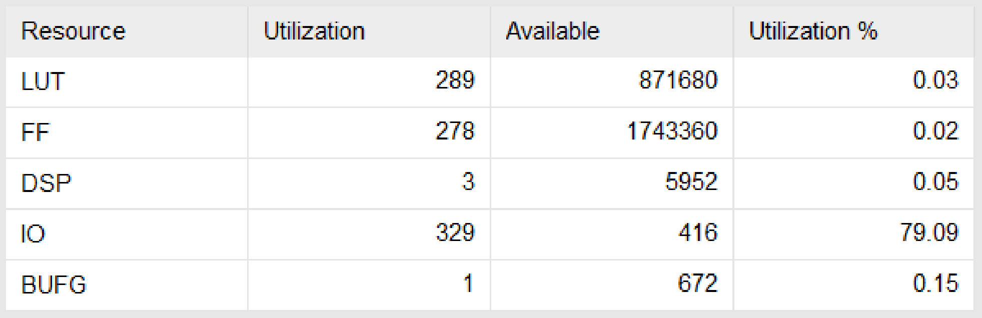
In this lab, we were to build up a FIR operation block that conduct a filtering with 11 coefficients. The configuring of the block are limited to axilite protocol and the raw and result data transmission are required to use AXI stream protocol. Additionally, both raw data and tap coefficients are required to be stored in srams. Data sram will function like a shift register. For the dataflow part, the multiple and add process in the convolution of filtering can have only one multiplier and one adder. The following are the operation done in my FIR IP:

First, the IP initialization when reset signal received. The IP will set the configuration to 32’h04, meaning that the IP is currently IDLE (ap_idle at bit 2). Once the outer system (simulated by testbench) detect that the IP is idle, it will start to configure it by sending tap coefficients and data length information to it using axilite protocol. The IP will decide to store the information to configuration register, data length register or tap coefficient sram according to the awaddr given by the outer system. Once the data length and the tap coefficient are all given, the outer system will again use axilite to overwrite the configuration state of the IP to 32’h01 to starting the IP’s operation.

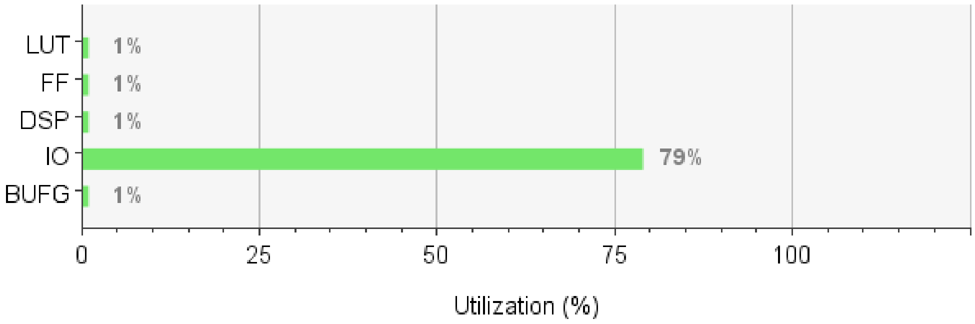
The next thing the IP do is to wait for the data to be sent in. According to the specification, ap_start value in the configuration need to be pulled down once the IP sees the first data coming in. So the IP will look at the ss_tvalid, the valid port in the AXI stream protocol to transmit raw data, to see if the first data is presented and pull down ap_start when detect the first data.

The third stage the IP enters is the computation stage. At the stage, the IP will first receive the data sent in by raising ss_tready. The data will be stored in the register and wait for the shift sram to finish shifting and emptying a space for storage. To control the tap sram and data sram, I use one common counter to generate the address for the two in that (1) only one multiplication and one accumulation can be done at one time due to the limitation of the multiplier and adder and (2) the tap coefficient used is correlated to the position of data in the shift register. This way, the tap coefficient and the raw data in the sram can be obtained simultaneously and compute the product to add to the partial sum of the final result. Also, after the data is extracted from the shift register and finish its computation, it will be written back to the next space of the shift register for the later use. Once all the previous data in the shift register have completed shifting, the received data from the outer system will then doing the multiplication with the tap coefficient and then write to the first place of the shift register. Notice that the IP will reset the data sram when the first data comes in by setting the write back data the data value used in the multiplier equal to 0. This way, we can make sure that the first and the later result is correct and not affected by the leftover data in the sram. Once the result is computed by adding up all the partial sum, the sm_tvalid will be raised and the IP will wait for the outer system to receive that data. After that, the IP will reset the accumulator, collect the data from the outer system and restart the computation process all over again. This is until the ss_tlast signal is detected. This means that the data collected is the last raw data. After the current output result is finish sending, the IP will check if all the data have been sent in, i.e. the processed data is equal to the data length. If not, the IP will stay at the same state to wait for another data to come. If it is, the IP will go for 10 more computation and transmission process for the last 10 output data. Once the last 10 outputs are produced, the sm_tlast signal will be raised and after the last output is transmitted, the IP will raise ap_idle and ap_done in the configuration register and go back to the IDLE state.

## 3. Resource Usage

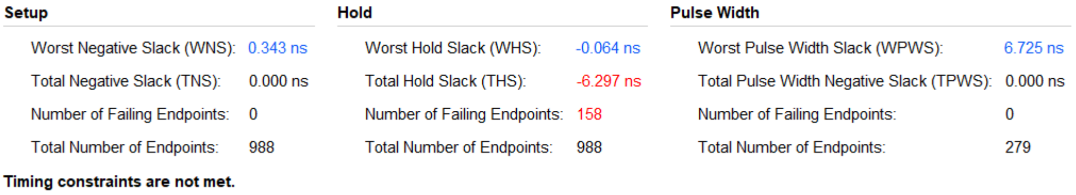


| Resource | Utilization | Available | Utilization % |
|---|---|---|---|
| LUT | 289 | 871680 | 0.03 |
| FF | 278 | 1743360 | 0.02 |
| DSP | 3 | 5952 | 0.05 |
| IO | 329 | 416 | 79.09 |
| BUFG | 1 | 672 | 0.15 |



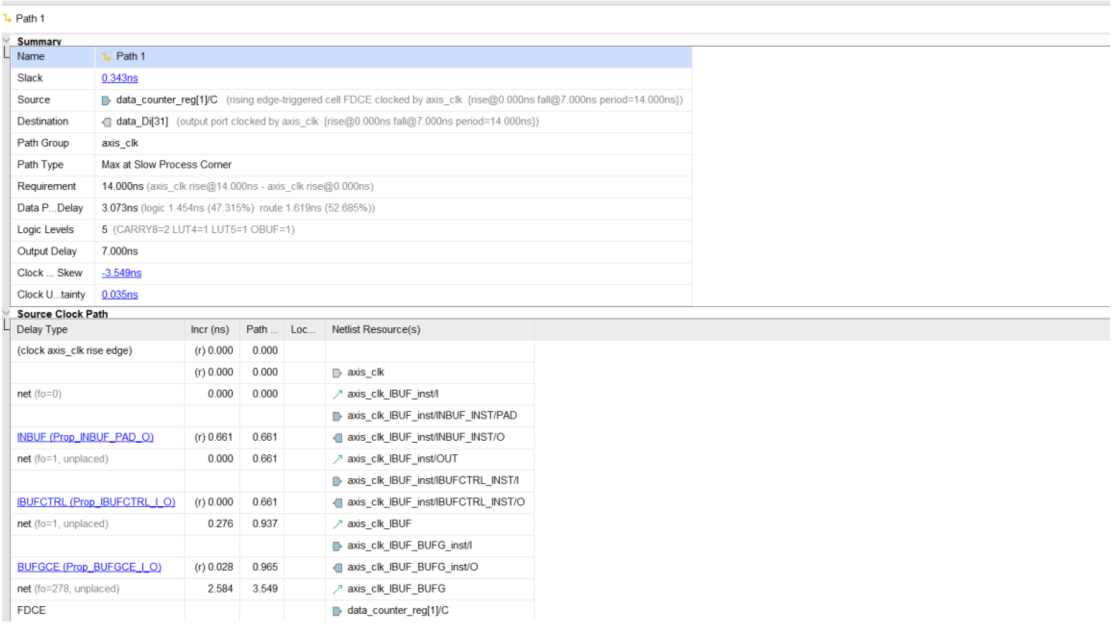
Board using Alveo U50 Data Center Accelerator Card

## 4. Timing report



| Setup | | Hold | | Pulse Width | |
|---|---|---|---|---|---|
| Worst Negative Slack (WNS): | 0.343 ns | Worst Hold Slack (WHS): | -0.064 ns | Worst Pulse Width Slack (WPWS): | 6.725 ns |
| Total Negative Slack (TNS): | 0.000 ns | Total Hold Slack (THS): | -6.297 ns | Total Pulse Width Negative Slack (TPWS): | 0.000 ns |
| Number of Failing Endpoints: | 0 | Number of Failing Endpoints: | 158 | Number of Failing Endpoints: | 0 |
| Total Number of Endpoints: | 988 | Total Number of Endpoints: | 988 | Total Number of Endpoints: | 279 |

**Timing constraints are not met.**



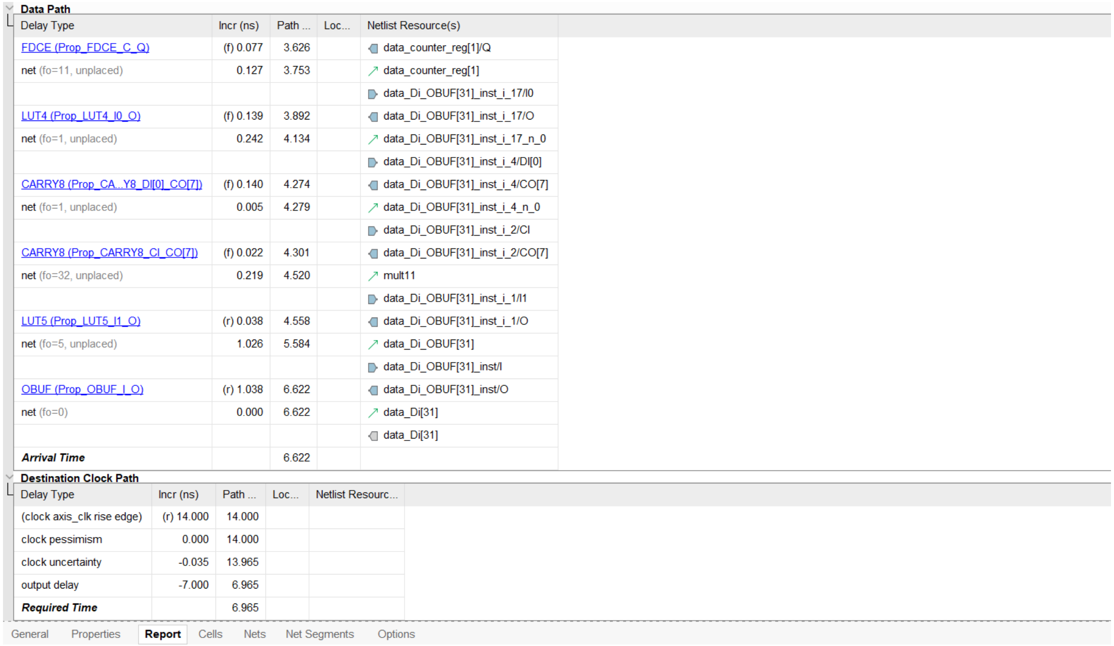
Path 1

**Summary**

| Name | Path 1 |
|---|---|
| Slack | 0.343ns |
| Source | data_counter_reg[1]/C (rising edge-triggered cell FDCE clocked by axis_clk {rise@0.000ns fall@7.000ns period=14.000ns}) |
| Destination | data_Di[31] (output port clocked by axis_clk {rise@0.000ns fall@7.000ns period=14.000ns}) |
| Path Group | axis_clk |
| Path Type | Max at Slow Process Corner |
| Requirement | 14.000ns (axis_clk rise@14.000ns - axis_clk rise@0.000ns) |
| Data P...Delay | 3.073ns (logic 1.454ns (47.315%) route 1.619ns (52.685%)) |
| Logic Levels | 5 (CARRY8=2 LUT4=1 LUT5=1 OBUF=1) |
| Output Delay | 7.000ns |
| Clock ... Skew | -3.549ns |
| Clock U...tainty | 0.035ns |

**Source Clock Path**

| Delay Type | Incr (ns) | Path ... | Loc... | Netlist Resource(s) |
|---|---|---|---|---|
| (clock axis_clk rise edge) | (r) 0.000 | 0.000 | | |
| | (r) 0.000 | 0.000 | | axis_clk |
| net (fo=0) | 0.000 | 0.000 | | axis_clk_IBUF_inst/I |
| | | | | axis_clk_IBUF_inst/INBUF_INST/PAD |
| INBUF (Prop_INBUF_PAD_O) | (r) 0.661 | 0.661 | | axis_clk_IBUF_inst/INBUF_INST/O |
| net (fo=1, unplaced) | 0.000 | 0.661 | | axis_clk_IBUF_inst/OUT |
| | | | | axis_clk_IBUF_inst/IBUFCTRL_INST/I |
| IBUFCTRL (Prop_IBUFCTRL_I_O) | (r) 0.000 | 0.661 | | axis_clk_IBUF_inst/IBUFCTRL_INST/O |
| net (fo=1, unplaced) | 0.276 | 0.937 | | axis_clk_IBUF |
| | | | | axis_clk_IBUF_BUFG_inst/I |
| BUFGCE (Prop_BUFGCE_I_O) | (r) 0.028 | 0.965 | | axis_clk_IBUF_BUFG_inst/O |
| net (fo=278, unplaced) | 2.584 | 3.549 | | axis_clk_IBUF_BUFG |
| FDCE | | | | data_counter_reg[1]/C |



Data Path

| Delay Type | Incr (ns) | Path ... | Loc... | Netlist Resource(s) |
|---|---|---|---|---|
| FDCE (Prop_FDCE_C_Q) | (f) 0.077 | 3.626 | | data_counter_reg[1]/Q |
| net (fo=11, unplaced) | 0.127 | 3.753 | | data_counter_reg[1] |
| | | | | data_Di_OBUF[31]_inst_i_17/I0 |
| LUT4 (Prop_LUT4_I0_O) | (f) 0.139 | 3.892 | | data_Di_OBUF[31]_inst_i_17/O |
| net (fo=1, unplaced) | 0.242 | 4.134 | | data_Di_OBUF[31]_inst_i_17_n_0 |
| | | | | data_Di_OBUF[31]_inst_i_4/DI[0] |
| CARRY8 (Prop_CA...Y8_DI[0]_CO[7]) | (f) 0.140 | 4.274 | | data_Di_OBUF[31]_inst_i_4/CO[7] |
| net (fo=1, unplaced) | 0.005 | 4.279 | | data_Di_OBUF[31]_inst_i_4_n_0 |
| | | | | data_Di_OBUF[31]_inst_i_2/CI |
| CARRY8 (Prop_CARRY8_CI_CO[7]) | (f) 0.022 | 4.301 | | data_Di_OBUF[31]_inst_i_2/CO[7] |
| net (fo=32, unplaced) | 0.219 | 4.520 | | mult11 |
| | | | | data_Di_OBUF[31]_inst_i_1/I1 |
| LUT5 (Prop_LUT5_I1_O) | (r) 0.038 | 4.558 | | data_Di_OBUF[31]_inst_i_1/O |
| net (fo=5, unplaced) | 1.026 | 5.584 | | data_Di_OBUF[31] |
| | | | | data_Di_OBUF[31]_inst/I |
| OBUF (Prop_OBUF_I_O) | (r) 1.038 | 6.622 | | data_Di_OBUF[31]_inst/O |
| net (fo=0) | 0.000 | 6.622 | | data_Di[31] |
| | | | | data_Di[31] |
| *Arrival Time* | | 6.622 | | |

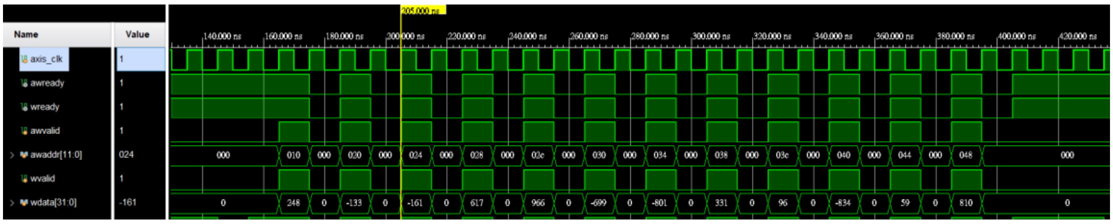
Destination Clock Path

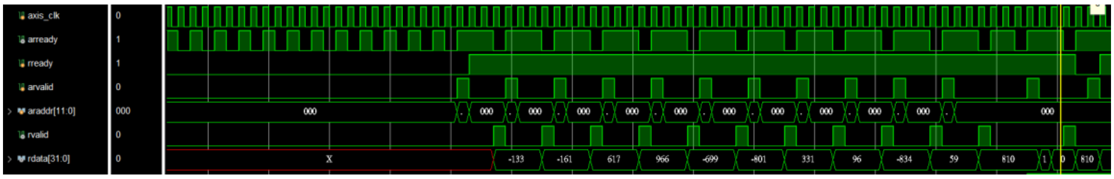
| Delay Type | Incr (ns) | Path ... | Loc... | Netlist Resourc... |
|---|---|---|---|---|
| (clock axis_clk rise edge) | (r) 14.000 | 14.000 | | |
| clock pessimism | 0.000 | 14.000 | | |
| clock uncertainty | -0.035 | 13.965 | | |
| output delay | -7.000 | 6.965 | | |
| *Required Time* | | 6.965 | | |

(max delay path)

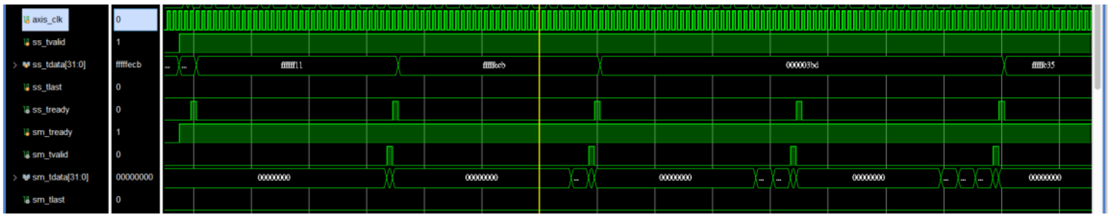
## 5. Simulation waveform

- Coefficient program, and read back

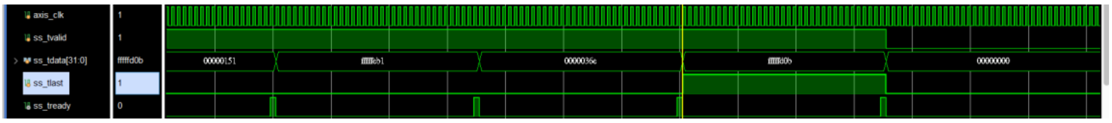




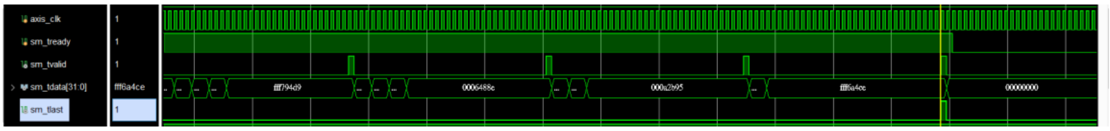
- Data-in stream-in & Data-out stream-out



Last-In:

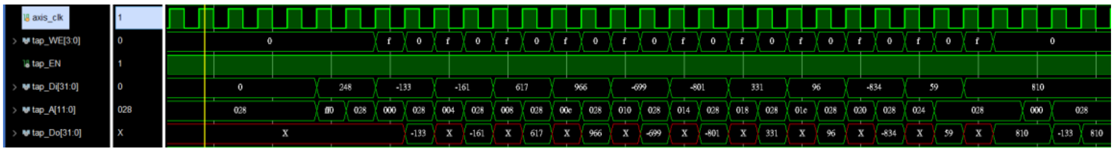


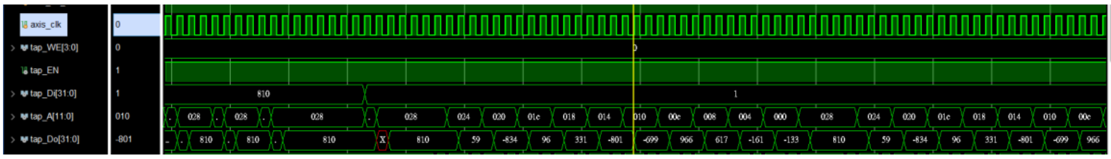
Last-Out:



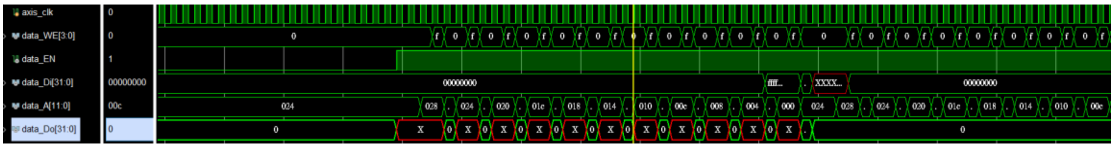
- RAM access control

Tap ram:



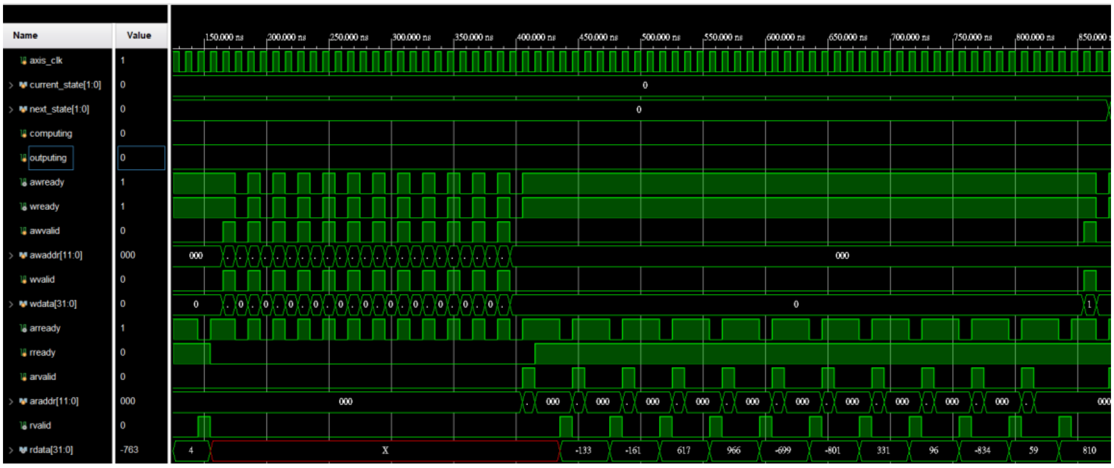


Data ram:

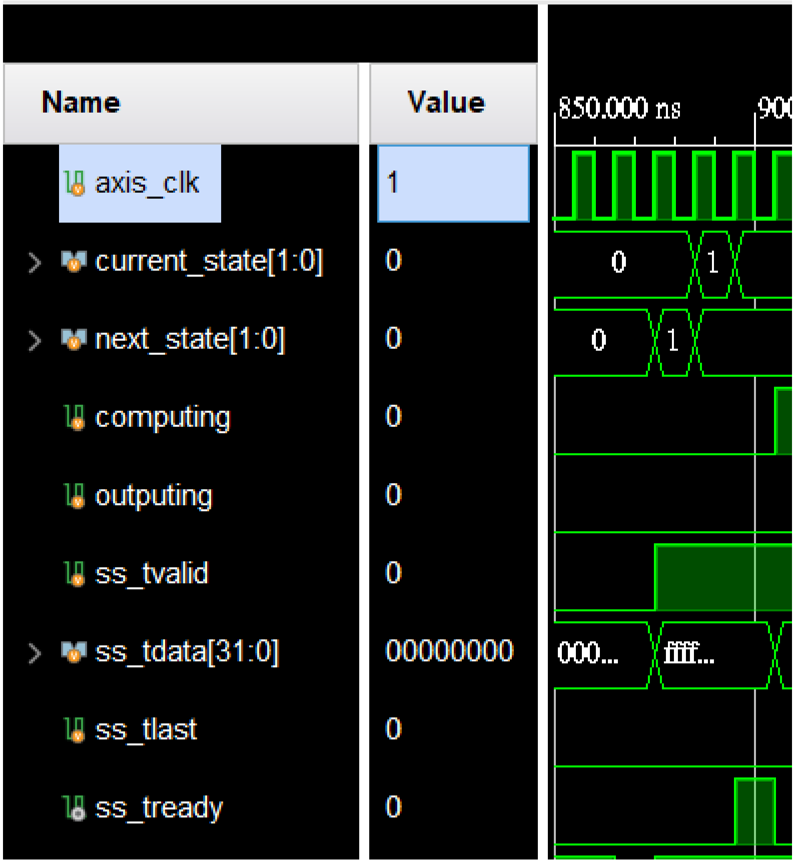


- FSM

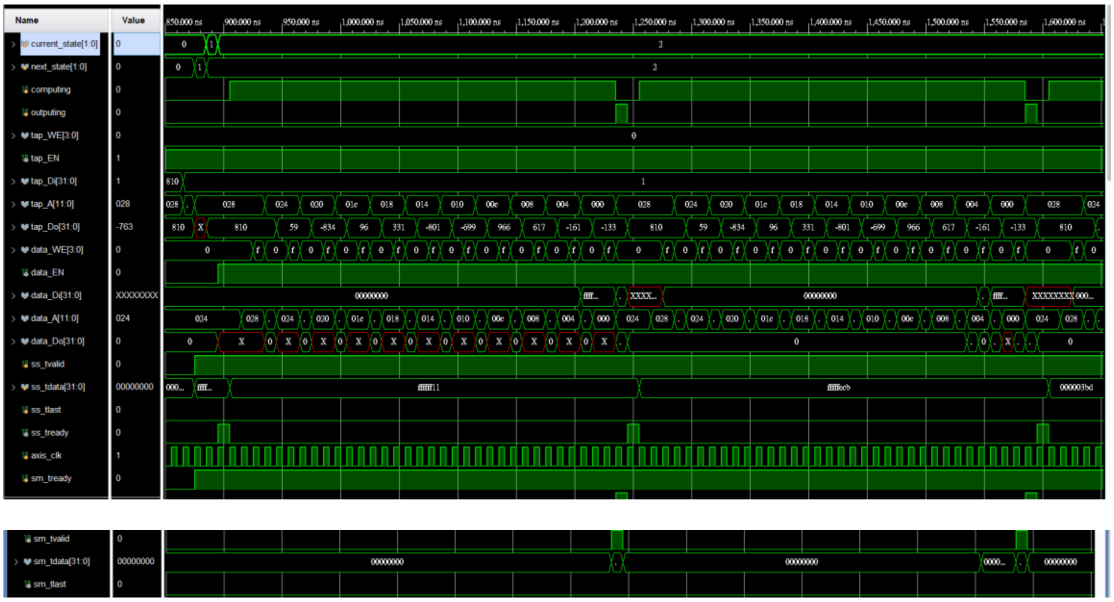
IDLE state to wait for configuration:



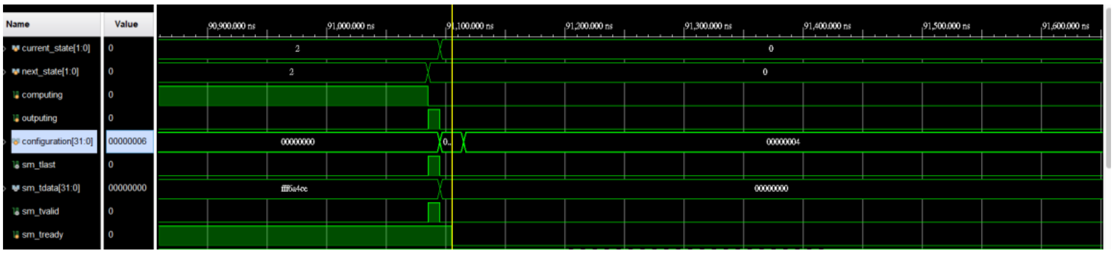
WAIT_FOR_DATA state to wait for the first data:



COMPUTE state for doing FIR process:



Back to IDLE when last output is sent:



| Name | Value |
|---|---|
| current_state[1:0] | 0 |
| next_state[1:0] | 0 |
| computing | 0 |
| outputing | 0 |
| configuration[31:0] | 00000006 |
| sm_tlast | 0 |
| sm_tdata[31:0] | 00000000 |
| sm_tvalid | 0 |
| sm_tready | 0 |