V&V Users Stories : Bremen University, DLR, Siemens

System Integration Testing with Model Based Testing

Cécile Braunstein Jan Peleska

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Abstract

This document presents the experiments (to be) conducted by Uni Bremen, DLR and Siemens for the system integration testing of parts of the OBU. The method details may be found in the WP4 Verification and Validation Plan. This document summarize the task to achieve and the state of this task.

1 Document and folder description

01-Requirements

- WP4-Validation and Verification plan : Contains the methods definition and the details of our task
- SysML Management of Radio Communication model : SysML model of the MoRC in xml format generated from an Enterprise architect description
- SysML Management of Radio Communication doc : Explanation of the SysML model, contains also the interface definition of the MoRC.

2 Task Resume

The detail of the task may be found in the Verification and Validation plan.

Uni Bremen will provide two SysML test model that represent the Management of the radio communication and the ceiling speed monitoring of the OBU. These models will be used to automatically generate test cases with the RT-tester tool. The tests will be used for system integration testing. Our goal is to have an test environment within the DLR laboratory for Hardware in the loop test and also use the same generated test cases to perform software int the loop testing with the generated code from SCADE. To show the strength of our tests, the test suites automatically generated will be analyzed according to the well known coverage measure. Moreover we will compare our test to those defined in the SUBSET-76.

3 Status of the task

3.1 Providing Test environment

Activity	Status	Remarks
Create a test model in SysML MoRC	Done	From the model evaluation of WP7
Provide the test model for the ceiling speed monitoring	To be commited	Still some cleaning to do
Generate test cases according to the defined interface given by DLR. (RT-Tester)	Active	DLR confirm interface
Provide simulation environment for the track-to-train simulation along routes used for testing	Active	
Study the automatic generation of these track layouts and speed simulations		
Set up a test environments for Hardware-in-the-loop Testing within DLR laboratory		
Set up a test environments for Software-in-loop testing with code provided by SCADE (Siemens)		

3.2 Test cases generation

Together with generated the test cases we will study the quality of the test suites.

Activity	Status	Remarks
Check the test model (SysML) RTT-BMC		
Add relevant LTL properties	Active	
Structural coverage analysis	Done	Automatically performs by RT-Tester
Requirement coverage analysis		
Mutation coverage analysis		
Provide techniques and Howto describing how test cases from Subset 76 can be executed in the RT-Tester environment		
Compare new test cases created by RT-Tester to new test cases for ceiling speed monitoring provided by ERTMS standardization group		

3.3 Exchange Formats

Test models represented in XMI/Ecore are used as SysML test modeling standard. RT-Tester model parsers are extended to cope with this format.

Activity	Status	Remarks
Test procedures general abstract syntax definition	Active	
Test results (test execution logs) general format		