



# Verification and Validation in openETCS: Conclusions & Discussion

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Halfterm Project Review

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Marc Behrens, Hardi Hungar

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Munich, 14.01.2014

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# WP 4 Review Schedule

- 17:00 - 17:20 Introduction and Overview of the first VnV Level (Marc Behrens und Hardi Hungar, DLR)
- 17:20 - 17:50 Results Model V&V (Ana Cavalli, Institute Telecom)  
[Video contribution]
  - 17:50 - 18:00 Coffee Break
- 18:00 - 18:10 Results Implementation / Code V&V (Jens Gerlach, Fraunhofer FOKUS)
- 18:10 - 18:30 Process and Safety (Jan Welte, TU BS)
- 18:30 - 18:40 Internal Assessment and Preparation of Workshop in Nuernberg (Hardi Hungar, DLR)
- **18:40 - 19:15 Overall Conclusions & Discussion of Upcomming V&V activities (Marc Behrens & Hardi Hungar, DLR)**

## Challenges

### Formalization of

- Test Model
- Test Architecture
- Interface Definition

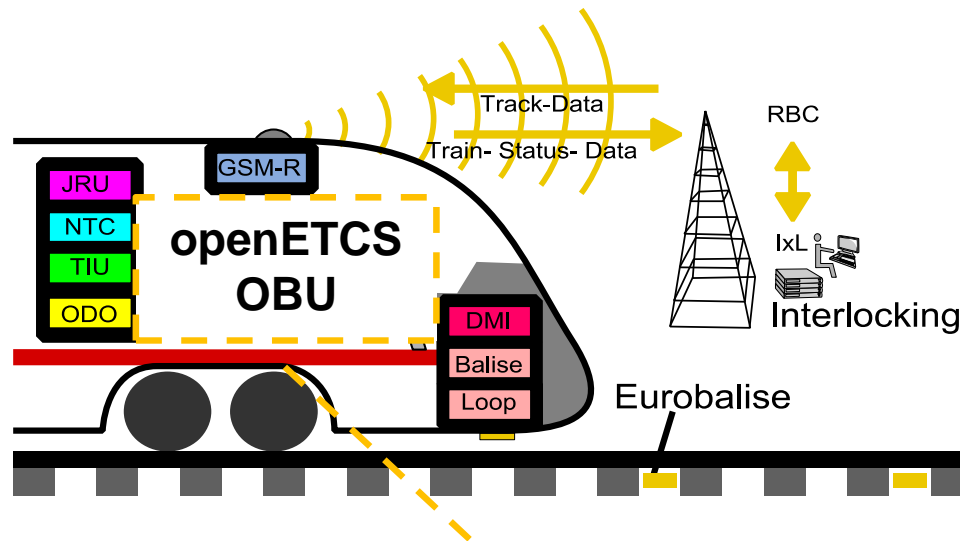
### Collaboration within the WP4

### Outlook

### 2nd level VnV

- Steps in Verification
- Steps in Validation
- Executing tests

# Challenges within complete system:

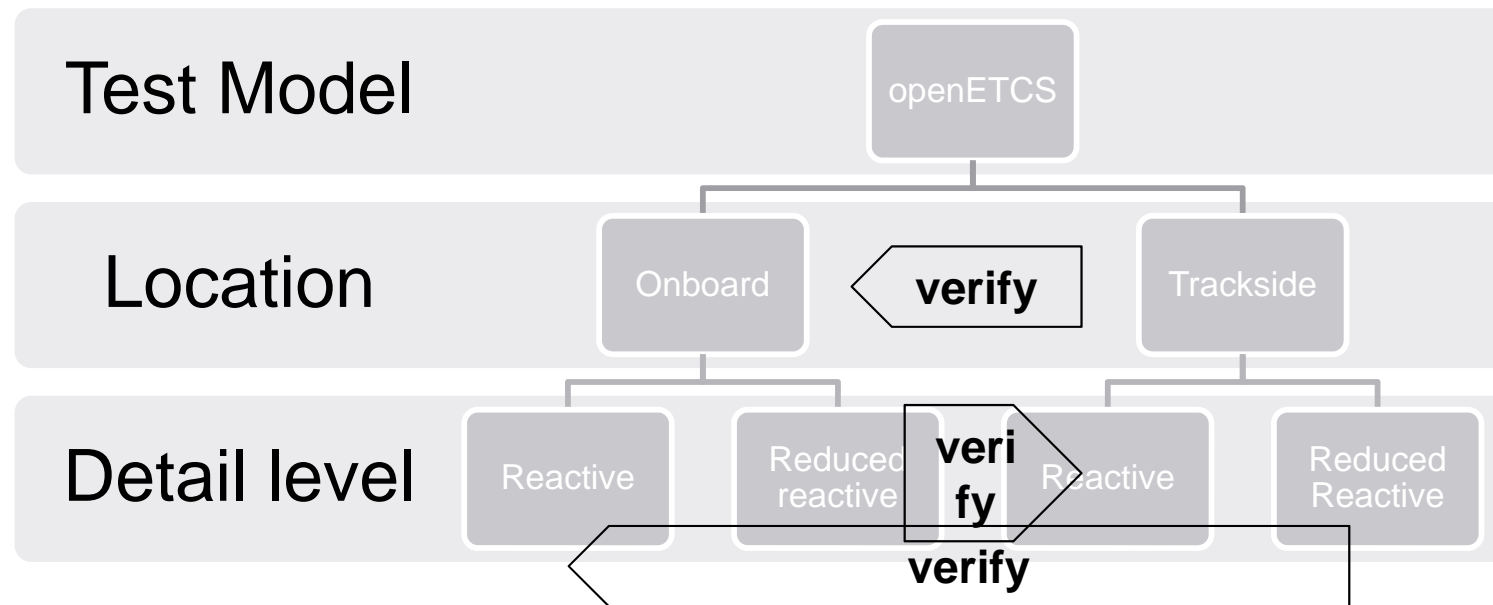


- Creating a formal specification of the ETCS OBU functionality  
→ Subset 026
- Software generated from the formal specification for purpose:
  - laboratory test
  - simulation
  - reference purposes

**System under Test (SuT)**

# Challenges within complete system:

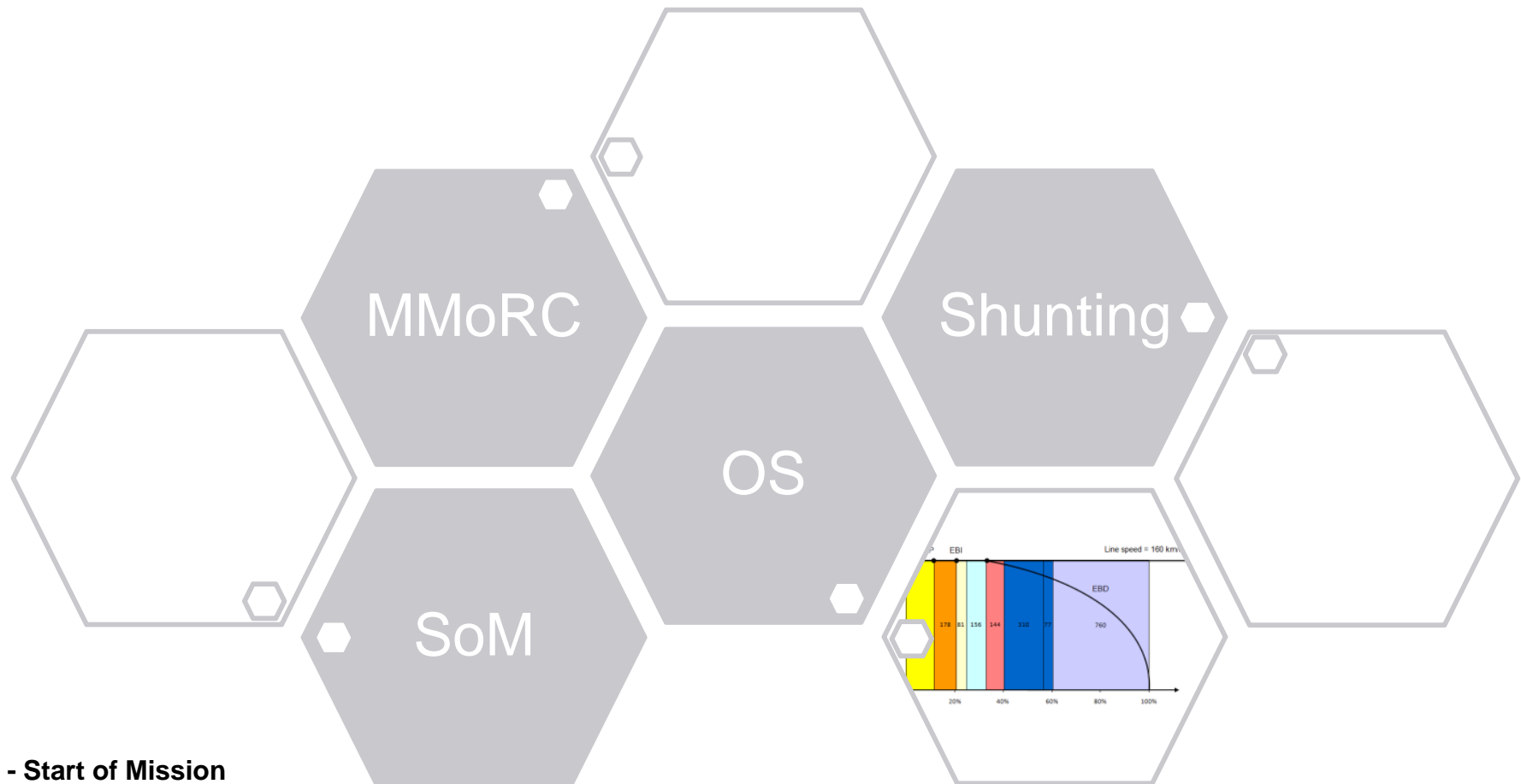
## Reduced Reactive Testmodel



**Reduced Reactive Testmodel used to verify the testmodel**

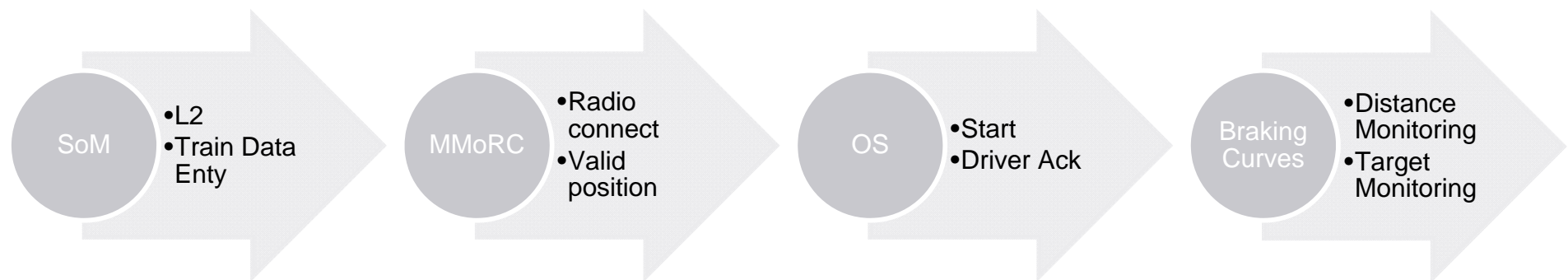
**HiL structure is applied to apply reduced reactive test model**

# Test Model Decomposition: 1<sup>st</sup> level VnV

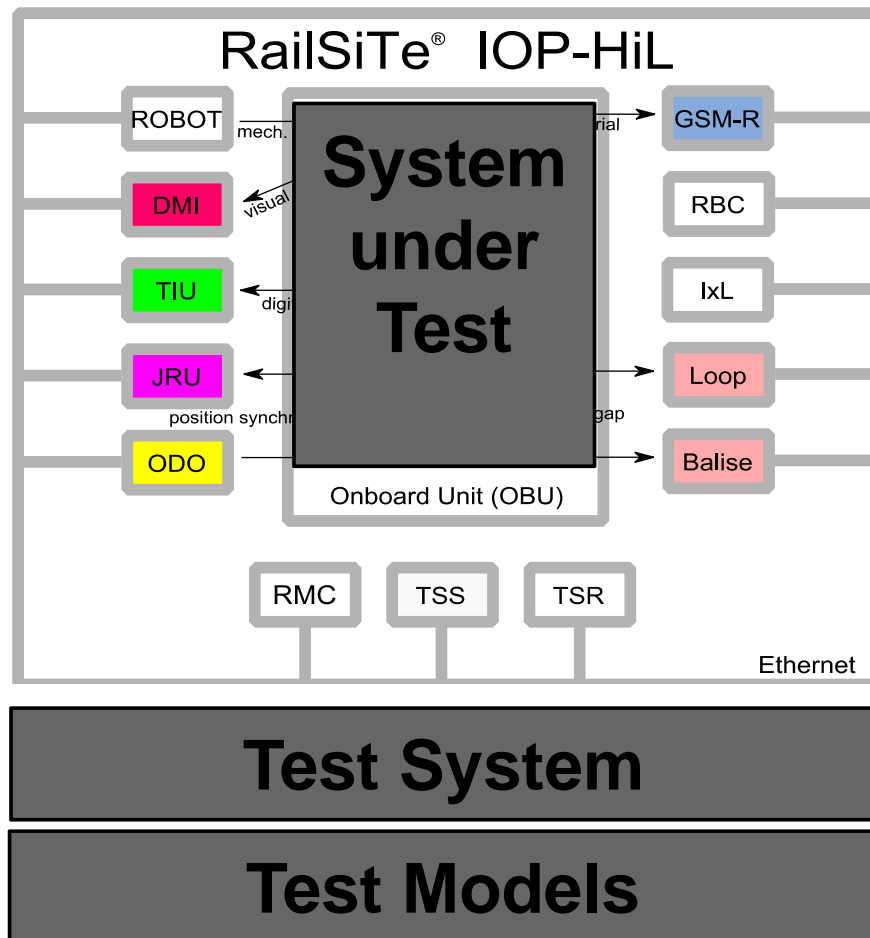


**SoM** - Start of Mission  
**MMoRC** - Managment of Radio Communication  
**OS** - Procedure OnSight

# First scenario merging the current testmodel



# Test Architecture Integration



- **Model Based - Extension of our Railway Simulation and Testing Environment (RailSiTe<sup>®</sup>)**
- **Develop generic tests enabling testing for operational scenarios and harmonizing validation through model verification**

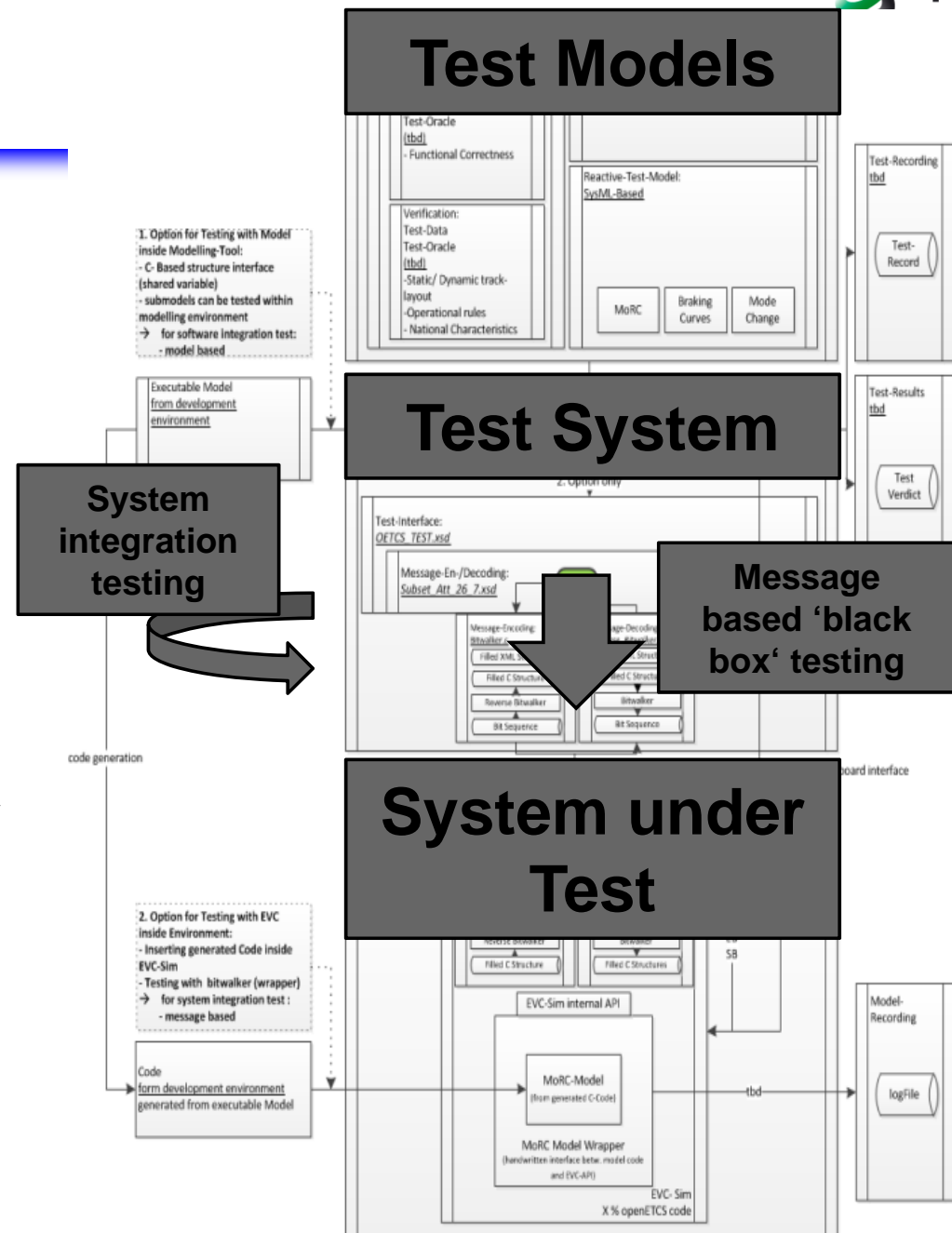


# Test Architecture

Model based definition  
of interfaces according to  
e.g. SUBSET-094

Human readable formats:  
SysML, XMI, XML, ...

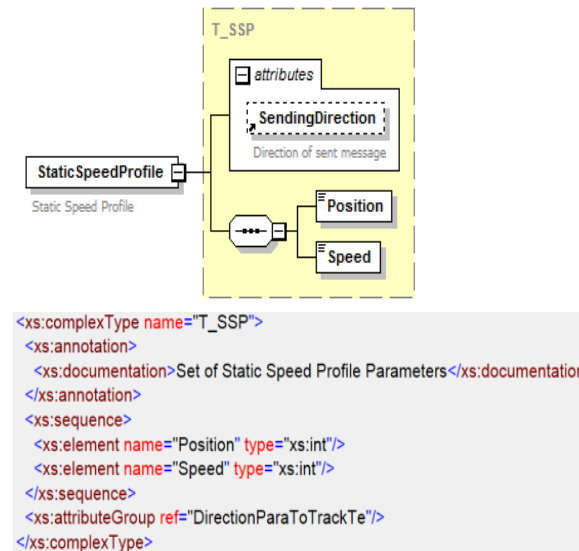
Synchronized Datadictionary  
modularized  
system integration test



# Model based interface definition

## Formalizing testing relevant Subsets of the TSI in

- Type definition
- Variable definition
- Human readable source



Documentation can be found on github:

<https://github.com/openETCS/validation/tree/master/VnVUserStories/VnVUserStoryDLR/05-Work/InterfaceSchema/Documentation>

## Verification results to the design model

### Specification questions:

- Where is the Subset-026 not clear enough to be consistently formalized comparing design-model to test-model?
- Specification questions to be synchronized with operational rules of validation scenarios

# Organization of the VnV Process: 2<sup>nd</sup> level VnV

## Process:

- Weekly Wednesday meeting from 11h00 to 12h30
- Sprints last 4 weeks
- **Contribution outside of the deliverables are collected inside user stories which then become part of the next deliverable.**

# Objectives of 2<sup>nd</sup> level VnV Process

## Objectives:

- Establish usable method and tool combination
- Perform complete verification of specification, model and code fragments
- Evaluate further method and tools to improve V&V
- **Define the quality gate for artifacts?**
  - E.g. Definition of Acceptance Criteria for each type of Objects for Verification:
    - *Specification*
    - *Model*
    - *Code*

# Test- Modelling

- # Lab-Testing

## Safety/ Assessment

## Requirements verification

# Validation

## How to enhance collaboration/ extend core knowledge?



## Upcoming activities:

- **Finishing the Deliverable 1st VnV Report D4.2**
- **Refining the VnV plan D4.1 anticipating the outcome of D4.2**
- **Integrating tools into testlab environment**
- **Starting Validation**
- **Setting up a common test model merging the different approaches.**
- **Processing the findings of the first internal assessment**
- **Supporting the modelling task with solid verification**
- **Identification of key partners for the topic**
  - *Strengthen collaboration between key partners*

## **Gain certainty on test models**

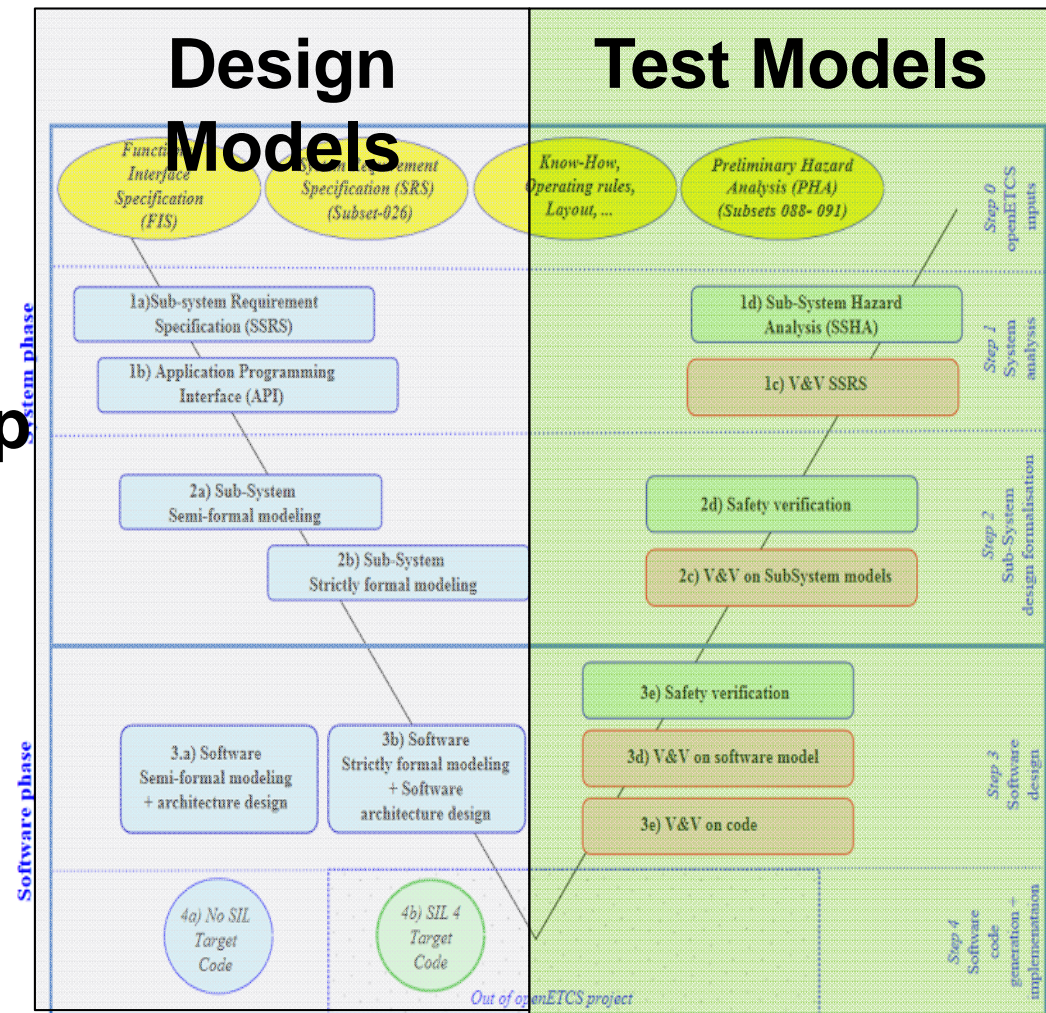
- **Testing: Develop operational reduced reactive test- model of the trackside**
- **Verify operational reduced reactive test- model of the trackside**
- **Verify with operational reduced reactive test- model of the onboard**
- **Develop functional operational counterpart to the reduced reactive test- model → Test Model (WP4)**



# Outlook: Early verification

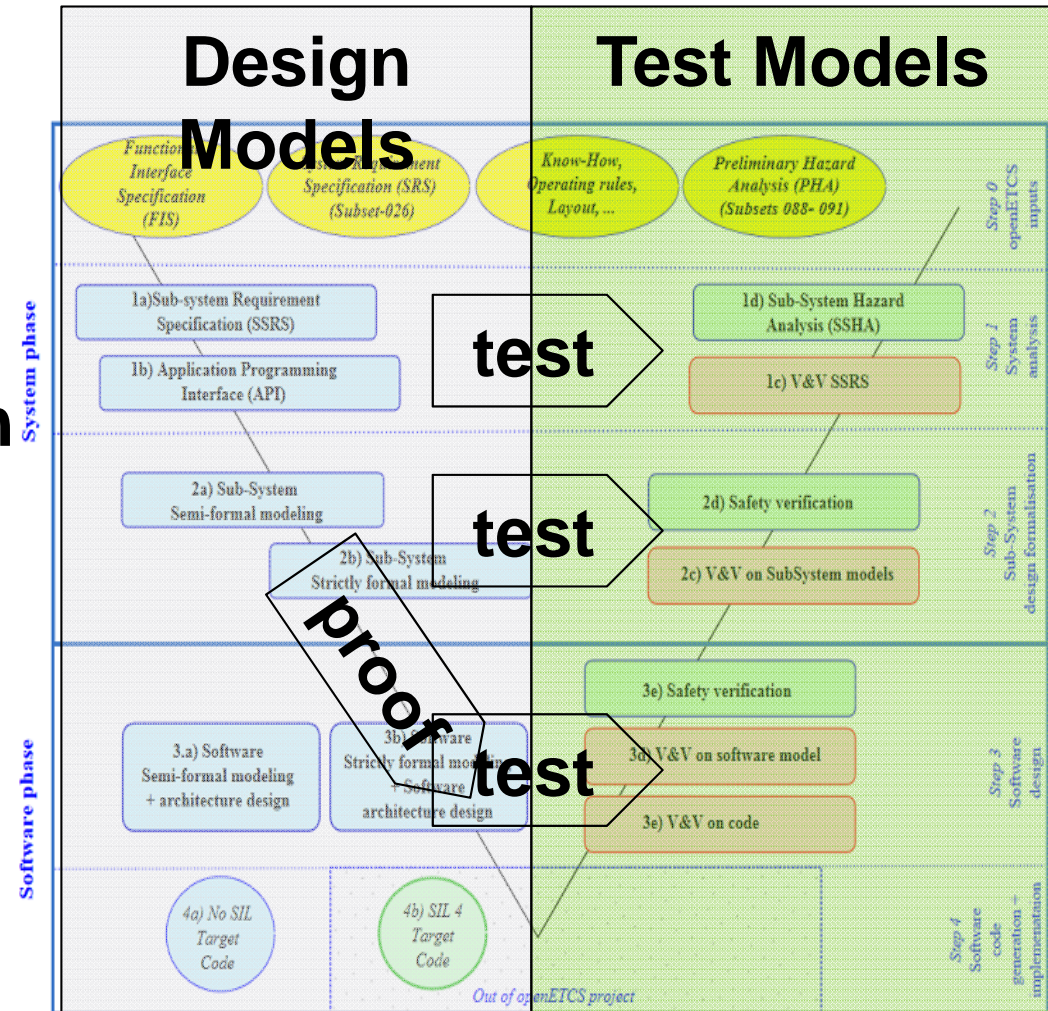
## System under Test:

- Subset-26 design model
- Test model is build up in parallel to the design model
- No hardware specification



# Outlook: Verification Concepts

- Test each level of design
- Proof of transformation can shift tests to a higher model level
- Does the V- Model become a Y – Model on which aspects?



# Outlook: Steps in **validation**

- Define validation properties/ scenarios
  - Develop scenario-data to model transformation
  - Transform scenario-data to model
  - Building the first track for openETCS as input data for validation
  - Validate model-based scenarios
- 
- Who is interested to join the validation activity?



# Outlook: Executing Tests



- Using tests generated from openETCS testmodel
- Verdict to be generated from testmodel
- Verifying the tests by verification of testmodel and applying reduce reactive model
- Physical testing Hardware, when baseline 3 hardware is provided (e.g. by General Electric).

**Thank you for your attention!**

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