Written test on 12^{th} of December 2018

Course: Computer Architecture and Engineering Course no. 02155

Exam time: 2 hours

No aids – Allowed: pocket calculator

Weighting: Each of the 5 problems counts 20%. All questions in a problem are weighted equally.

Answers are evaluated based on correctness, completeness and conciseness (i.e., answers must be correct, show how the result is obtained, and contain only the necessary text).
If some specification is missing, just state your own specification and continue the problem according to your stated specification.

Problem 1

Answer the following questions.

Question 1.1

Why does RISC-V have a signed and an unsigned version of load byte, but only one version for store byte?

Question 1.2

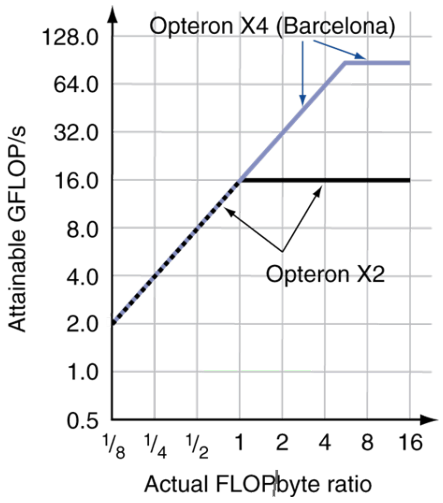
When does a page fault occur?

Question 1.3

What is the use of the Translation Look-aside Buffer (TLB)?

Question 1.4

In this "roofline" diagram for two Opteron processors X2 and X4, explain what happens for X2 and X4 when running a kernel with arithmetic intensity 2.0.
What modifications can be done to improve the performance of X4?



Problem 2

Consider the following RISC-V processors:

P1: 5-stage pipelined processor (stages: F, D, E, M, W) without data-forwarding, with $f_{clock} = 1\ GHz$. Branches are assumed not-taken and the decision on taking the branch is made at the end of stage D.

P2: as **P1**, but with data-forwarding implemented and branch prediction hardware (placed in stage F).

The processors are used to execute the following fragment of RISC-V code. At the time of execution, the value in register `x20`=16 (decimal), and the branch has been already taken several times.

```
0x01010    loop:  ld    x31, 0(x20)
0x01014           addi  x20, x20, -8
0x01018           add   x31, x31, x21
0x0101C           sd    x31, 8(x20)
0x01020           bne   x20, x0, loop
0x01024           sub   x23, x23, x24
0x01028           xor   ....
```

Question 2.1

a) Show the timing diagram[1] (instructions executed in each clock cycle) for the execution on processor **P1** of the above fragment of RISC-V code. Stop when you fetch instruction `xor ....`

b) Compute the corresponding execution time for **P1**.

Question 2.2

Sketch in a simple drawing how the branch prediction hardware could be implemented, and explain its main operations.

Question 2.3

a) Show the timing diagram for the execution on processor **P2** of the above fragment of RISC-V code. Stop when you fetch instruction `xor ....`

b) Compute the corresponding execution time for **P2**.

[1] For the timing diagram you should use the following compact representation, for example:

```
                1 2 3 4 5 6 7 ...
addi x2, x0, 5  F D E M W
lw x1, 0(x3)      F D E M W
...                 ...
```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Problem 3

Average times for reading and writing to a storage devices are common measurements used to compare devices. Calculate values related to read and write time for the disk with following characteristics:

- 11 ms average seek time
- 7200 RPM rotation speed
- 34 MBytes/s disk transfer rate
- 480 MBits/s controller transfer rate

Calculate following values and answer the following question:

Question 3.1
Calculate the average time to read or write a 1024-byte sector.

Question 3.2
Calculate the average time to read or write a 2048-byte sector.

Question 3.3
Determine the dominant factor for the performance. If you could make improvement to any aspect of the disc, what would you choose? If there is no dominant factor, explain why.

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Problem 4

Consider the following caches. For all, assume 2KB size, 32-bit addresses, 32-bit words, and byte addressing:

C1: direct mapped with 2 word blocks.

C2: direct mapped with 4 word blocks.

C3: 2-way set associative with 2 word blocks and LRU replacement.

For each cache:

Question 4.1
Show how binary addresses are divided into tag, index, block offset, and byte offset.

Question 4.2
Calculate the total number of bits required for the caches.

Question 4.3
For each memory access below, state whether the access is a hit or miss. The abbreviations are: Index (Idx), Offset (Off), and Hit or Miss (H/M).

	C1				**C2**				**C3**			
Address	Tag	Idx	Off	H/M	Tag	Idx	Off	H/M	Tag	Idx	Off	H/M
0x000												
0x004												
0x008												
0x00C												
0x800												
0x008												
0x000												
0x800												

Question 4.4
Calculate the hit ratio.

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Problem 5

Consider a program executing 10^7 instructions with the following mix of operations:

floating-point ops.	lw, sw	branches	R-type
20%	30%	10%	40%

A processor P1 requires the following number of cycles:

floating-point ops.	lw, sw	branches	R-type
12	5	3	4

Question 5.1
Determine the CPI for the benchmark program.

Question 5.2
For a clock rate of 3 GHz, what is the CPU execution time?

Additional information about the cache.

Instruction miss rate is 5%. Data miss rate per cache access is 12%. Miss penalty for both data and instructions is 8 cycles.

Question 5.3
Determine the execution time including memory stalls.

End of the Exam