Wrap-up

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DTU 02155 Computer Architecture and Engineering

Assignment #3 Deliverables

For this assignment you will be working in groups of 1-2. You will not receive extra credits by doing all the work by yourself, so there is no benefit in working alone.

Similar to the other assignments, you have to hand in a report (in PDF) using the front page specified in assignment 1. The report should contain an introduction, a description of the design and implementaton of your simulator, and some discussion of your design.

In addition to the report, you should hand in your simulator source code that can be compiled and executed on Ubuntu. You only have to hand in one set of source code, i.e., not one for each stage in the tasks. These additional deliverables should be uploaded as a single zip file. Furthermore, you need to demonstrate your simulator to a TA.

Deadline for the report 4th December 2022 at 23:59 upload DTU Learn

Exam

The final exam has been scheduled for the

Thursday 8^{th} of December 2022

2 hours written exam
Time and Place check http://eksamensplan.dtu.dk

All Aids.

Digital Exam

- Use your own laptop
- Train on how to answer questions by using a text editor
- Select some simple drawing tool if you need to show some diagram/drawing

Questions

?

Review of Exam Problems

Problems

- Pipeline and Hazards
- Cache
- Roofline Diagram

RISC-V Datapath and Control

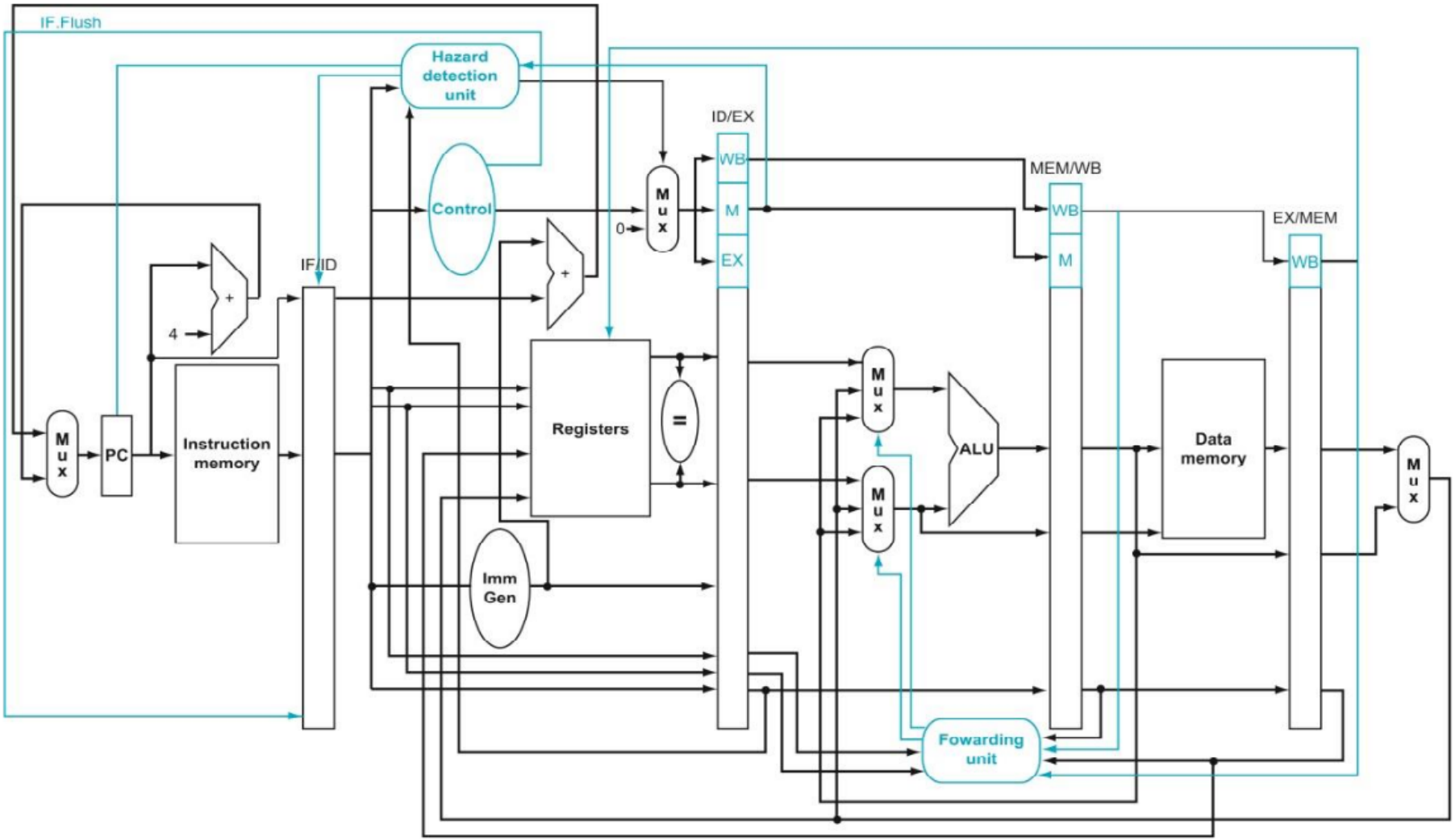

Figure 4.66 The final datapath and control for this chapter.

Pipeline and Hazards

In the following fragment of RISC-V code, the loop is executed N times.

```
loop: lw   x3, 0(x2)
      and  x7, x3, x5
      slt  x1, x6, x3
      addi x2, x2, -4
      bne  x2, x0, loop
```

a) Write the time diagram of one iteration of the loop for a pipelined processor with the following characteristics:

- 5 pipeline stages (IF, ID, EX, MEM, WB).
- Branches are resolved in ID stage.
- The processor stalls on hazards.

Pipeline and Hazards (cont.)

Solution a)

```
                      1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9
lw   x3, 0(x2)        F D E M W
and  x7, x3, x5         F - - D E M W
slt  x1, x6, x3               F D E M W
addi x2, x2, -4                 F D E M W
bne  x2, x0, loop                 F - - D E M W
(following instr.)                        F  <---   FLUSHED
-------------------------------------------------------------
lw   x3, 0(x2)                              F D E M W
```

The number of clock cycles required each loop is 10.

Pipeline and Hazards (cont.)

b) What is the execution time for the loop, if it is executed 100 times (i.e. $N = 100$) and the clock frequency is 1 GHz?

Solution b)

$$\text{Execution time} = (\text{n. clock cycles}) \times T_{clock} = 10 \cdot N \times 1\ ns = 1.0\ \mu s$$

Pipeline and Hazards (cont.)

c) Repeat assuming that hardware for forwarding is available.

Solution c)

We can forward

- the content of x3 from MEM/WB of `lw` to EX of `and` (stall 1 cycle)

The content of x2 cannot be forwarded from EX/MEM of `addi` to ID stage of `bne` in the datapath of Figure 4.66. Need to modify the hardware.

```
                      1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9
lw   x3, 0(x2)        F D E M W
and  x7, x3, x5         F - D E M W
slt  x1, x6, x3           - F D E M W
addi x2, x2, -4               F D E M W
bne  x2, x0, loop               F - - D E M W
(following instr.)                    F  <---   FLUSHED
-------------------------------------------------------------
lw   x3, 0(x2)                            F D E M W
```

$$\text{Execution time} = 9N \times 1\ ns = 900\ ns$$

Pipeline and Hazards (cont.)

d) Solution with forwarding extended to the ID stage.

Solution d)

- The content of x2 from EX/MEM of `addi` is forwarded to ID stage of `bne`.

```
                    1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9
lw   x3, 0(x2)      F D E M W
and  x7, x3, x5       F - D E M W
slt  x1, x6, x3         - F D E M W
addi x2, x2, -4             F D E M W
bne  x2, x0, loop             F - D E M W
(following instr.)                F  <---   FLUSHED
-------------------------------------------------------
lw   x3, 0(x2)                        F D E M W
```

$$\text{Execution time} = 8N \times 1\ ns = 800\ ns$$

Cache

Sequence of address references given as word addresses:

3 4 5 12 4 5 8 12 2 4 6 2 4 10 12

For a cache of size 8 words initially empty, label each reference in the list as a hit or a miss and show the final content of the cache for each of the following cache organizations:

a) direct-mapped cache

b) 2-way set-associative cache with FIFO replacement

c) 4-way set-associative cache with LRU replacement

Roofline Diagram

Benchmark two multicores using the roofline model

- Multicore M1 has a peak floating-point performance (peak-FP perf.) of 128 GFLOP/s from Arithmetic Intensity (AI) AI=8 FLOP/byte (and above).
  Its FP performance at AI=1/8 FLOP/byte is 2 GFLOP/s.
- Multicore M2 has a peak-FP performance of 16 GFLOP/s from AI=1/2 FLOP/byte (and above), and its performance at AI=1/8 FLOP/byte is 4 GFLOP/s.

1. Draw the roofline model for multicore M1.
2. Draw the roofline model for multicore M2.
3. Explain what happens when running a benchmark with AI=1 FLOP/byte on the two multicores.
   Which multicore does perform the best?

Roofline Diagram (Solution)