02155 - Computer architecture and Engineering
Fall 2022

Assignment 2

Group 31

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This report contains 4 pages

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A2.1

a)

P1

Instruction	1	2	3	4	5	6	7	8	9
addi a2, x0, 5	x								
lw a1, 0(a0)		x							
addi a1, a1, 5			x						
sw a1 , 0(a0)				x					
add a1 , x0 , a2					x				
beq a1 , x0 , branch1						x			
beq a1 , a2 , branch2							x		
addi a1 , a1 , 6								x	
addi a2 , a2 , 7									x

P2

Instruction	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
addi a2, x0, 5	F	D	E	M	W																
lw a1, 0(a0)		F	D	E	M	W															
addi a1, a1, 5			F	D	D	D	E	M	W												
sw a1 , 0(a0)				F	F	F	D	D	D	E	M	W									
add a1 , x0 , a2							F	F	F	D	E	M	W								
beq a1 , x0 , branch1										F	D	D	D	E	M	W					
beq a1 , a2 , branch2											F	F	F	D	E	M	W				
add a1 , a1 , a1														F	D						
add a2 , a2 , a2															F						
addi a1 , a1 , 6																F	D	E	M	W	
addi a2 , a2 , 7																	F	D	E	M	W

P3

Instruction	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
addi a2, x0, 5	F	D	E	M	W											
lw a1, 0(a0)		F	D	E	M	W										
addi a1, a1, 5			F	D	D	E	M	W								
sw a1 , 0(a0)				F	F	D	E	M	W							
add a1 , x0 , a2						F	D	E	M	W						
beq a1 , x0 , branch1							F	D	E	M	W					
beq a1 , a2 , branch2								F	D	E	M	W				
add a1 , a1 , a1									F	D						
add a2 , a2 , a2										F						
addi a1 , a1 , 6											F	D	E	M	W	
addi a2 , a2 , 7												F	D	E	M	W

b)

P1 requires 9 clock cycles, each taking 10 ns. $T_{P_1} = 9 \cdot 10ns = 90ns$

P2 required 21 clock cycles, each taking 2 ns. $T_{P_2} = 21 \cdot 2ns = 42ns$

P3 required 16 clock cycles, each taking 2 ns. $T_{P_3} = 16 \cdot 2ns = 32ns$

c)

Speedup of **P3** over **P1** is: $\frac{T_{P_1}}{T_{P_3}} = 2.8125$

Speedup of **P3** over **P2** is: $\frac{T_{P_2}}{T_{P_3}} = 1,3125$

A2.2

Total amount of cycles required of the program using double precision is given as: $C_{double} = 10^9$
Total amount of cycles spent on FP operations using double precision is:

$$C_{FP\text{-}double} = 10^9 \cdot 0.6 = 6 \cdot 10^8$$

Total amount of cycles spent on non-FP operations is:

$$C_R = 10^9 \cdot 0.4 = 4 \cdot 10^8$$

With single precision (binary32) and all FP operations being independent, 2 operations can always be executed in parallel, thus halving the required FP operations.

$$C_{FP\text{-}single} = \frac{C_{FP\text{-}double}}{2} = 3 \cdot 10^8$$

The total clock cycles required with single precision is:

$$C_{single} = C_{FP\text{-}single} + C_R = 7 \cdot 10^8$$

With half precision (binary16) and all FP operations being independent, 4 operations can be executed in parallel, thus quartering the required FP operations.

$$C_{FP\text{-}half} = \frac{C_{FP\text{-}double}}{4} = 1.5 \cdot 10^8$$

The total clock cycles required with single precision is:

$$C_{half} = C_{FP\text{-}half} + C_R = 5.5 \cdot 10^8$$

Execution time is found with the following equation:

$$\frac{\textbf{CPU Clock Cycles}}{\textbf{Clock rate}} = \textbf{CPU Time}$$

The execution times are:

$$T_{double} = \frac{C_{double}}{f} = \frac{10^9}{4GHz} = \frac{10^9}{4 \cdot 10^9 Hz} = 0.25s = 250ms$$

$$T_{single} = \frac{C_{single}}{f} = \frac{7 \cdot 10^8}{4GHz} = 175ms$$

$$T_{half} = \frac{C_{half}}{f} = \frac{5.5 \cdot 10^8}{4GHz} = 137.5ms$$

Speedup of **Single precision** over **Double precision** is: $\frac{T_{double}}{T_{single}} \approx 1.428$

Speedup of **Half precision** over **Double precision** is: $\frac{T_{double}}{T_{half}} \approx 1,818$

A2.3

A2.4