02155 - Assignment 2

Practical information

This second deliverable assignment consists of a collection of exam problems (one per page) from the previous years.

For this assignment you have to write a small report in English with detailed problem solutions (not only the results). The grade you will obtain for the report will be part of the final grade. Please hand in the assignment as group report.

The report should have a front page similar to the one used in Assignment 1. There are no other requirements on the template to be used for the report.

The report should be handed-in only in electronic format (PDF) using the Assignment utility in DTU Learn.

Feel free to ask or send an e-mail to the TA if you have questions regarding the practical information and the assignment in general.

Problems

Exercise A2.1 - Exam problem (2017)

Consider the following RISC-V processors:

P1: single cycle processor (each instruction is executed in one clock cycle) with $T_{clock} = 10\ ns$.

P2: 5-stage pipelined processor (stages: F, D, E, M, W) without data-forwarding, with $T_{clock} = 2\ ns$. Branches are assumed not-taken and the decision on taking the branch is made at the end of stage D.

P3: as **P2**, but with data-forwarding implemented.

The processors are used to execute the following fragment of RISC-V code.

```
main:
        addi a2, x0, 5
        lw a1, 0(a0)
        addi a1, a1, 5
        sw a1, 0(a0)
        add a1, x0, a2
        beq a1, x0, branch1
        beq a1, a2, branch2
branch1:
        add a1, a1, a1
        add a2, a2, a2
branch2:
        addi a1, a1, 6
        addi a2, a2, 7
```

a. For each processor, show the timing diagram[1] (instructions executed in each clock cycle) of the execution of the above fragment of RISC-V code.

b. For each processor, compute the execution time of the fragment of RISC-V code.

c. What is the speed-up of **P3** over **P1** and **P2**?

[1] For the timing diagram you should use the following compact representation, for example:

```
                1 2 3 4 5 6 7 ...
addi a2, x0, 5  F D E M W
lw a1, 0(a0)      F D E M W
...                 ...
```

Exercise A2.2 - Exam problem (2017)

A single core processor can operate at the following Voltage Scaling (VS) and Frequency Scaling (FS) modes:

		High-perf.	Medium	Low-power
frequency	(GHz)	4	3	2
supply V_{DD}	(V)	1.0	0.9	0.8

Its Floating-Point (FP) unit can issue per clock cycle:

- 1 double-precision (binary64) FP operation;
- 2 single-precision (binary32) FP operations in parallel;
- 4 half-prexision (binary16) FP operations in parallel.

For all three types of operations, the FP-unit latency is the same.

We run a C program on the processor and we want to determine its performance under the three types of FP operations (and operands).
Assume that

- the execution of the program requires 10^9 cycles when using binary64 FP operations;
- 60% of the cycles are spent FP operations;
- All FP operations are independent.

In the High-performance ($f = 4$ GHz, $V_{DD} = 1$ V) mode, determine the execution time for the three types of FP operations and the speed-ups with respect to the double-precision case.

Exercise A2.3 - Exam problem (2017)

Consider the following caches. For both, assume 4KB size, 32-bit addresses, and byte addressing:

C1: direct mapped with 8 word blocks and write-through policy.

C2: 4-way set associative with 4 word blocks, LRU replacement, and write-back policy.

For each cache:

a. Show how binary addresses are divided into tag, index, block offset, and byte offset.

b. Calculate the total number of bits required for the caches.

c. For each memory access below, state whether the access is a hit or miss:

	C1				**C2**			
Address	Tag	Index	Offset	Hit/Miss	Tag	Index	Offset	Hit/Miss
0x0022								
0x0023								
0x0034								
0x0420								
0x1420								
0x0422								
0x1430								

d. Calculate the hit ratio.

Exercise A2.4 - Exam problem (2017)

Consider three systems with three different cache configurations:

- Cache 1: Direct-mapped with one-word blocks
- Cache 2: Direct-mapped with four-word blocks
- Cache 3: Two-way set associative with four-word blocks

For the three configurations, the following miss rate measurements have been made:

- Cache 1: Instruction miss rate is 4%; data miss rate is 9%.
- Cache 2: Instruction miss rate is 2%; data miss rate is 5%.
- Cache 3: Instruction miss rate is 2%; data miss rate is 3%.

For these machines, 40% of the instructions contain a data reference. Assume that the cache miss penalty is 6 + Block size in words. The CPI for this workload was measured on a machine with Cache 1 and was found to be 2.0.
Determine which machine spends the most cycles on cache misses.