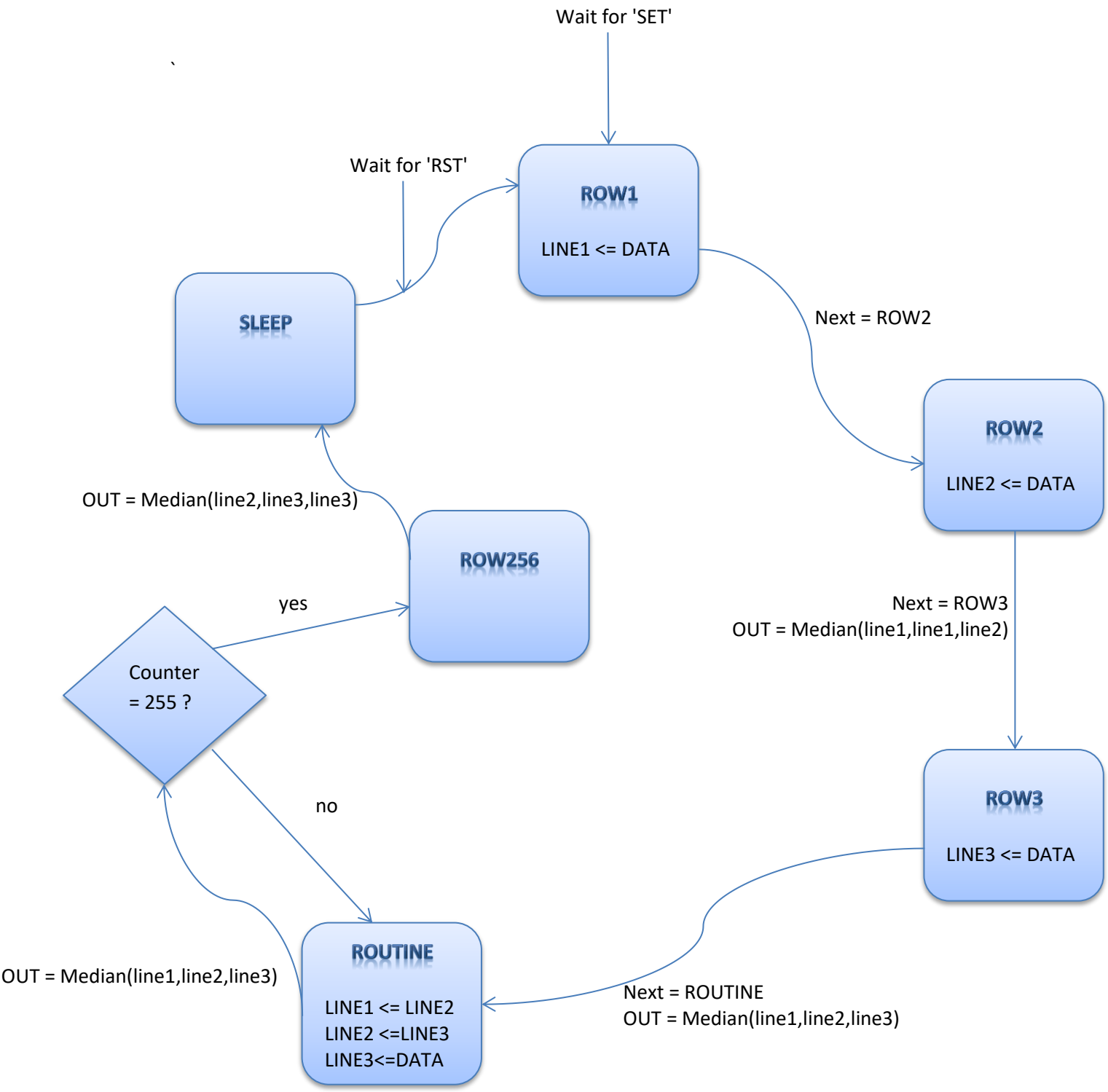
Student: Oded Yosef
Lecturer: Dr. Benjamin Abramov

Final project – VerilogHDL

1. State machine diagram



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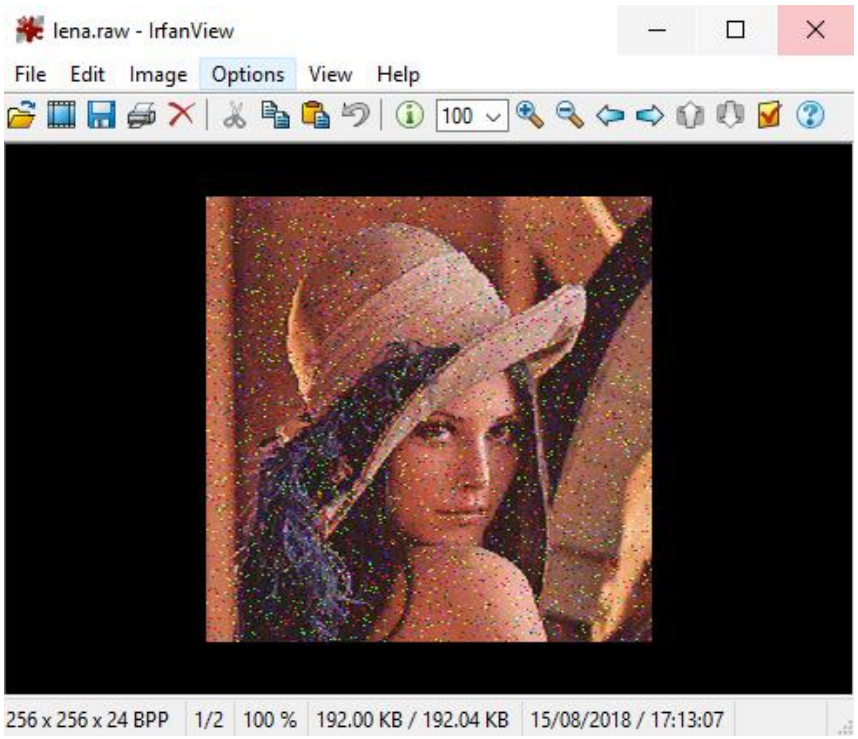
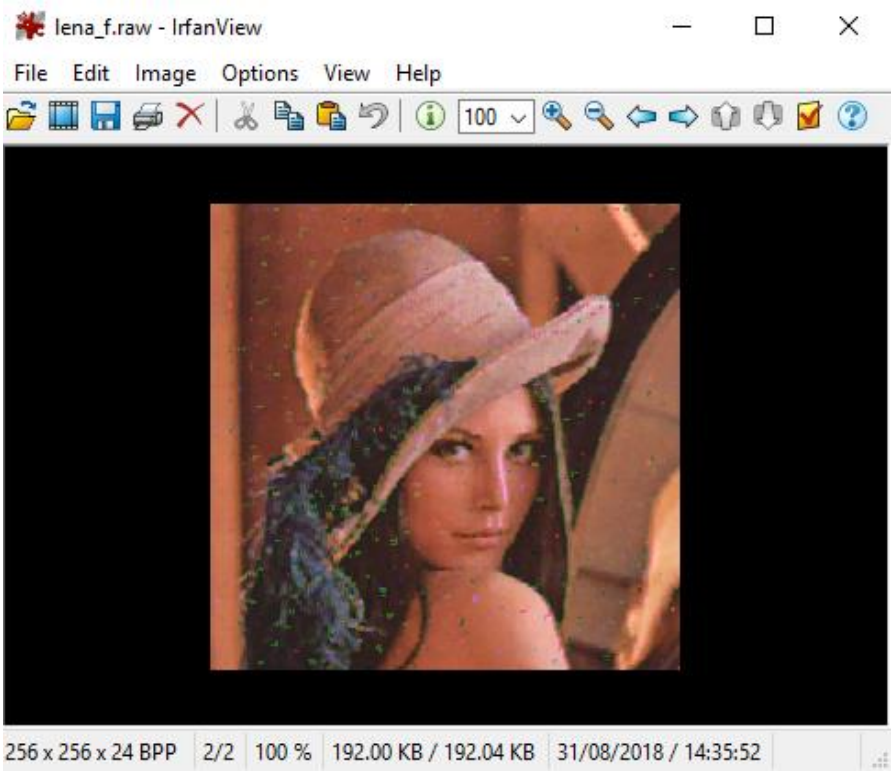
2. Filter impact



Dirty Lena



Filtered Lena

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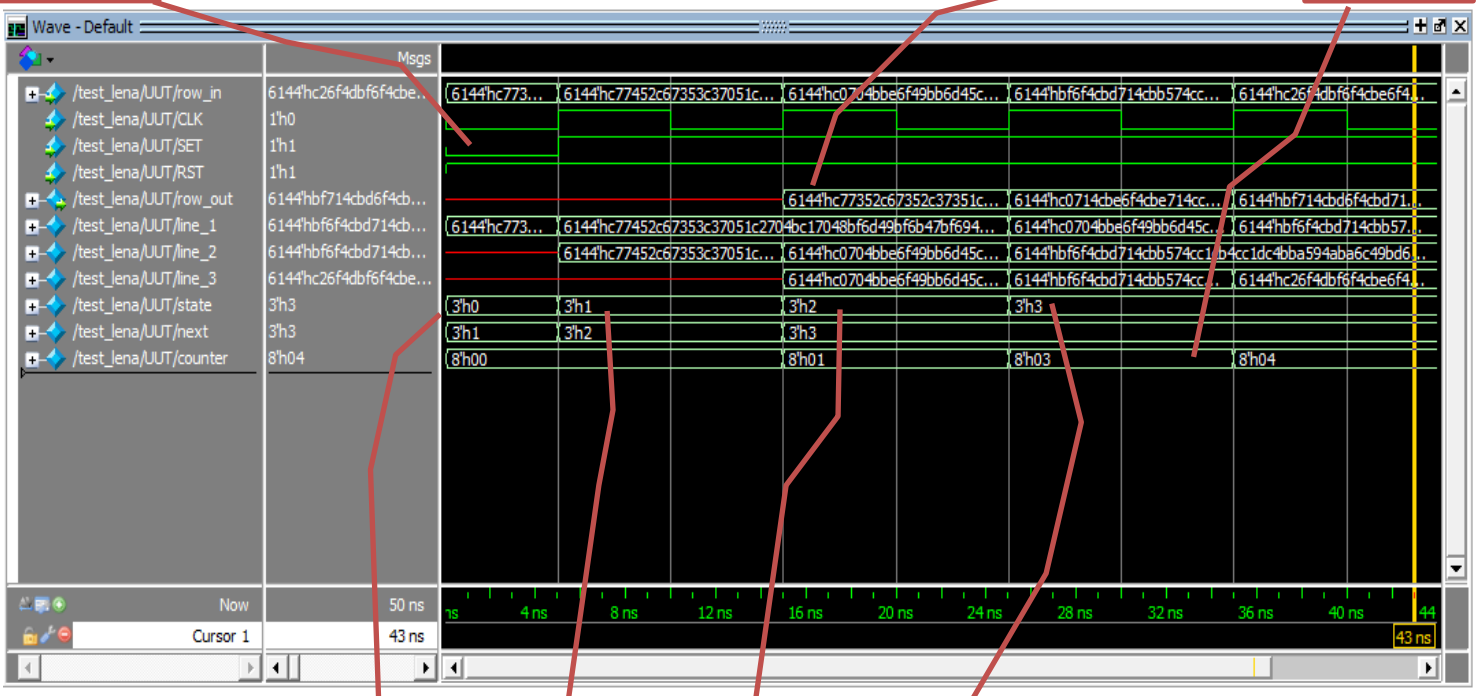
3. Test Bench simulation – wave's timeline

SET = '0' , starting the FSM flow

Start writing to file

Count

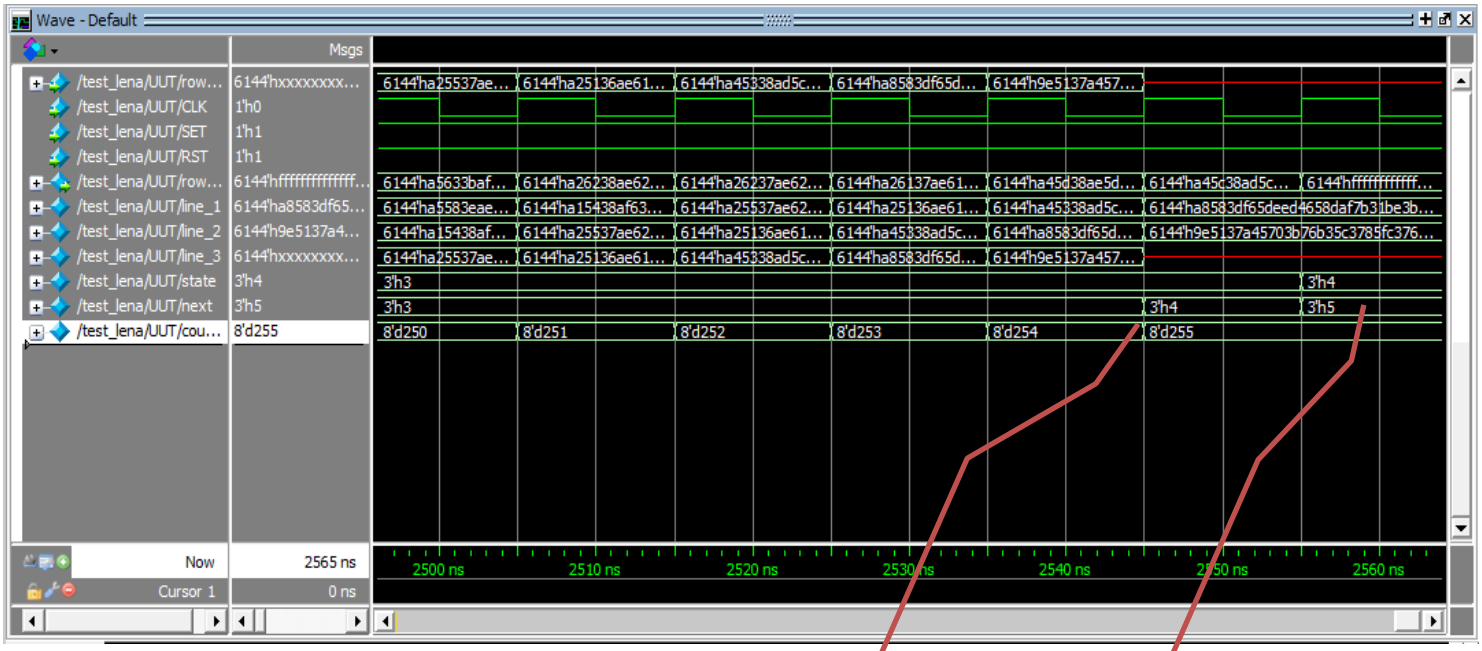


State 0 "ROW1"

State 1 "ROW2"

State 2 "ROW3"

State 3 "ROUTINE"



Counter = 255
Next = state 4
"ROW256"

Next ="SLEEP"

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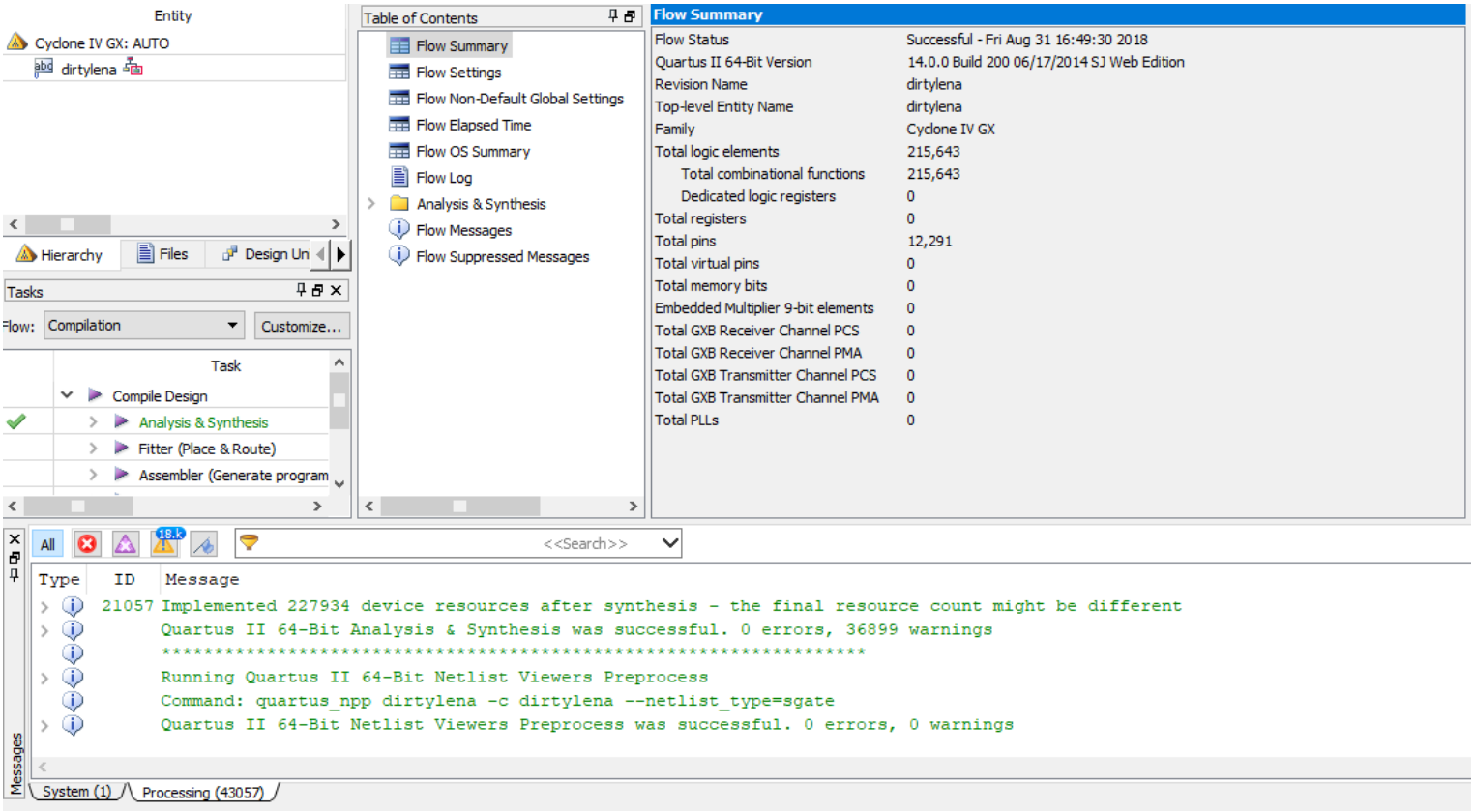
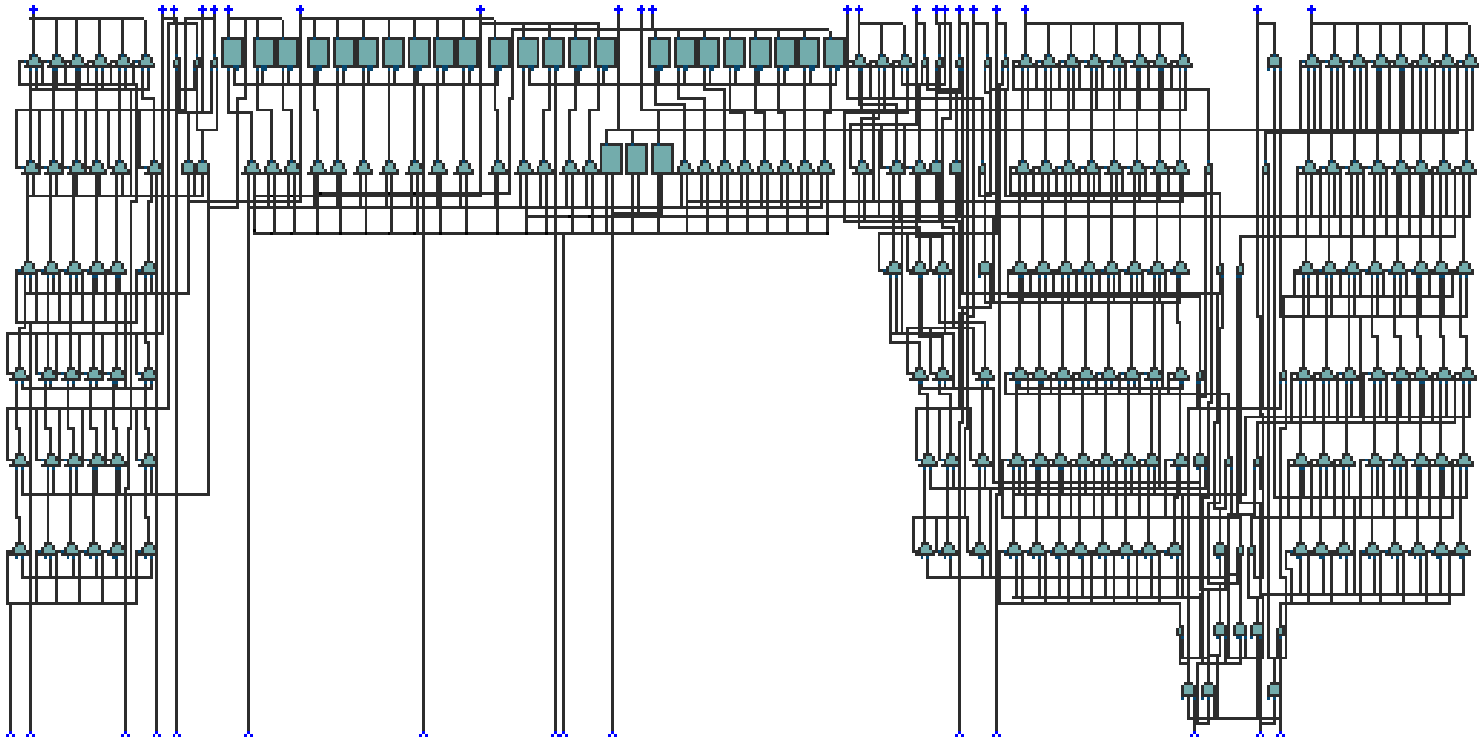
4. Synthesis



Analysis and synthesis, Qaurtus report



RTL View, Quartus