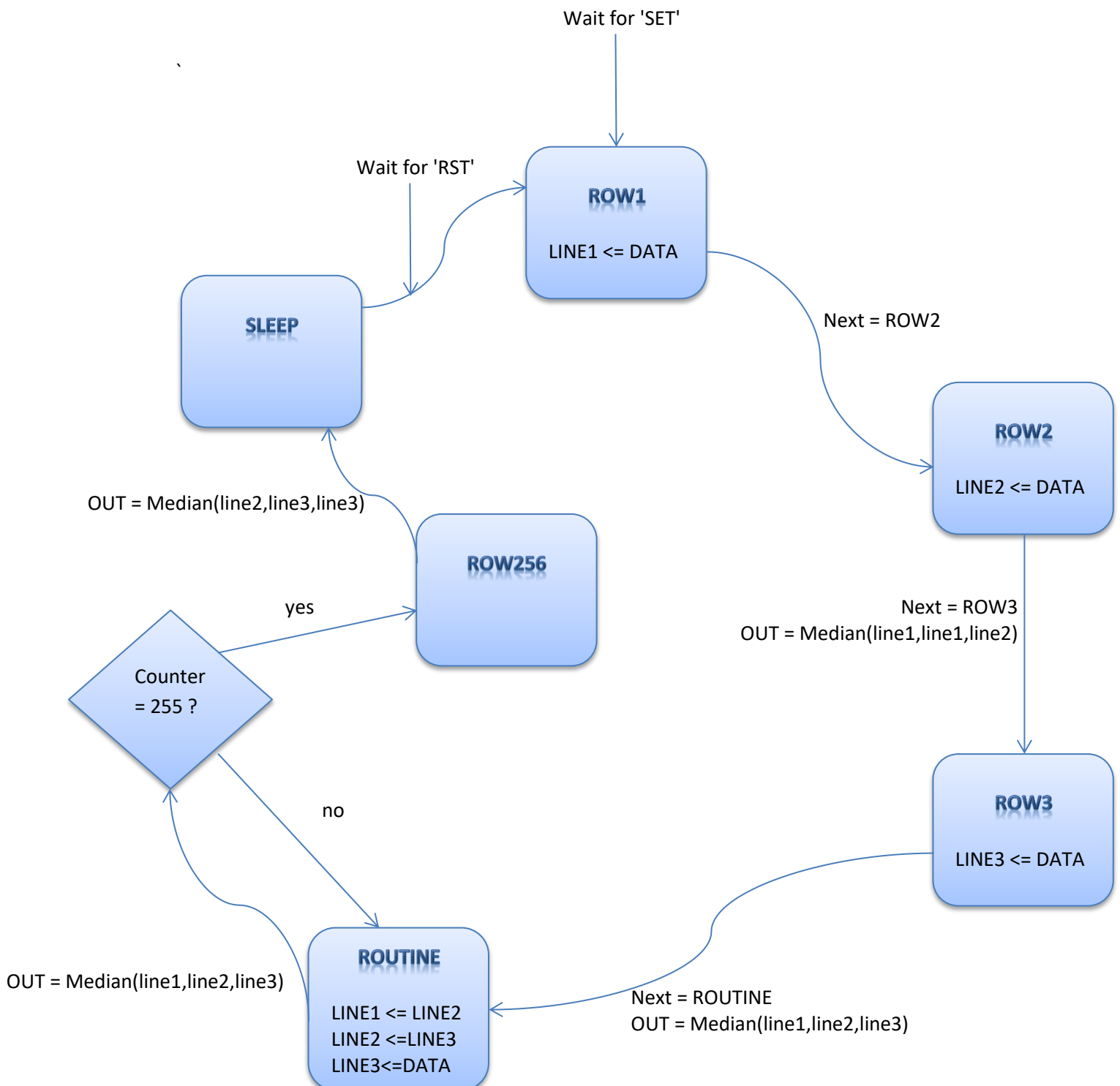
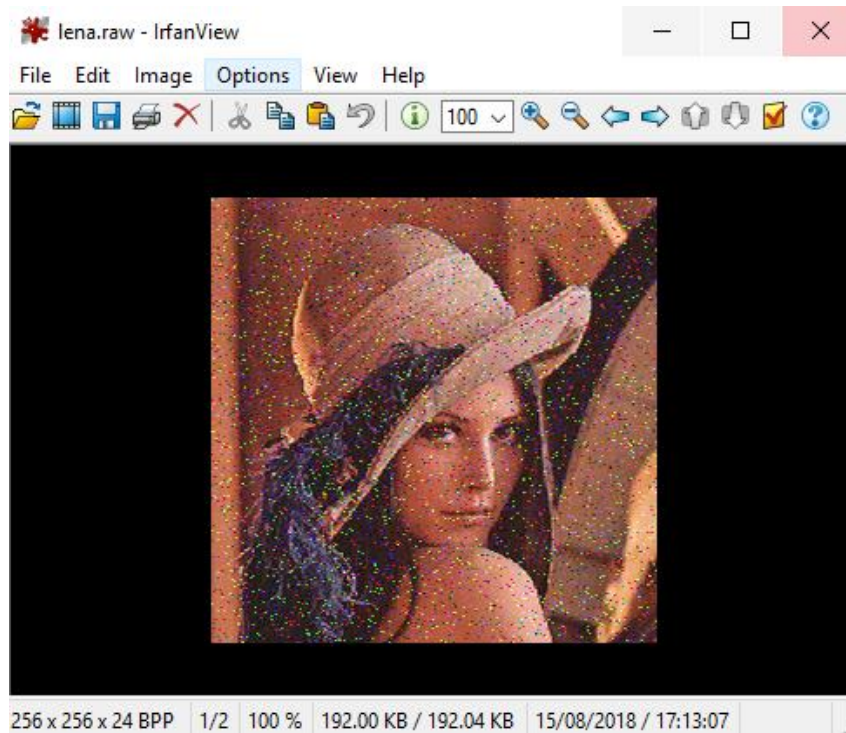


# Final project – VerilogHDL

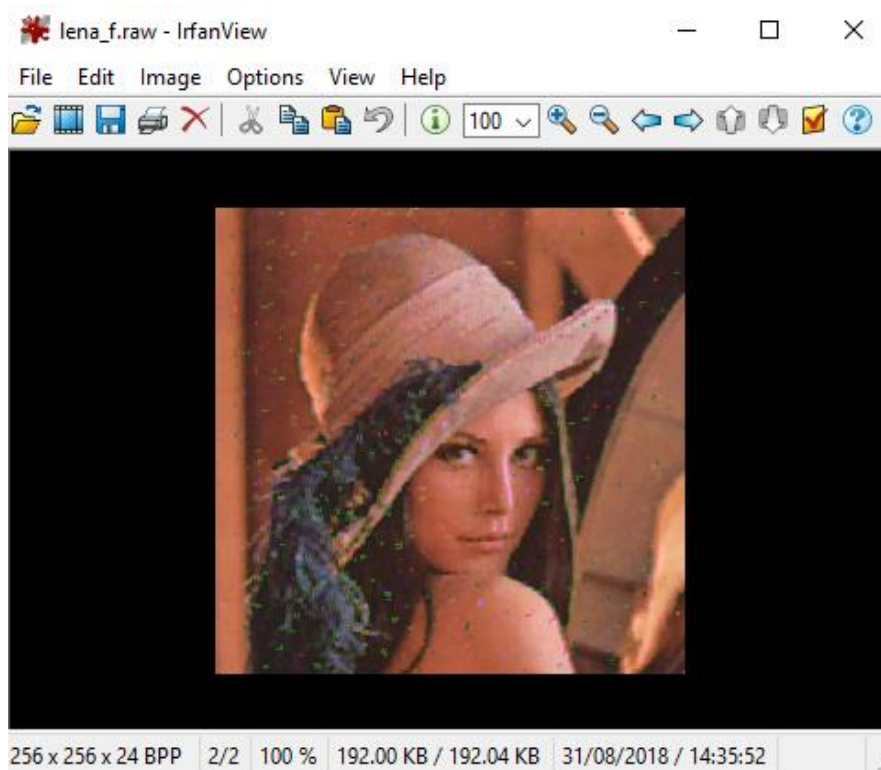
## 1. State machine diagram



## 2. Filter impact



**Dirty Lena**



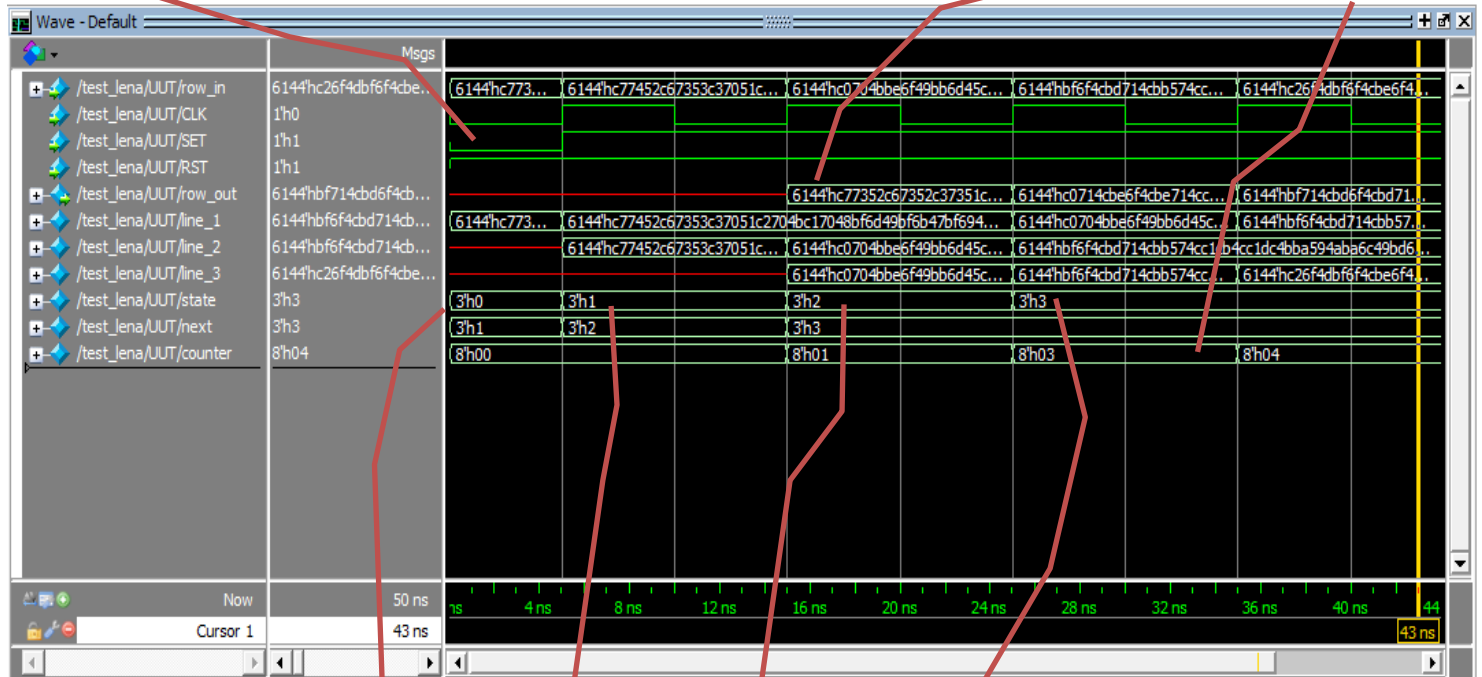
**Filtered Lena**

SET = '0',  
starting the  
FSM flow

### 3. Test Bench simulation – wave's timeline

Start writing  
to file

Count

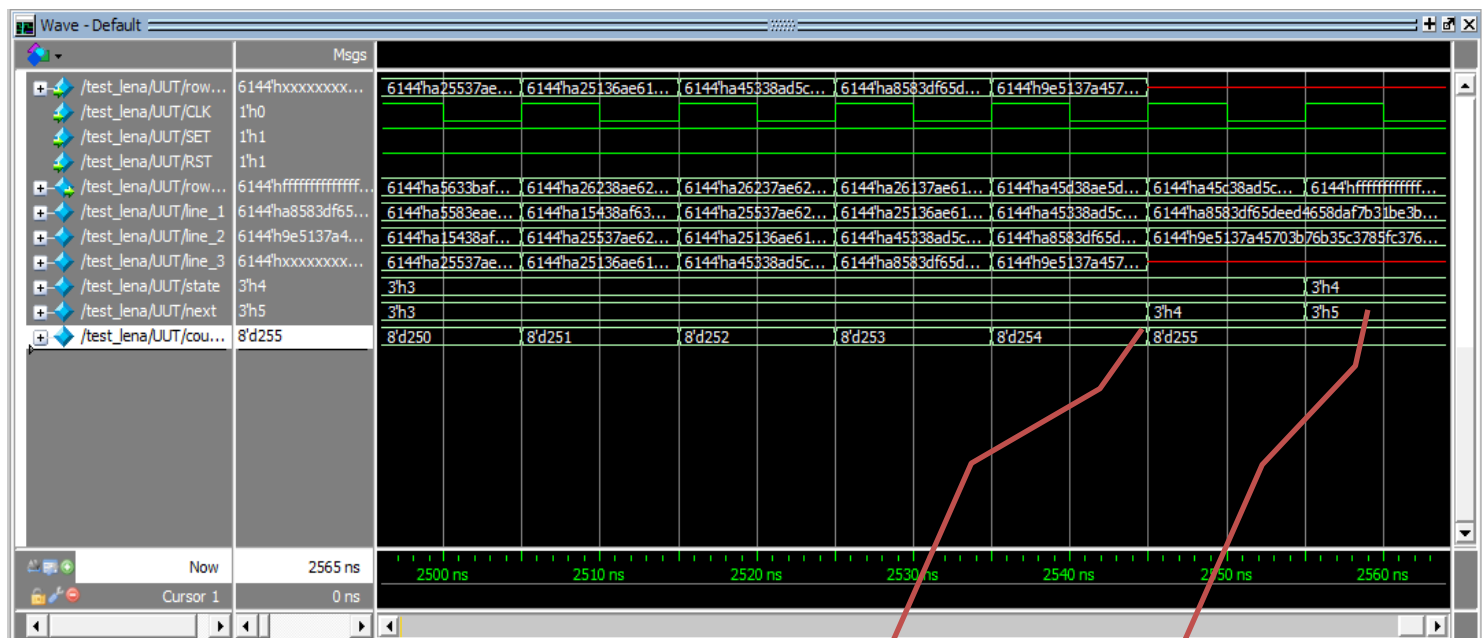


State 0  
"ROW1"

State 1  
"ROW2"

State 2  
"ROW3"

State 3  
"ROUTINE"



Counter = 255  
Next = state 4  
"ROW256"

Next = "SLEEP"

## 4. Synthesis

The screenshot displays the Quartus II IDE interface during the synthesis process. The top-left pane shows the project hierarchy with 'Cyclone IV GX: AUTO' and 'dirtylena'. The top-right pane, titled 'Flow Summary', provides a detailed overview of the synthesis results. The bottom-left pane shows the 'Tasks' list, with 'Analysis & Synthesis' highlighted. The bottom-right pane displays the 'Messages' window, showing the successful completion of the synthesis process.

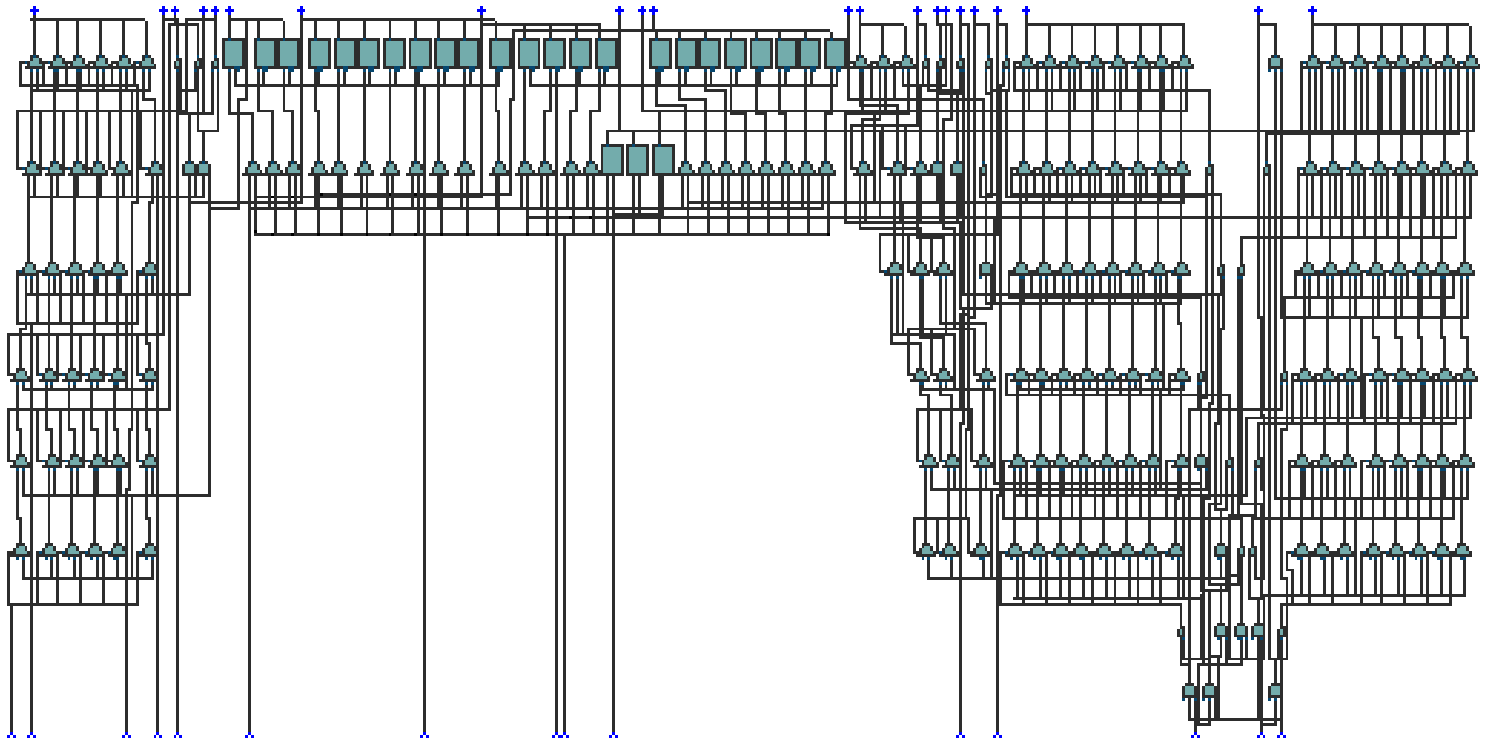
**Flow Summary**

Flow Status	Successful - Fri Aug 31 16:49:30 2018
Quartus II 64-Bit Version	14.0.0 Build 200 06/17/2014 SJ Web Edition
Revision Name	dirtylena
Top-level Entity Name	dirtylena
Family	Cyclone IV GX
Total logic elements	215,643
Total combinational functions	215,643
Dedicated logic registers	0
Total registers	0
Total pins	12,291
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	0
Total GXB Receiver Channel PCS	0
Total GXB Receiver Channel PMA	0
Total GXB Transmitter Channel PCS	0
Total GXB Transmitter Channel PMA	0
Total PLLs	0

**Messages**

```
> 21057 Implemented 227934 device resources after synthesis - the final resource count might be different
> Quartus II 64-Bit Analysis & Synthesis was successful. 0 errors, 36899 warnings
> *****
> Running Quartus II 64-Bit Netlist Viewers Preprocess
> Command: quartus_npp dirtylena -c dirtylena --netlist_type=sgate
> Quartus II 64-Bit Netlist Viewers Preprocess was successful. 0 errors, 0 warnings
```

### Analysis and synthesis, Qartus report



RTL View, Quartus