Daniel Mejia Mendez

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EDUCATION

Syracuse University, College of Engineering and Computer Science **Anticipated May 2027**
Bachelor of Science, Computer Engineering **Cumulative GPA: 3.99**
Honors: Renée Crown Scholar (Syracuse University Honors Program), 1870 Scholar, Success Scholar

TECHNICAL SKILLS

Languages: C++, C, Python, VHDL, SystemVerilog, Assembly (6502), MATLAB, HSPICE, JavaScript, HTML/CSS, SQLite
Applications: Intel Quartus, Cadence, Fusion 360, Blender
Spoken Languages: Spanish
Coursework: Computer Architecture, Intro to VLSI Design (HSPICE), Digital Logic Design (VHDL), Systems and Network Programming (C)
Ongoing Coursework: Digital Signal Processing and Control (MATLAB), Operating Systems, Embedded and Mobile Systems

WORK EXPERIENCE

Bionics Systems and Control Lab – Researcher (FPGA Systems), Syracuse, NY **Dec 2023 - Present**
- Developing a VHDL module to process four analog sensor inputs and encode data for a CAN-FD transceiver on an FPGA.
- Migrating data acquisition from an Arduino-based interface to an FPGA-driven pipeline to reduce latency and overcome bandwidth limitations.
- Integrating FPGA-based systems into ongoing human-robot interaction research in collaboration with lab researchers.

Department of Physics - Peer Coach, Syracuse, NY **Aug 2024 – Present**
- Facilitated Astronomy 101 lab sections covering light, optics, and celestial mechanics.
- Conducted weekly physics recitations alongside graduate TAs, teaching classical mechanics and electricity and magnetism.

Academic Excellence Workshop - Facilitator (Python Programming), Syracuse, NY **Aug 2025 – Dec 2025**
- Led weekly collaborative sessions for 9 students in introductory programming using Python.
- Developed original problem sets with course faculty to emphasize logic, debugging, and problem-solving strategies.

PROJECTS

32-Bit Pipelined Processor (SystemVerilog, RTL Simulation & Synthesis)
- Developing a modular 32-bit pipelined processor from scratch in SystemVerilog, targeting a custom ISA and multi-stage datapath architecture.
- Designed and implemented a fully synthesizable 32-bit barrel shifter supporting logical shifts and rotates.
- Simulating and debugging RTL using Icarus Verilog and Surfer, validating signal timing and hardware behavior.
- Writing SystemVerilog testbenches with reference models to verify behavior across edge cases.

4-Bit CPU (VHDL, Quartus, EDA Playground, DE-10 Lite FPGA)
- Designed and implemented a 4-bit CPU in VHDL with a custom ALU, ROM, program counter, registers, branching logic, and control FSM.
- Developed a finite-state machine to coordinate the fetch–decode–execute cycle and manage branching and ALU operations.
- Simulated and validated instruction flow using Riviera Pro and EPWave waveform analysis prior to FPGA deployment.

8-Bit 6502-Based Breadboard Computer (6502 Assembly, C++, Arduino IDE)
- Designed and built an 8-bit computer using the W65C02S CPU with custom address decoding, clock, memory, and I/O.
- Wrote assembly to control hardware via memory-mapped I/O, including fixed-point (8.8) arithmetic.
- Verified MHz bus timing and signal integrity using an Arduino logic probe and oscilloscope.

Motion Controlled Robotic Arm (C++, Arduino IDE, Fusion 360, Ubuntu, ESP32, Raspberry Pi)
- Programmed an ESP32-based IMU system to capture joint motion and transmit data via BLE for real-time control.
- Integrated IMU sensing and servo control using ROS2; designed and assembled robotic hardware with CAD.

EXPERIENCE AND LEADERSHIP

Management Leadership for Tomorrow - Career Prep Fellow **Jan 2024 – Present**
- Accepted into a selective 18-month professional development program for high-achieving diverse talent.
- Complete business case studies and assignments to grow leadership and technical skills.
- Attend conferences hosted by industry leaders such as Deloitte, LinkedIn, and Target.