

AM69 Processor Starter Kit

TABLE OF CONTENTS

PAGE	CONTENTS
01	TABLE OF CONTENTS
02	REVISION HISTORY
03	SYSTEM BLOCK DIAGRAM
04	3-Phase DUAL PMIC PDN-OB DIAGRAM
05	Power Flow Diagram
06	I2C Tree
07	I2C TABLE
08	GPIO MAPPING TABLE
09	SOC : CSI & DSI INTERFACE
10	SOC : SERDESO INTERFACE
11	SOC : SERDES1 INTERFACE
12	SoC: LPDDR4 - DDR0
13	SoC: LPDDR4 - DDR2
14	SoC: LPDDR4 - DDR1
15	SoC: LPDDR4 - DDR3
16	SOC: OSPI FLASH
17	SOC: MCU & MAIN GENERAL IO, OSC CLKs
18	SOC: GENERAL IO
19	SOC: MCU RGMII / MMC[0:1] / ADC
20	SOC: DEBUG and XDS110 MUX
21	SOC: USB2.0
22	SOC: ANALOG POWER 1
23	SOC: IO POWER 2
24	SOC : DIGITAL POWER 3
25	SOC: GROUND
26	RESET BUTTONS
27	CPLD
28	Board ID EEPROM & 40 Pin EXP Header
29	eMMC FLASH
30	Micro SD CARD INTERFACE
31	USB3.0 HUB

PAGE	CONTENTS
32	USB 3.0 TYPE-A CONNECTORS - 1
33	USB 3.0 TYPE-A CONNECTORS - 2
34	USB 3.0 TYPE C INTERFACE
35	PCIe_M.2_INTERFACE(M Key)
36	PCIe_M.2_INTERFACE(E Key)
37	PCIe x4 Card Slot
38	MCU GB ETHERNET
39	CSI MUX - DATA
40	CSI2 EXPANSION CONNECTOR
41	CSI2 FPC CAMERA CONNECTORS
42	DISPLAY PORT INTERFACE
43	DVI/HDMI TRANSMITTER
44	ENET EXPANSION CONNECTOR
45	CAN TRANSCEIVERS #2-MAIN DOMAIN
46	QUAD PORT CONSOLE
47	XDS110 DEBUGGER
48	TEST AUTOMATION HEADER
49	Power Input
50	POWER SUPPLY #1
51	POWER SUPPLY #2
52	POWER SUPPLY #3
53	HCPS A - VDD CPU
54	HCPS A - VDD CORE
55	SOC PMIC
56	SOC LDO's
57	SOC CURRENT SENSE RESISTORS
58	CURRENT MONITORS - INA226
59	CURRENT MONITORS - INA231
60	PMIC SUPPORT CIRCUIT
61	SERDES CLOCK GENERATOR
62	SK NOTES & ACCESSORIES

REVISION HISTORY

REV #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
E2	21 OCT 2022	Taken AM69 SK Rev E1 design as reference and Added CDCI6214 clock generators for PCIe devices	Mistral Design Team		
	2 NOV 2022	1. Replaced U113 with clock buffer CDCDB400 as a clock source for PCIe M key and E key. 2. Updated U50 connection to provide resistor mux for CDCI1_OE2/OE3 and CDCI1_OE1/OE4 signals from U112	Mistral Design Team		
E2A	23 FEB 2023	Added ECN information for TIVA automation rework.	Mistral Design Team		
E2B	13 MAR 2023	1.Updated L1 L6 part number to XAL7070-122MEC 2.Updated U76 U78 part number to BSZ019N03LSATMA1	Mistral Design Team		
E3	16 MAR 2023	1.Updated L1 L6 part number to XAL7070-102MEC 2.Updated U76 U78 part number to CSD18563Q5A 3.Updated U75 U81 part number to CSD18543Q3A. 4. C36, R48,C42, R50 values have been modified. 5.TA_I2C_SCL , TA_I2C_SDA have been swapped with PM2_SCL, PM2_SDA. 6.Updated FB1, L28, R130, R368,R347,R267 to OE for EMC compliance. 7.Made C801, C448, C441,C111 DNI.	Mistral Design Team		

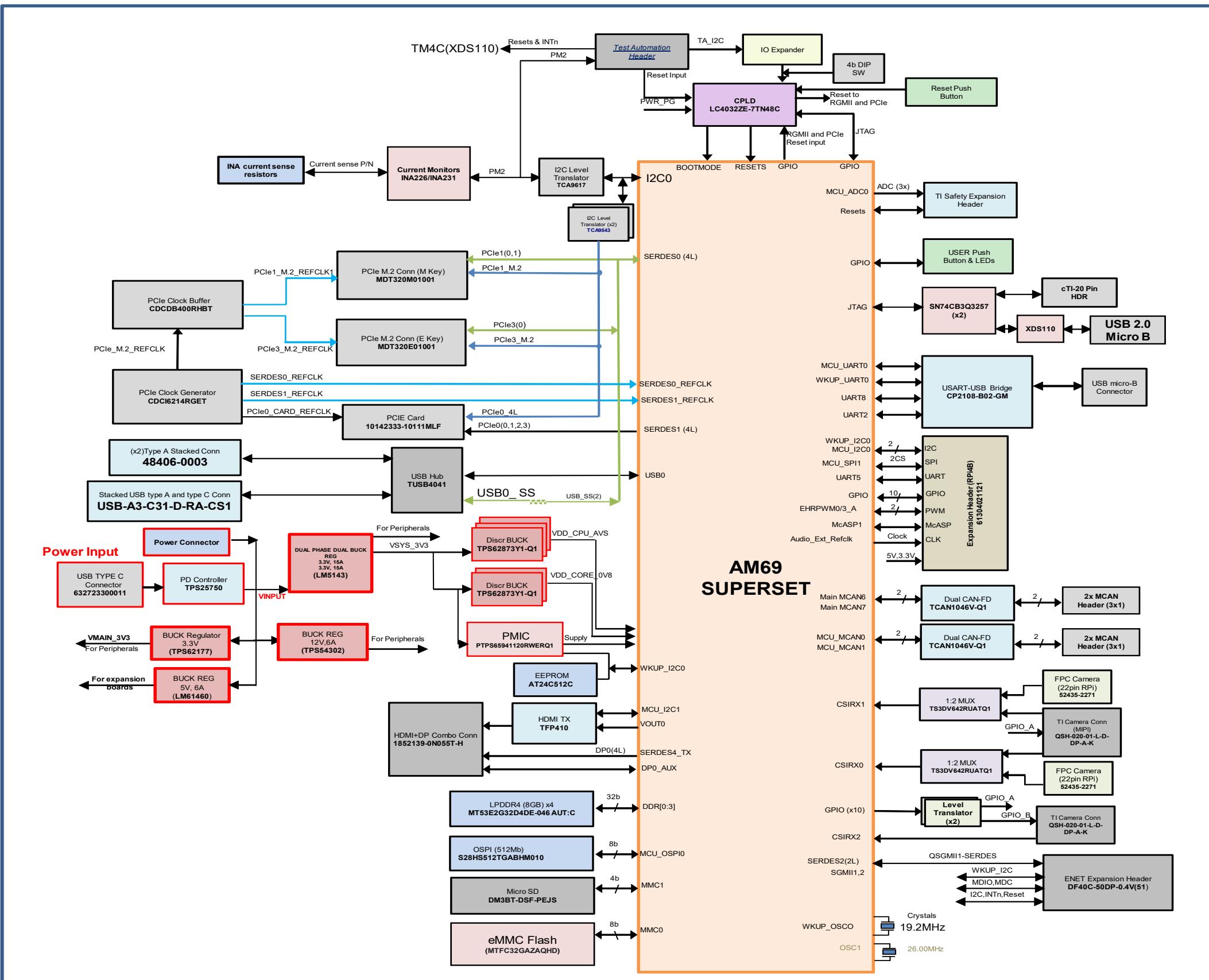
Project :



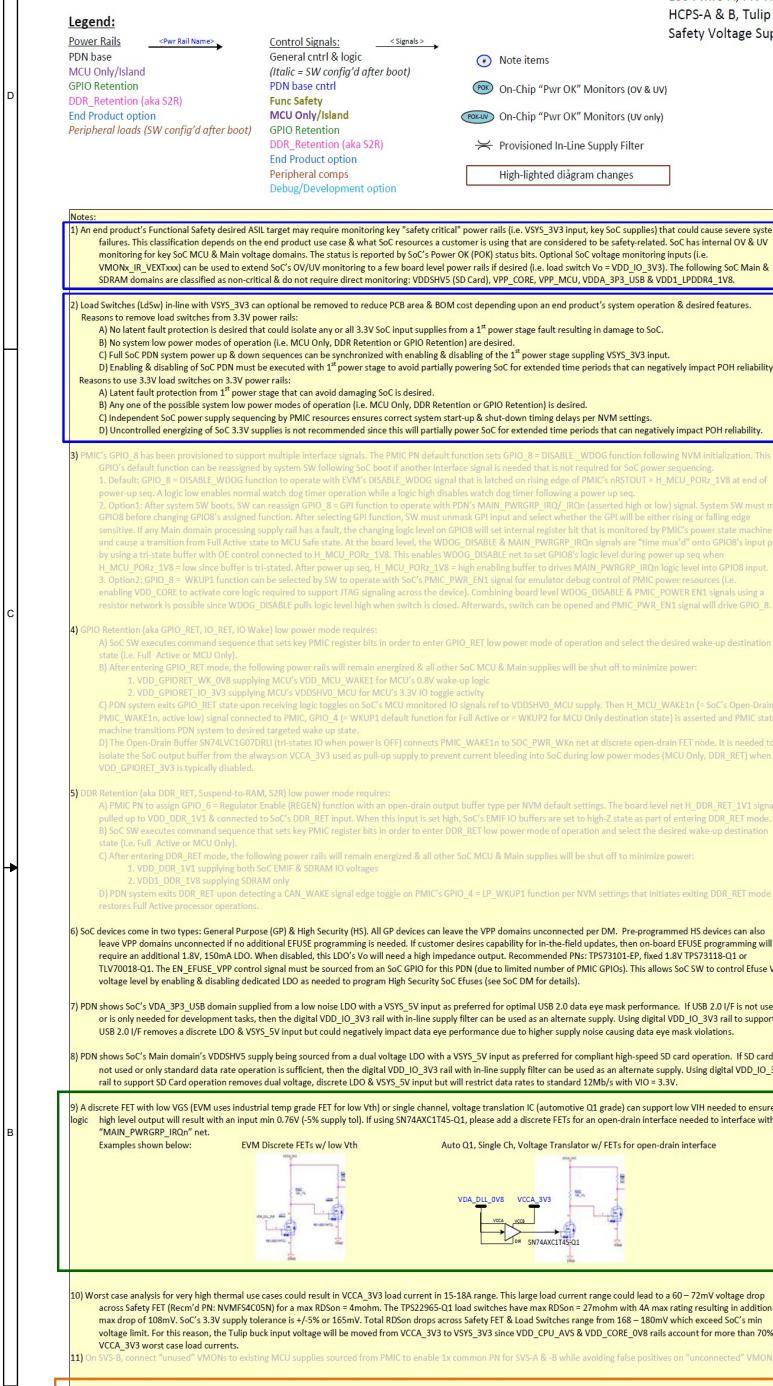
REVISION HISTORY

ze	PROC154E3 001 SK AM69	Rev
C		E3
ate:	Wednesday, March 29, 2023	Sheet 2 of 62

SYSTEM BLOCK DIAGRAM



PDN Recommended for New Designs



Leo PMIC-A, PN TPS6594133ARWERQ1 (TIPN ID = 1, MP Buck Rails = 3, PG2.0 NVM ID = 13 rev 2)
 HCPs-A & B, Tulip PN TPS62873Y1QWRXSRQ1 (ISA PN ID = 3, Jacinto7 Family ID = Y1)
 Safety Voltage Supervisor, PN TPS389006004TERTRQ1 (OTP ID = 004 = new common PN for use with Jacinto7 J7845A PDN-3A scheme)

Features Supported (EVM Max Features):

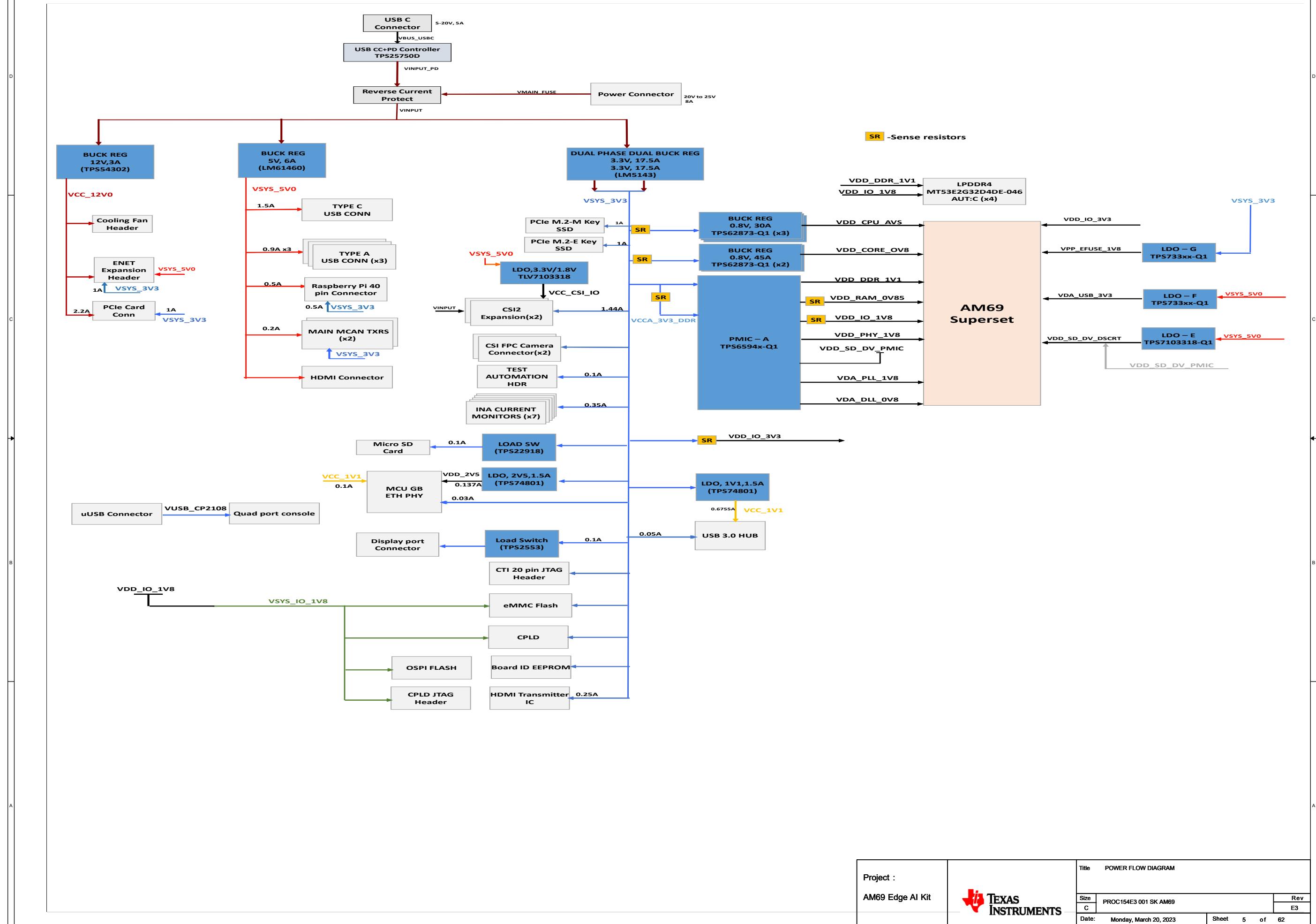
1. SoC performance: Max 2.0GHz clock with SERDES interfaces operational
2. a. Not a Functional Safety capable sys
- b. Grouped Main & MCU power rails (no supply FFI)
3. 4x SDRAMs: 32Gb, 4-Die, 32b, 4266MTs, LPDDR4 mode
4. Boot & Mass Flash: Octal SPI or Hyperflash & eMMC, UFS
5. Signaling Levels: MCU & Main Dual VIO

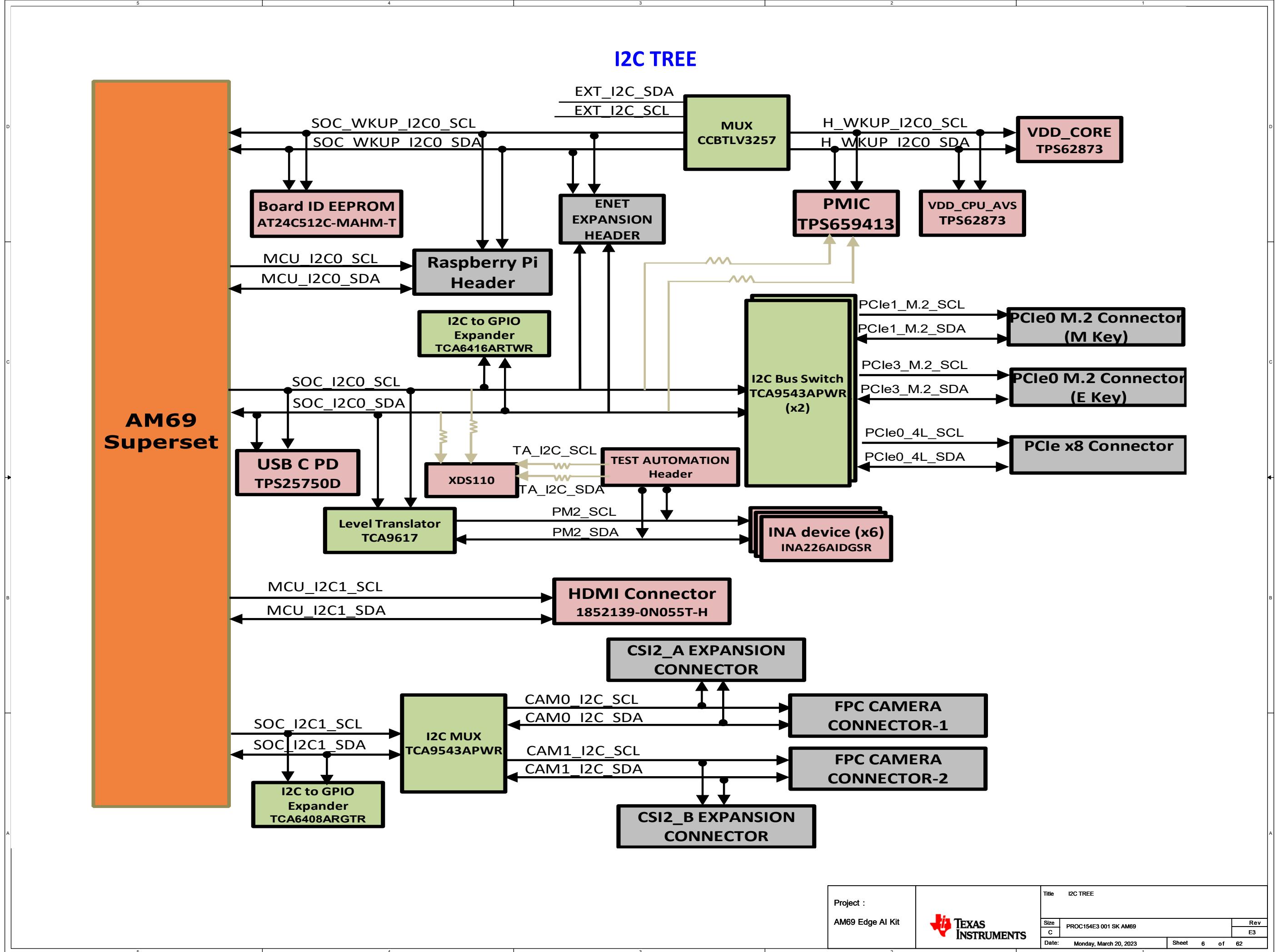
(All SoC PN variants: TDA4AP/VP/AH/VH)
 (Power Rail & GPIO Mapping Overview)

PDN-3H.1 History
 V0.6 10/05/2022 BMC Initial capture J7845A EVM Single Lite Dual HCPs PDN-3H.1 derived from PDN-3H v0.6 with following changes:
 1. Removed In-line Safety FET to reduce cost & area
 2. Removed Safety Voltage Supervisor
 3. Removed load switch supplying VDD_IO_3V3 to SoC and updated Note 2.
 4. Add SEL_3V3_VBN control signal to PMIC's GPIO6 from SoC GPIO to provision LDO2 to supply dual VIO for SD card HSD-I operation

7. End Product Options:
 - Compliant high-speed SD Card (needs 1 indep pwr rail & 1 VIO ctrl signal & discrete LDO needs Vin = 5V)
 - Compliant USB 2.0 data eye (needs 5V, 1 indep pwr rail & discrete LDO needs Vin = 5V)
 - HS SoC Efuse programming on-board (needs 1 indep pwr rail & 1 ctrl signal)

AM69 SK POWER FLOW DIAGRAM





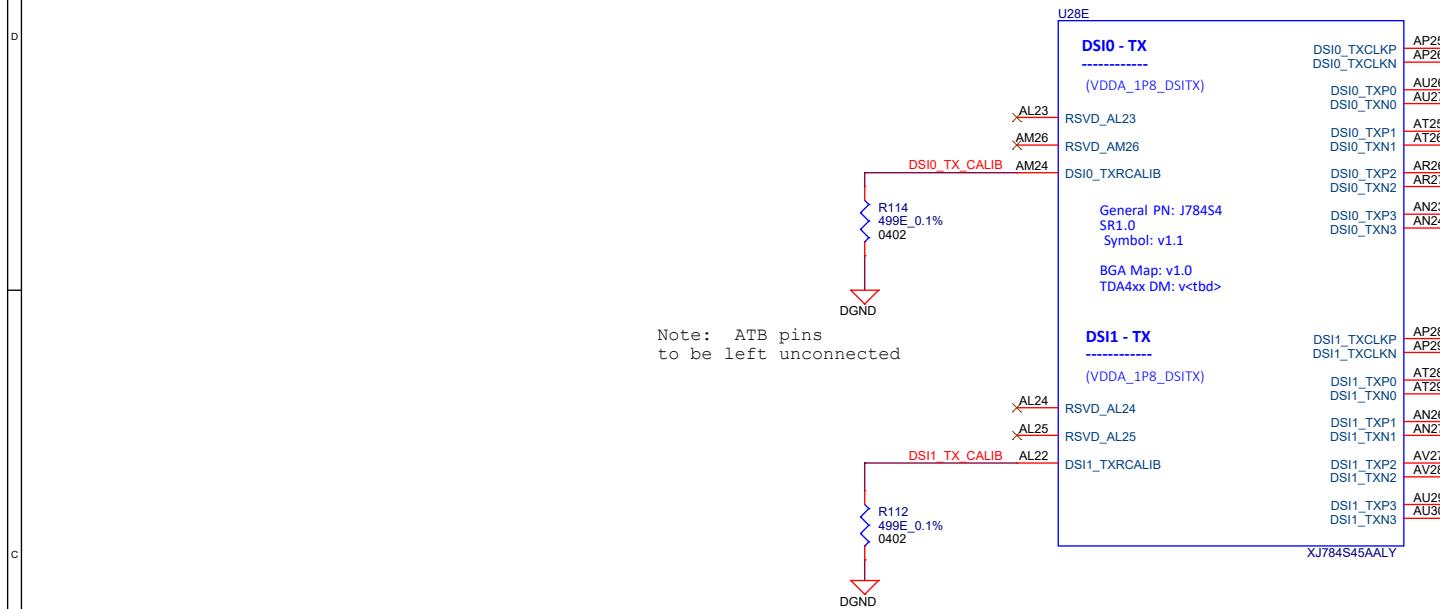
I2C TABLE

AM69 SK I2C Slave Address Table			
SOC I2C Port	Device Description	Part#	I2C Address
WKUP_I2C0	PMIC	TPS6594133ARWERQ1	0x48, 0x49, 0x4A & 0x4B
	VDD_CPU_AVs High-Current Power Stage A	TPS62873Y1QWRXSRQ1	0x40
	VDD_CORE_0V8 High-Current Power Stage B	TPS62873Y1QWRXSRQ1	0x43
	Raspberry Pi Header	61304021121	
	Board ID EEPROM	AT24C512C-MAHM-T	0x51
	ENET Expansion Header	171446-1109	0x57
MCU_I2C0	Raspberry Pi Header	61304021121	
MAIN_I2C0	Test Automation Header	687140183622	
	INA226 device for VCCA_3V3_CORE	INA226AIDGSR	0x45
	INA226 device for VCCA_3V3_CPU_AVs	INA226AIDGSR	0x4F
	INA226 device for VCCA_3V3_DDR	INA226AIDGSR	0x4D
	INA226 device for VDD_RAM_0V85	INA226AIDGSR	0x46
	INA226 device for VDD_IO_3V3	INA226AIDGSR	0x41
	INA226 device for VDD_IO_1V8	INA226AIDGSR	0x40
	PCIe_M.2_Interface M Key	MDT320M01001	
	PCIe_M.2_Interface E Key	MDT320E01001	
	Ext Power Measurement Header	61300311121	
	PCIe Card Slot	10018783-10202TLF	
	USB C PD Controller	TPS25750D	0x20
	Level Translator-1	TCA9543APWR	0x71
	Level Translator-2	TCA9543APWR	0x72
	GPIO Expander	TCA6416ARTWR	0x21
MCU_I2C1	PMIC	TPS6594133ARWERQ1	
	ENET Expansion Header	171446-1109	0x77
	HDMI Connector	1852139-0N055T-H	
	FPC Camera Connector 1	52435-2271	
	FPC Camera Connector 2	52435-2271	
	CSI2_A Expansion Connector	QSH-020-01-L-D-DP-A-K	
MAIN_I2C1	CSI2_B Expansion Connector	QSH-020-01-L-D-DP-A-K	
	GPIO Expander	TCA6408ARGTR	0x21
	Level Translator	TCA9543APWR	0x70

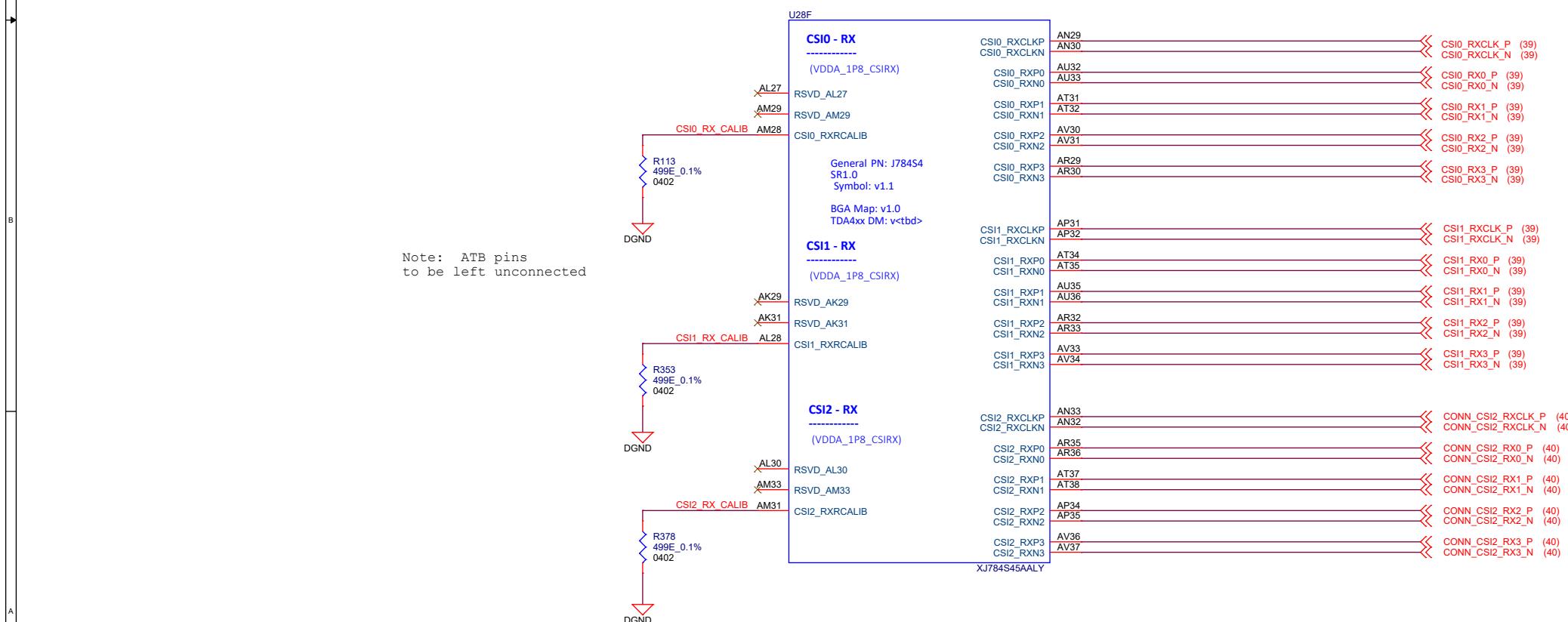
GPIO MAPPING TABLE

GPIO Mapping						
WKUP Domain						
J7AHP Mapping		Net Name	Input/Output	Default	State	Usage
Package Signal Name	GPIO					
MCU_OSP1_Csn1	WKUP_GPIO_28	EN_EFUSE_VPP	O	PD	Active High	Enable for VPP_EFUSE_1V8 LDO
MCU_OSP1_Csn2	WKUP_GPIO_29	CPLD_TMS/CSIB_EXP_GPIO1	IO	NA	NA	GPIO signal for CS12 EXPANSION Connector
MCU_OSP1_CLK	WKUP_GPIO_31	CPLD_TCK/CSIB_EXP_GPIO2	IO	NA	NA	GPIO signal for CS12 EXPANSION Connector
MCU_OSP1_LBCLK0	WKUP_GPIO_32	CSI_EXP_GPIO_1	IO	NA	NA	GPIO signal for CS12 EXPANSION Connector
MCU_OSP1_DQS	WKUP_GPIO_33	CPLD_TDO/CSIB_EXP_GPIO3	IO	NA	NA	GPIO signal for CS12 EXPANSION Connector
MCU_OSP1_D0	WKUP_GPIO_34	CPLD_TDI/CSIB_EXP_GPIO4	IO	NA	NA	GPIO signal for CS12 EXPANSION Connector
MCU_OSP1_D1	WKUP_GPIO_35	CSI_EXP_GPIO_5	IO	NA	NA	GPIO signal for CS12 EXPANSION Connector
MCU_OSP1_D2	WKUP_GPIO_36	CSI_EXP_GPIO_2	IO	NA	NA	GPIO signal for CS12 EXPANSION Connector
MCU_OSP1_D3	WKUP_GPIO_37	CSI_EXP_GPIO_3	IO	NA	NA	GPIO signal for CS12 EXPANSION Connector
MCU_OSP1_Csn0	WKUP_GPIO_38	CSI_EXP_GPIO_4	IO	NA	NA	GPIO signal for CS12 EXPANSION Connector
MCU_OSP1_Csn1	WKUP_GPIO_39	CSIB_EXP_GPIO5	IO	NA	NA	GPIO signal for CS12 EXPANSION Connector
MCU_SPI_CLK	WKUP_GPIO_54	WKUP_GPIO_54	O	Bootmode	Active High	Select line for CPLD's Mux
MCU_SPI_D0	WKUP_GPIO_55	USER_LED1	O	Bootmode	Active High	User LED
MCU_SPI_D1	WKUP_GPIO_69	SYS_MCU_PWRDN	O	Bootmode	Active High	System Power Down ('0' - normal operation '1' - system power down)
MCU_SPI_CS0	WKUP_GPIO_70	WKUP_GPIO_70	O	NA	NA	GPIO signal for FPC camera Connector
WKUP_GPIO_10	WKUP_GPIO_10	HDMI_LS_OE	O	PU	Active High	Level Shifter Output Enable for HDMI
WKUP_GPIO_14	WKUP_GPIO_14	HDMI_PDn	O	Bootmode	Active Low	Power Down Signal for HDMI
WKUP_GPIO_49	WKUP_GPIO_49	WKUP_GPIO_49	IO	NA	NA	GPIO signal for 40 pin Expansion Header
PMIC_POWER_EN1	WKUP_GPIO_88	WKUP_GPIO_88	IO	NA	NA	GPIO signal for FPC camera Connector
WKUP_GPIO_56	WKUP_GPIO_56	WKUP_GPIO_56	IO	NA	NA	GPIO signal for 40 pin Expansion Header
WKUP_GPIO_57	WKUP_GPIO_57	WKUP_GPIO_57	IO	NA	NA	GPIO signal for 40 pin Expansion Header
MCU_ADC1_AIN0	WKUP_GPIO_79	SOC_INT1z	I	PU	Active Low	Test Automation INT signal
MCU_ADC1_AIN1	WKUP_GPIO_80	SOC_INT2z	I	PU	Active Low	Test Automation INT signal
MCU_ADC1_AIN2	WKUP_GPIO_81	MCU_RGMII_INT#	I	PU	Active Low	Interrupt Signal from RGMII
MCU_ADC1_AIN3	WKUP_GPIO_82	SOC_WAKE	I	PU	Active High	SOC wake signal from Reset Button
MCU_ADC1_AIN4	WKUP_GPIO_83	PMIC_INTrn	I	PU	Active Low	PMIC interrupt signal
MCU_ADC1_AIN5	WKUP_GPIO_84	ENET1_EXP_INTB	I	NA	NA	Interrupt Signal from ENET Expansion Header
MCU_ADC1_AIN6	WKUP_GPIO_85	IO_EXP_I2CO_INTB	O	NA	NA	I2CO Interrupt Signal to ENET Expansion Header
WKUP_GPIO_66	WKUP_GPIO_66	WKUP_GPIO_66	IO	PU	NA	GPIO signal for 40 pin Expansion Header
WKUP_GPIO_67	WKUP_GPIO_67	WKUP_GPIO_67	IO	NA	NA	GPIO signal for 40 pin Expansion Header
Main Domain						
EXTINTn	GPIO_0	HDMI_HPD	I	NA	Active High	HDMI hot plug detect signal
MCAN13_TX	GPIO_3	GPIO_3	IO	NA	NA	GPIO signal for 40 pin Expansion Header
MCAN13_RX	GPIO_4	DPO_3V3_EN	O	PD	Active High	Enable signal for Display port Current Limiter
MCAN1_TX	GPIO_27	GPIO_27	IO	NA	NA	GPIO signal for 40 pin Expansion Header
MCASP0_AXR8	GPIO_36	GPIO_36	IO	NA	NA	GPIO signal for 40 pin Expansion Header
ECAPO_IN_APWM_OUT	GPIO_49	SEL_SDIO_3V3_1V8n	O	PU	Active Low	One of Enable signal for VDD SD DV
GPIO Expander						
Port No	GPIO	I2C	Input/Output	Default	State	Usage
P0	CSI_VIO_SEL	MAIN_I2C1 Address : 0x21 Part No - TCA6408ARGTR	O	PD	Active High	Enable signal for Camera IO supply
P1	CSI_MUX_SEL_2		O	PD	Active High	Select lines for CSI mux
P2	CSI2_RSTz		O	PD	Active Low	Reset signal for CSI Expansion Connector
P3	IO_EXP_CAM0_GPIO1		IO	NA	NA	GPIO signals for FPC Camera Connector
P4	IO_EXP_CAM1_GPIO1		IO	NA	NA	GPIO signals for FPC Camera Connector
P00	BOARDID EEPROM_WP	MAIN_I2CO Address : 0x21 Part No - TCA6416ARTWR	O	PD	Active High	Board ID EEPROM Write Protect
P01	CAN_STB		O	PD	Active High	Stand By Input for CAN Transceiver
P02	GPIO_uSD_PWR_EN		O	PU	Active High	One of Enable signal for Micro SD Load Switch
P03	IO_EXP_MCU_RGMII_RST#		O	NA	Active Low	MCU_RGMII Reset signal to CPLD
P04	IO_EXP_PCIE0_4L_PERST#		O	NA	Active Low	PCIe 4 lane Reset signal to CPLD
P05	IO_EXP_PCIE1_M2_RTSz		O	NA	Active Low	PCIe M Key Reset signal to CPLD
P06	IO_EXP_PCIE3_M2_RTSz		O	NA	Active Low	PCIe E Key Reset signal to CPLD
P07	PM_INA_BUS_EN		O	PU	Active High	Enable signal for PM2 I2C lines
P10	ENET1_EXP_PWRDN		O	PU	Active High	Power Down Signal for Enet Expansion Header
P11	EXP1_ENET_RSTz		O	NA	Active Low	Reset Signal for Enet Expansion Header
P12	ENET1_I2CMUX_SEL		O	NA	Active High	I2C mux select Signal for Enet Expansion Header
P13	PCle0_CLKREQ#		I	PU	Active Low	PCIe Card Clock request Signal
P14	PCle1_M2_CLKREQ#		I	PU	Active Low	PCIe M Key Clock request Signal
P15	PCle3_M2_CLKREQ#		I	PU	Active Low	PCIe E Key Clock request Signal
P16	CDCI1_OE2/OE3	TEST AUTOMATION I2C Address : 0x20 Part No - TCA6408ARGTR	IO	PU	NA	GPIO signal CDCI Clock Generator
P17	CDCI1_OE1/OE4		IO	PU	NA	Output Enable for CDCI Clock Generator
P0	SW_CPLD_CONTROL_IN1		O	NA	NA	CPLD Switch Control Signals for Bootmode Logic
P1	SW_CPLD_CONTROL_IN2		O	NA	NA	CPLD Switch Control Signals for Bootmode Logic
P2	SW_CPLD_CONTROL_IN3		O	NA	NA	CPLD Switch Control Signals for Bootmode Logic
P3	SW_CPLD_CONTROL_IN4		O	NA	NA	CPLD Switch Control Signals for Bootmode Logic

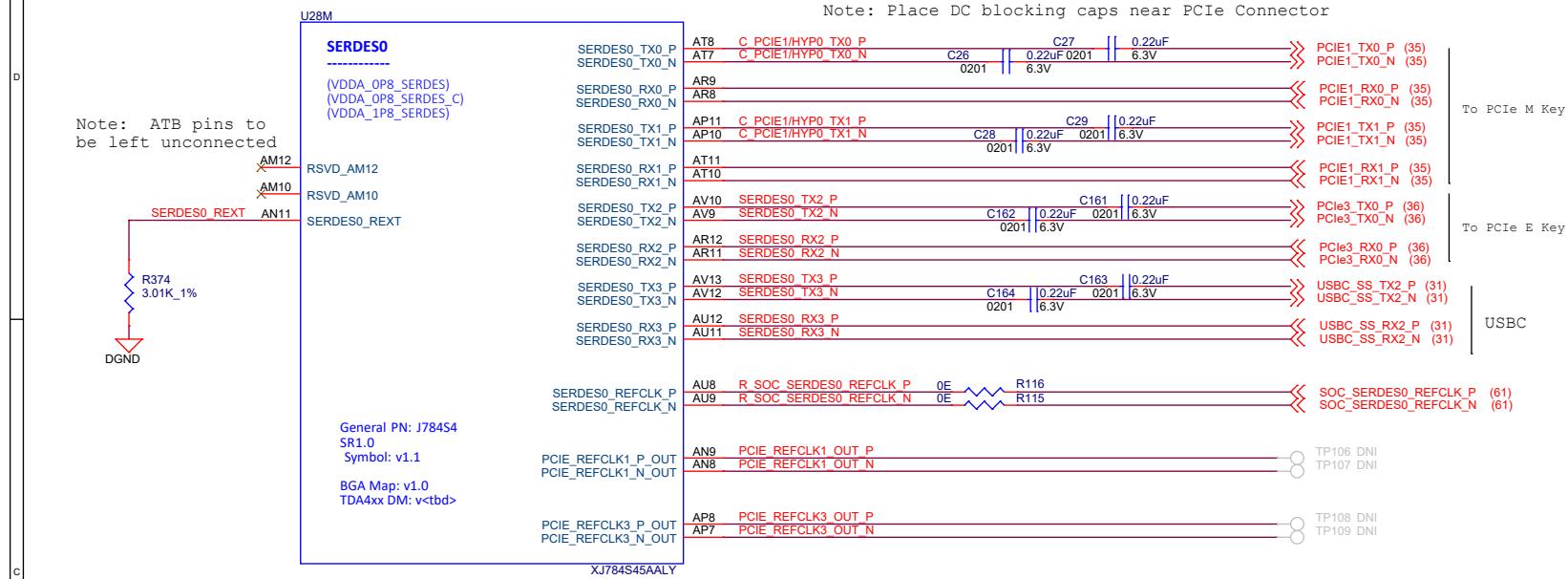
DSI



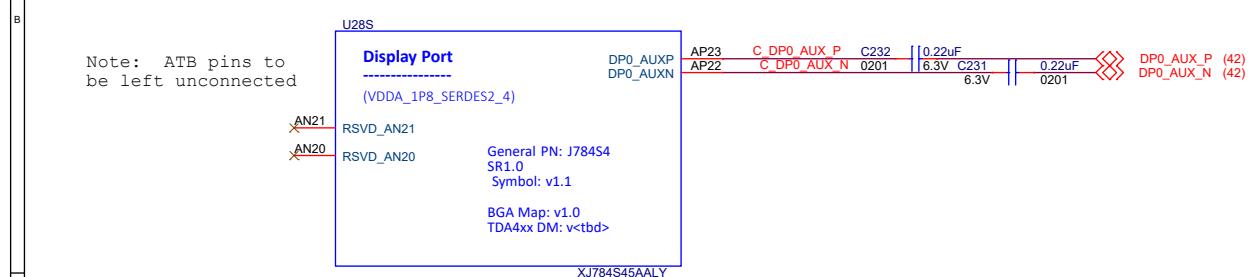
CSI



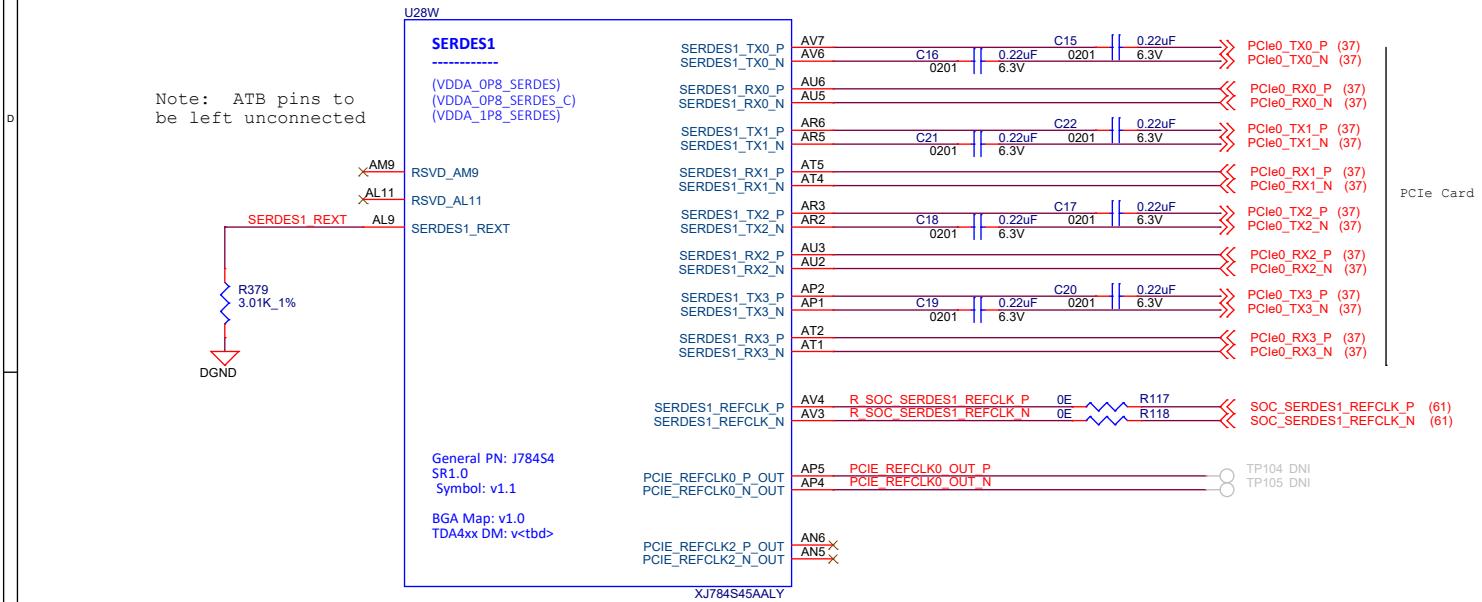
SERDES0



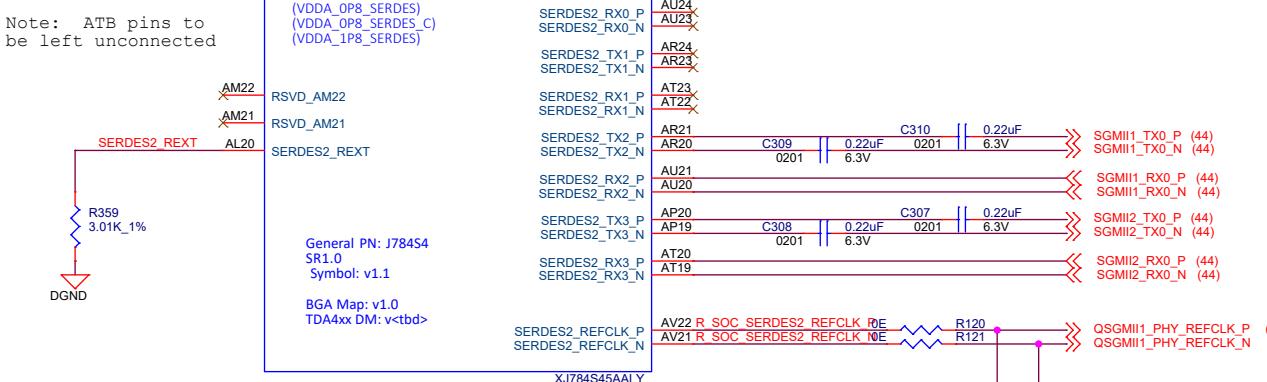
DP_AUX



SERDES1

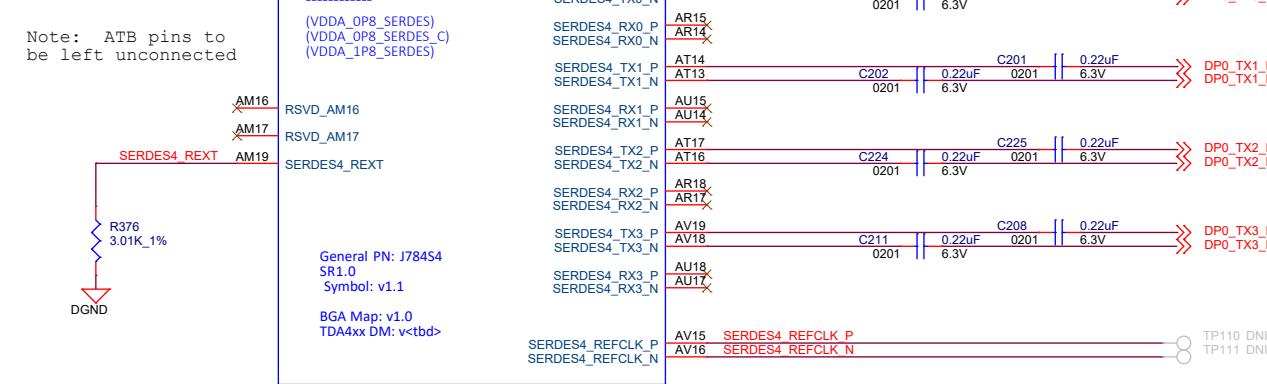


SERDES2

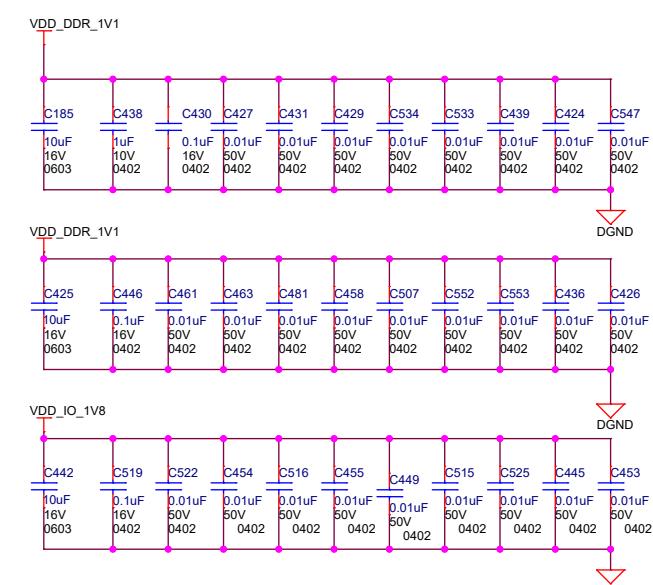
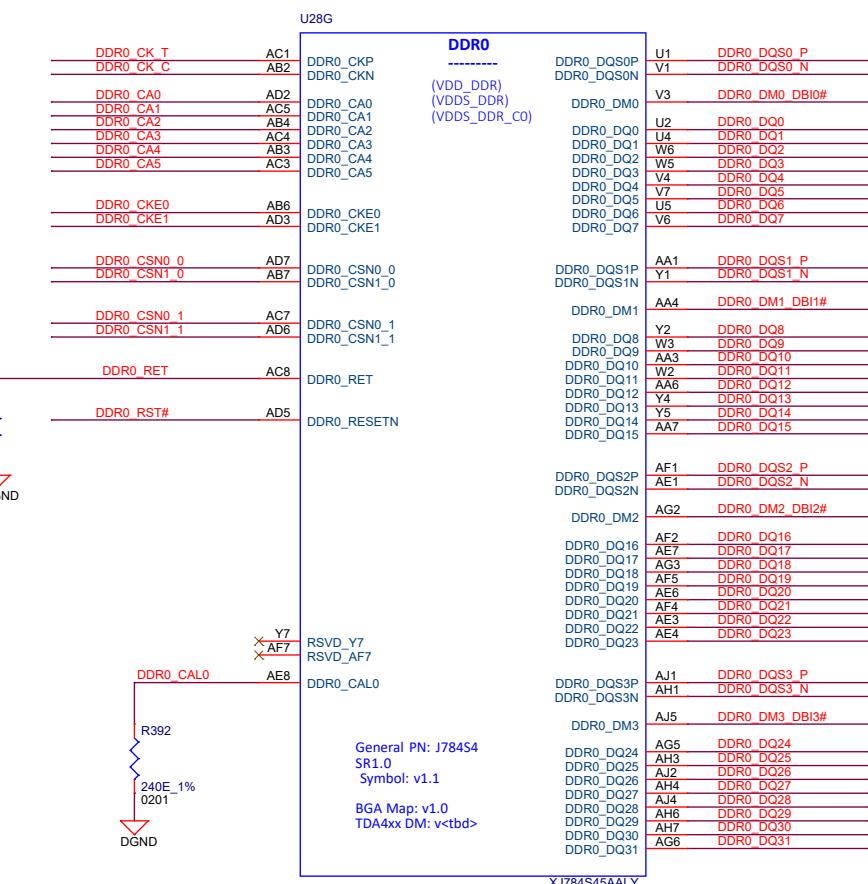
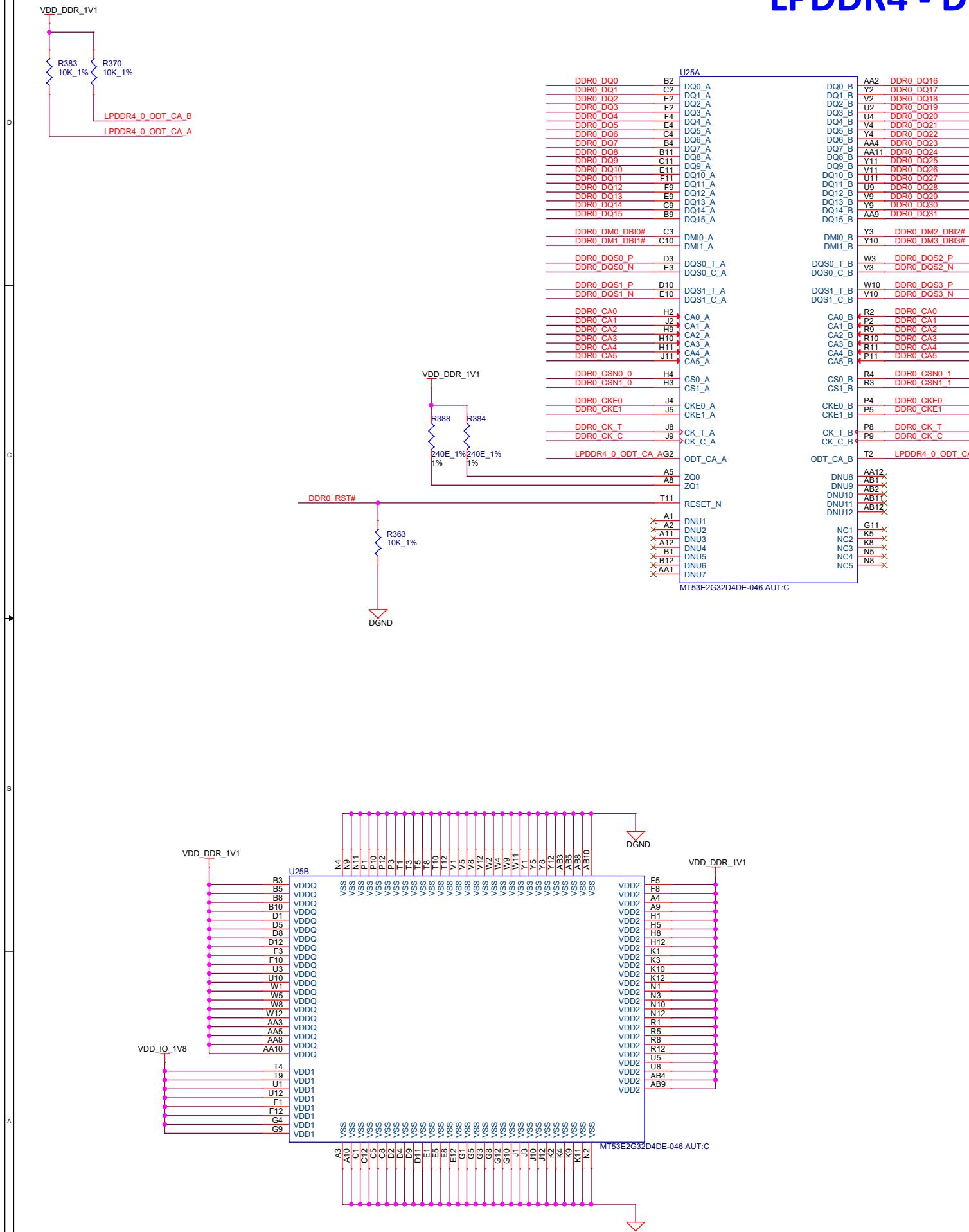


R109 49.9E_1%
R110 49.9E_1%
DGND

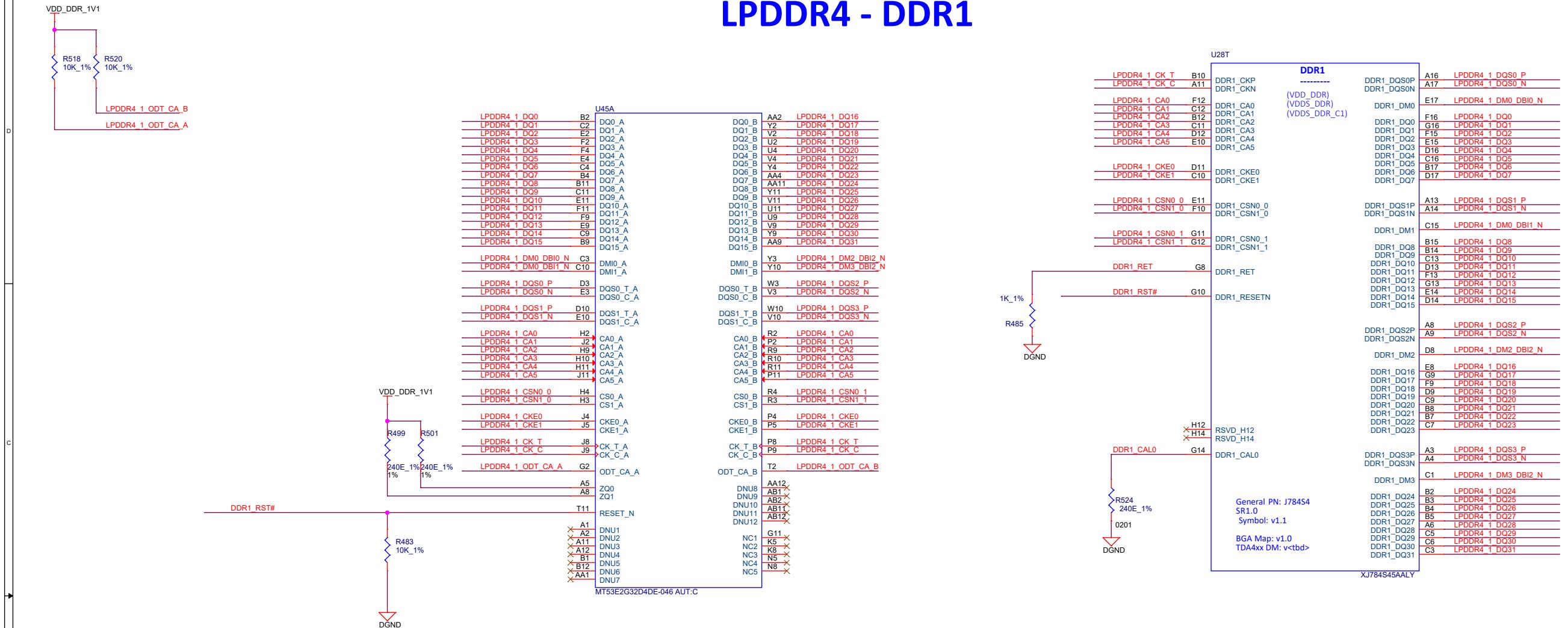
SERDES4



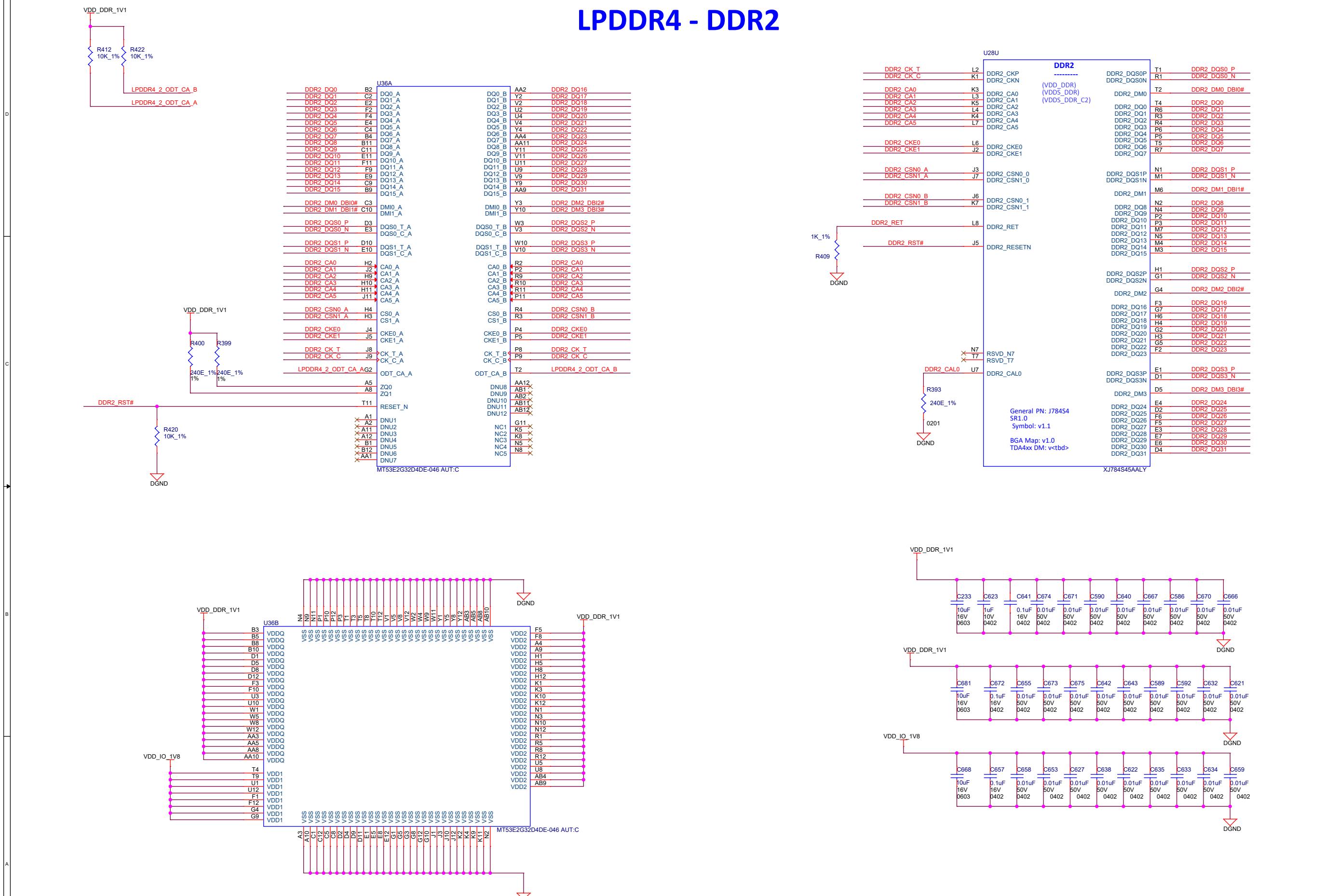
LPDDR4 - DDR0



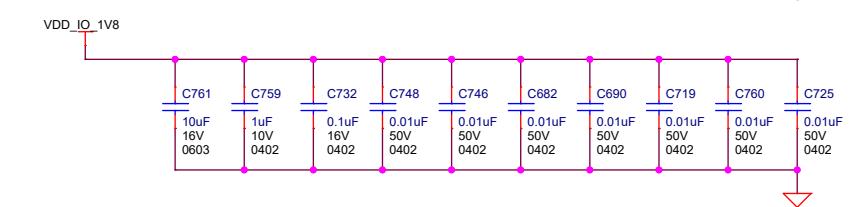
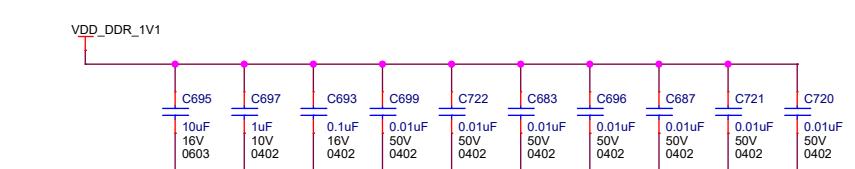
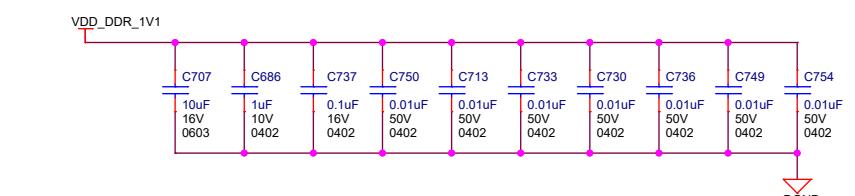
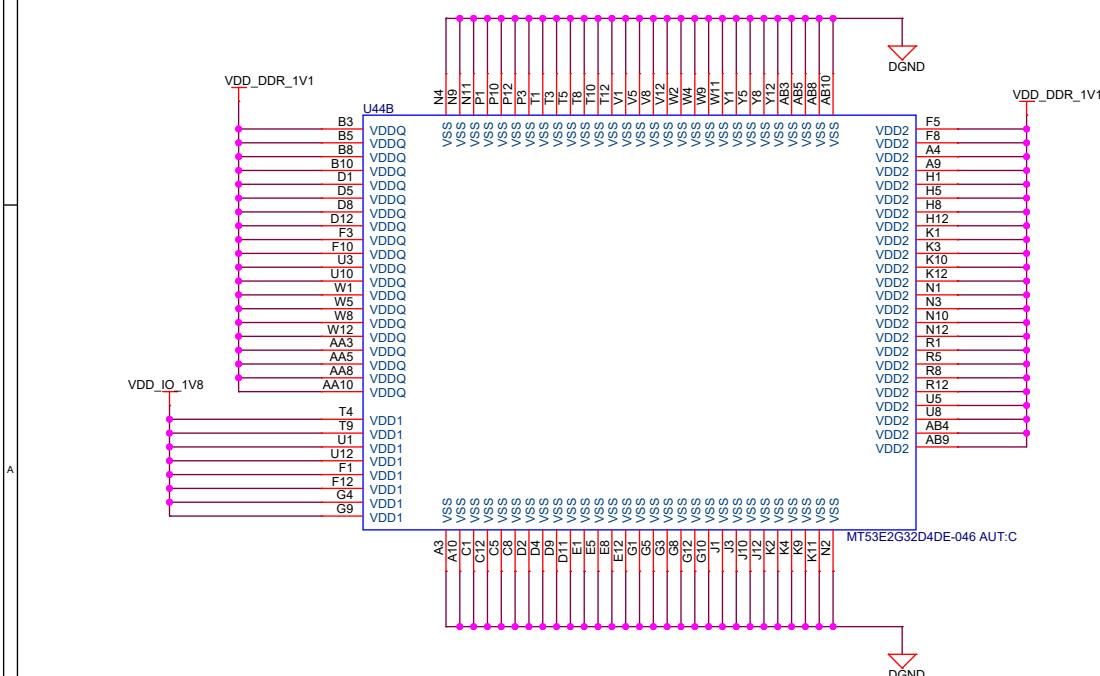
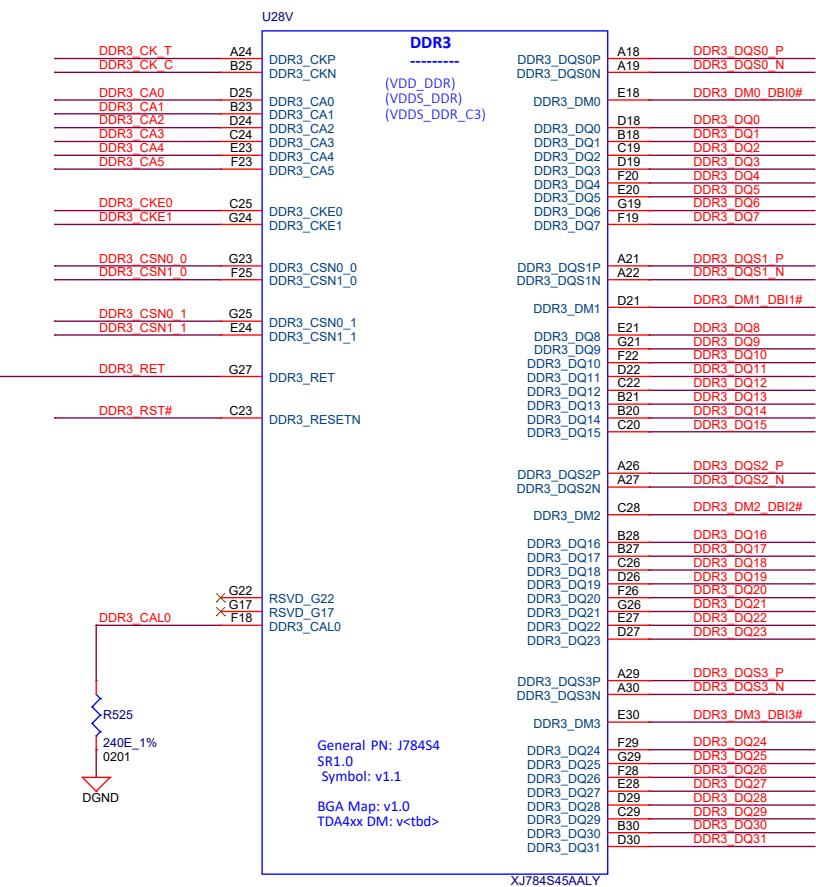
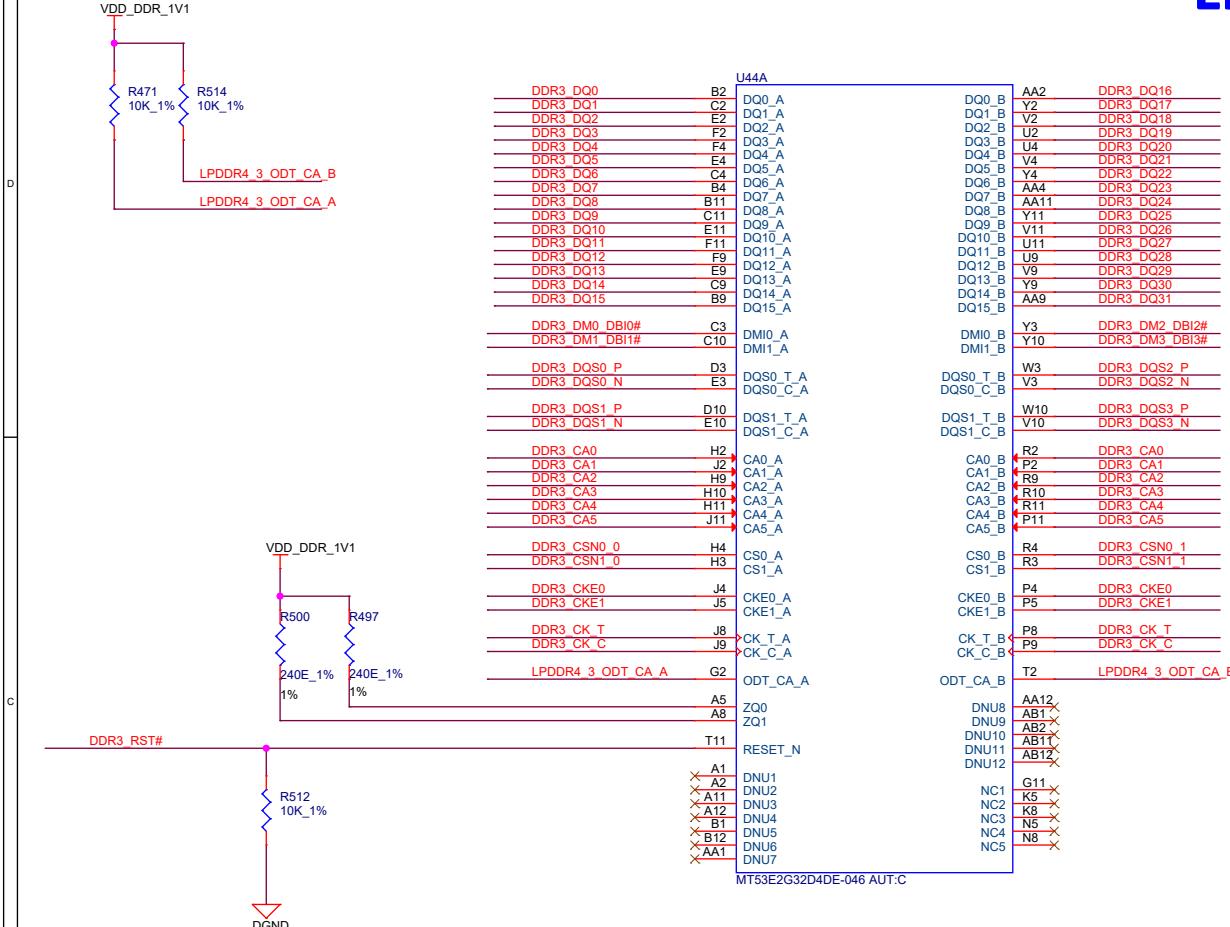
LPDDR4 - DDR1



LPDDR4 - DDR2

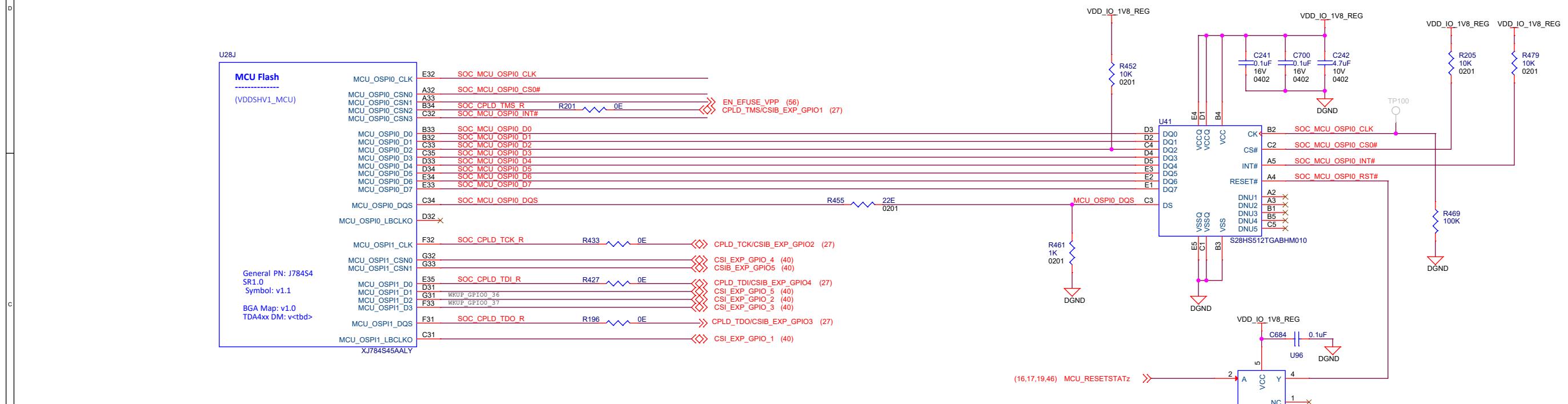


LPDDR4 - DDR3



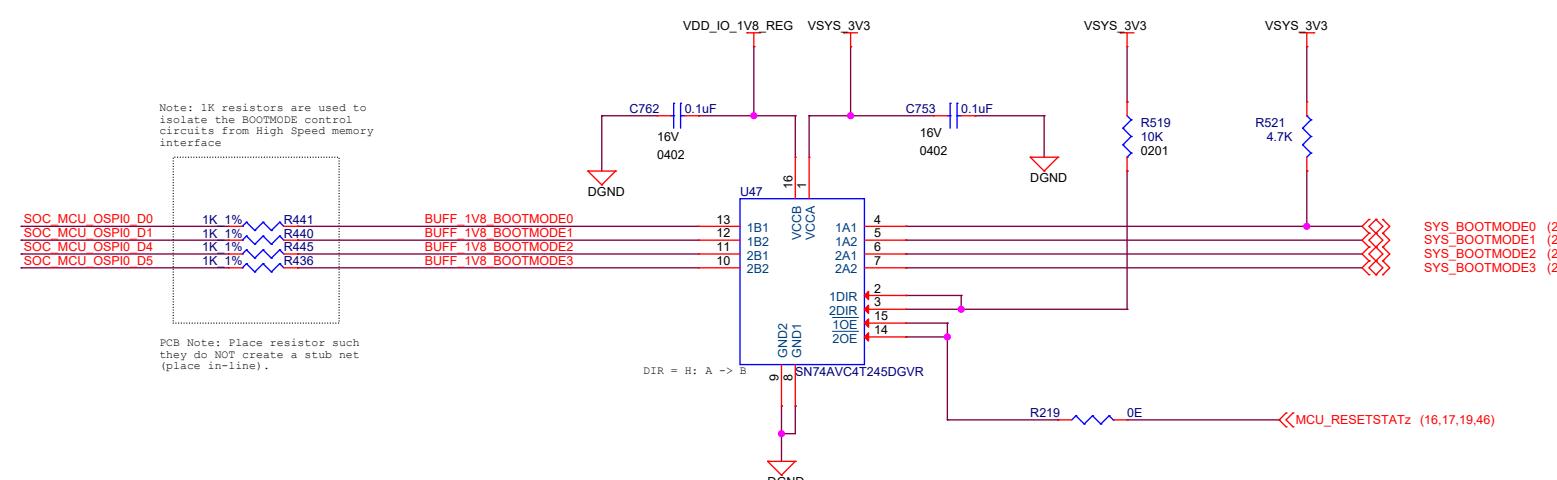
MCU FLASH

OSPI FLASH

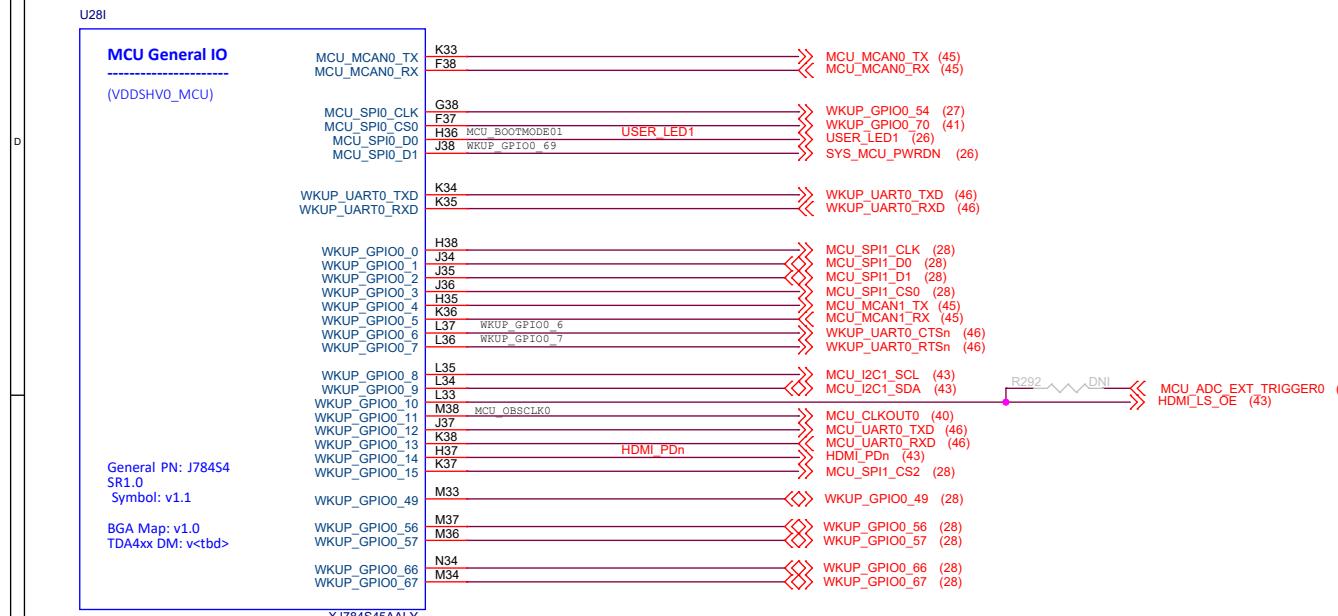


BOOTMODE Control Logic

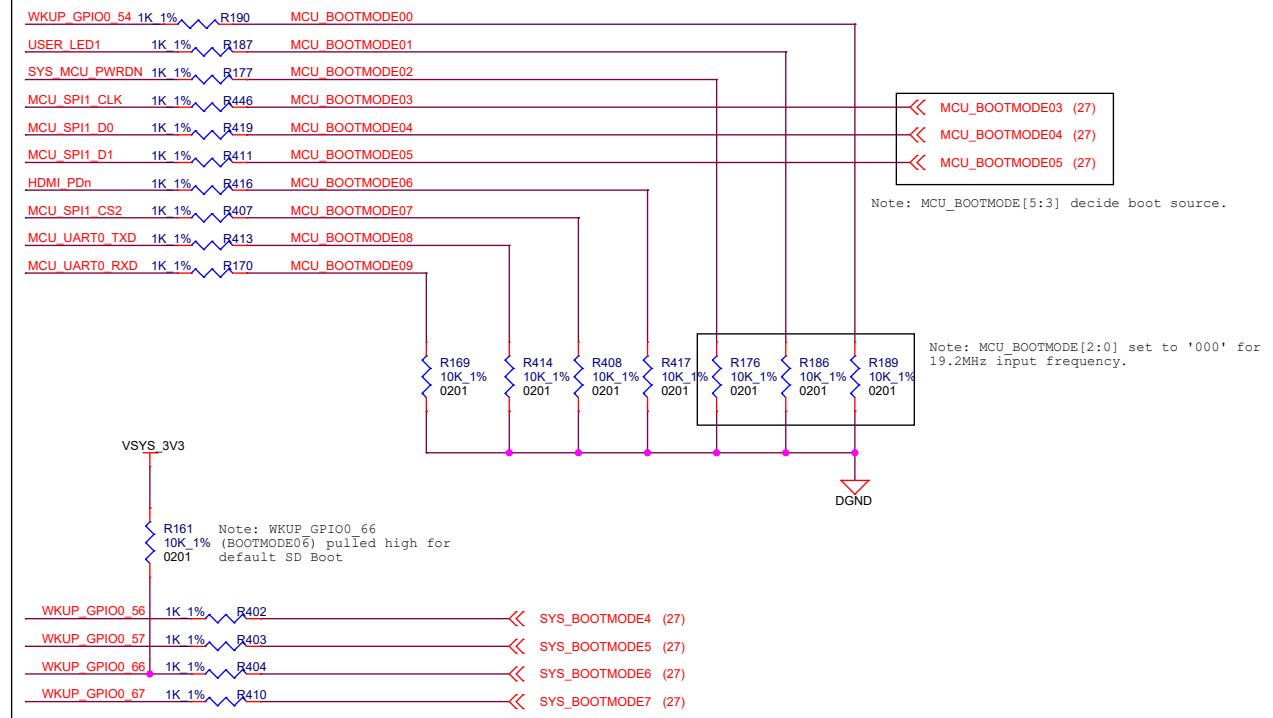
Note: Logic used to configure BOOTMODE settings during reset. This is four (4) of a total of eighteen (18) boot pins. Specific value is user configured (dip switch).



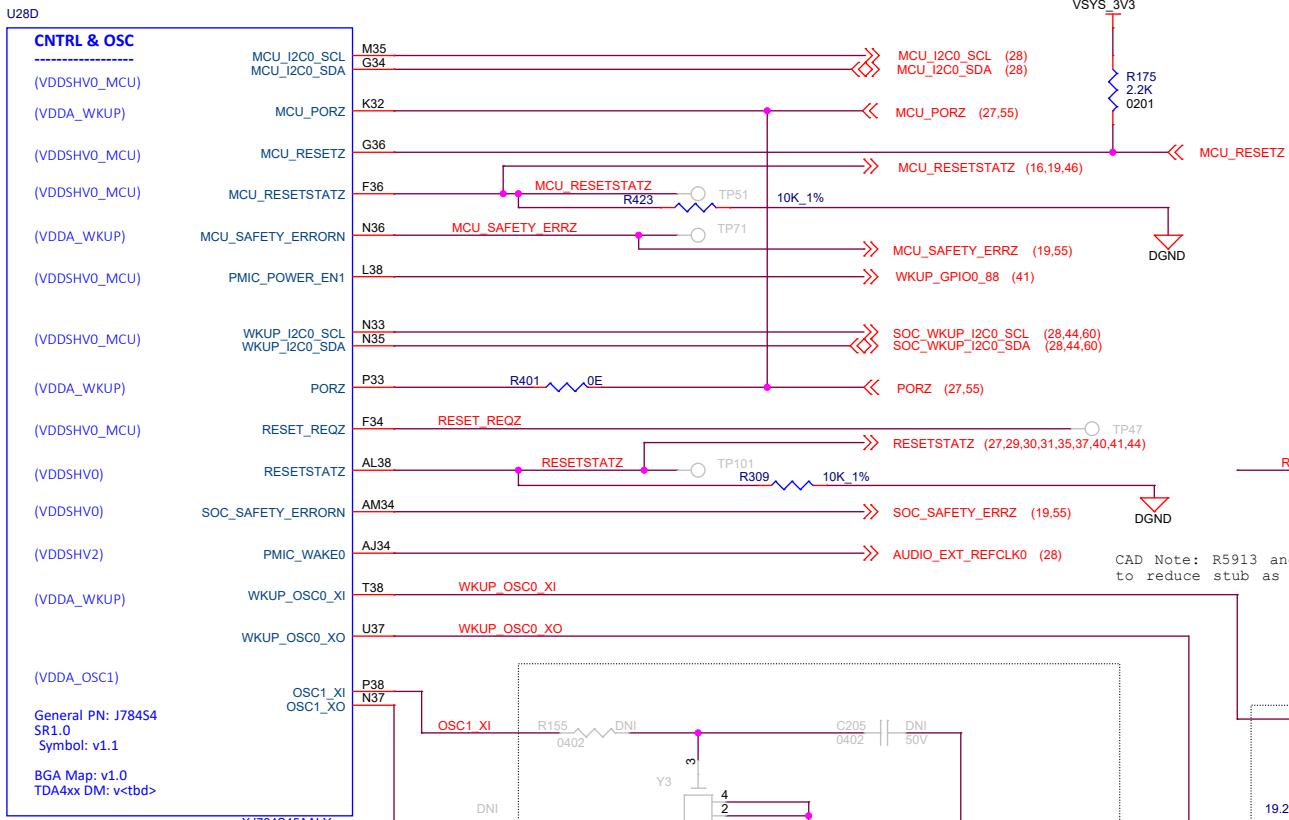
MCU & MAIN GENERAL IO, OSC CLKS



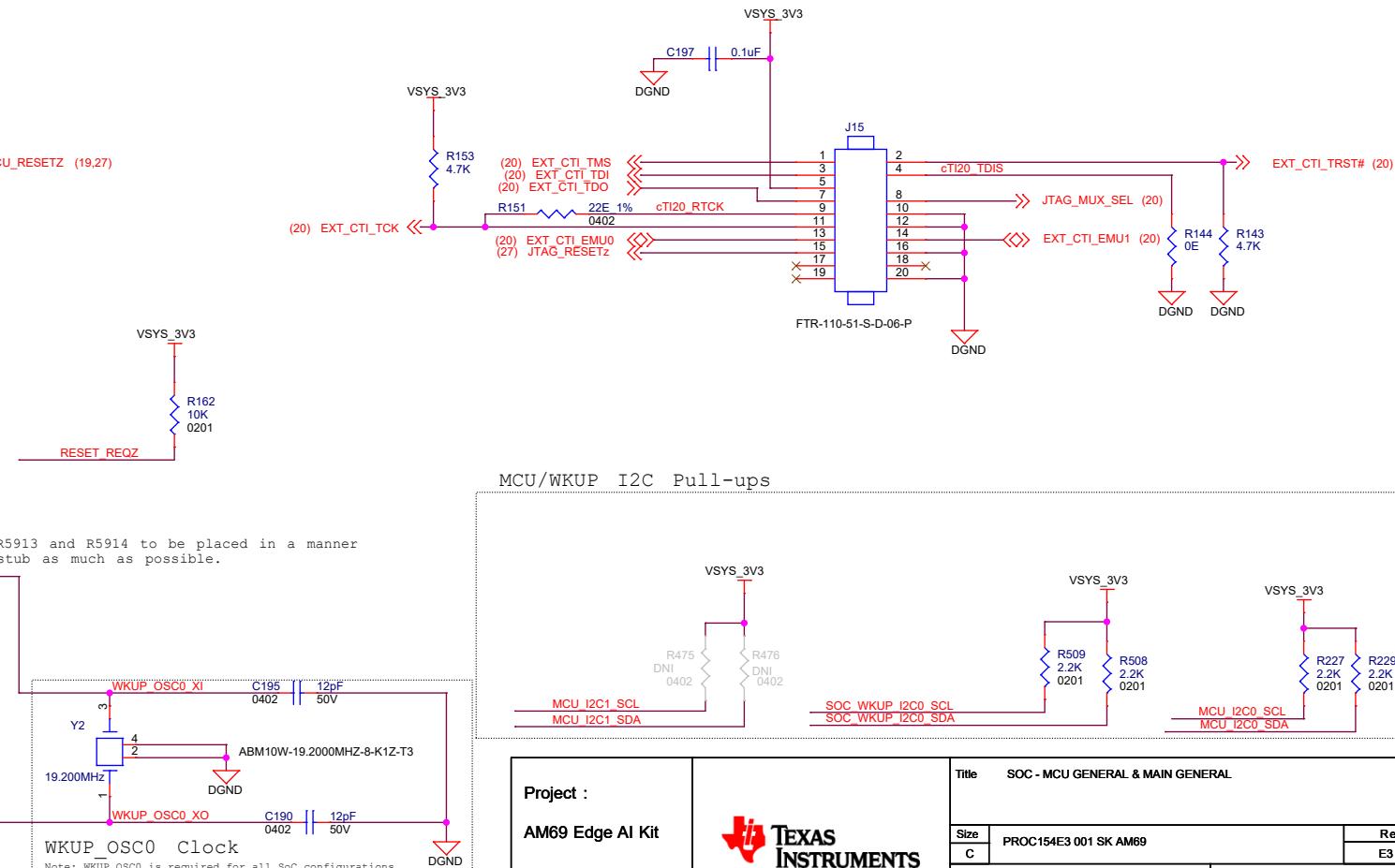
BOOTMODE



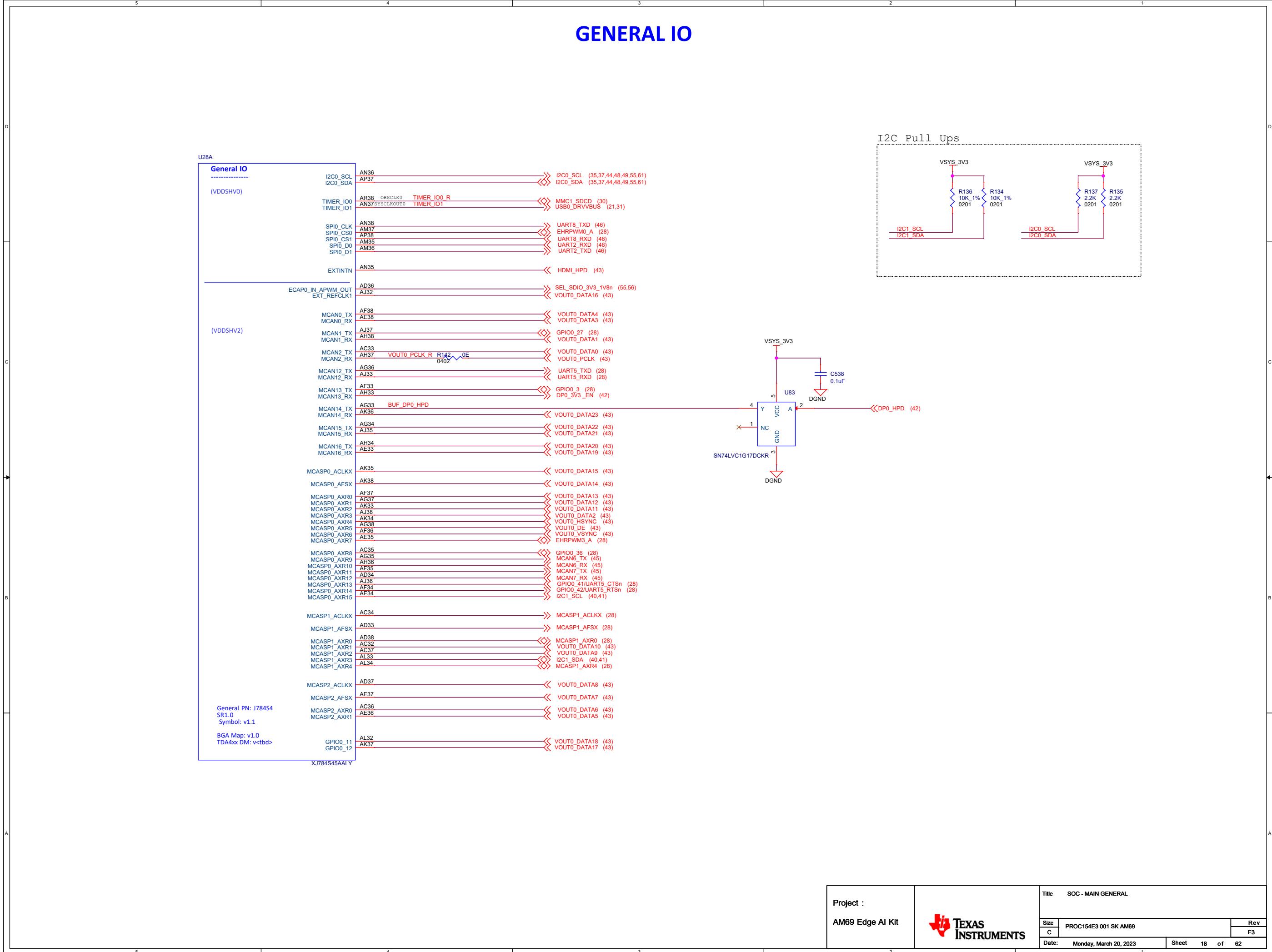
CONTROL & OSC



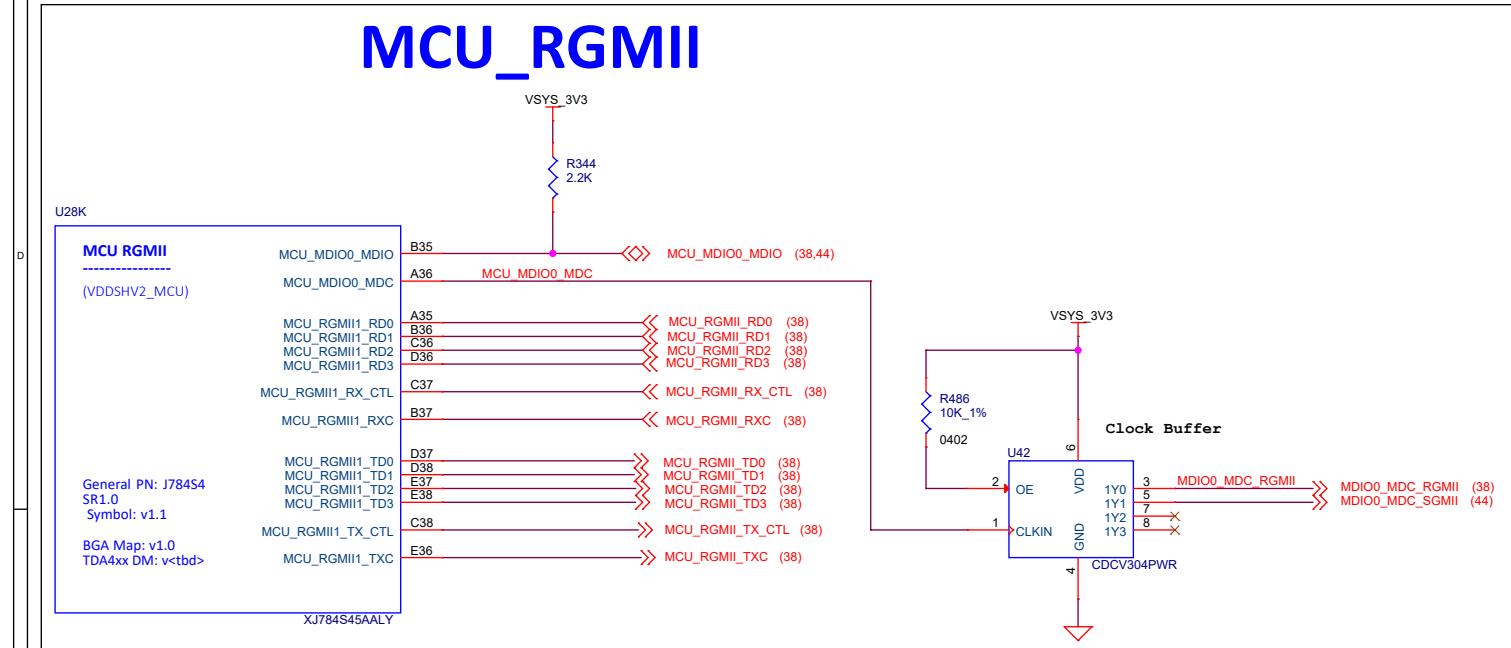
cTI 20PIN JTAG HEADER



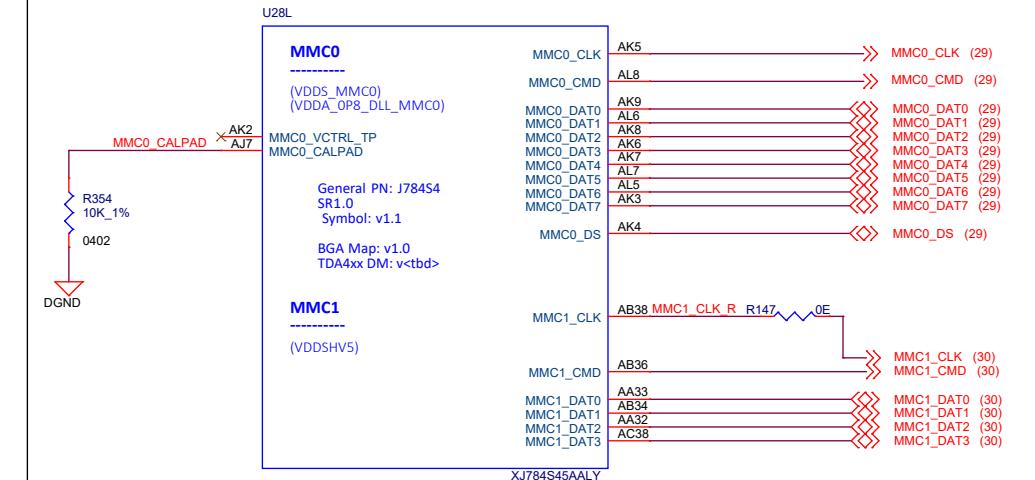
GENERAL IO



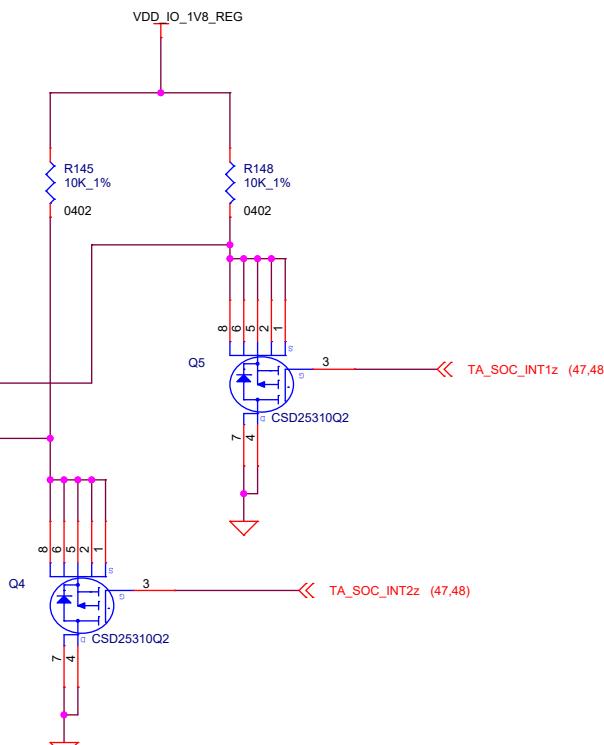
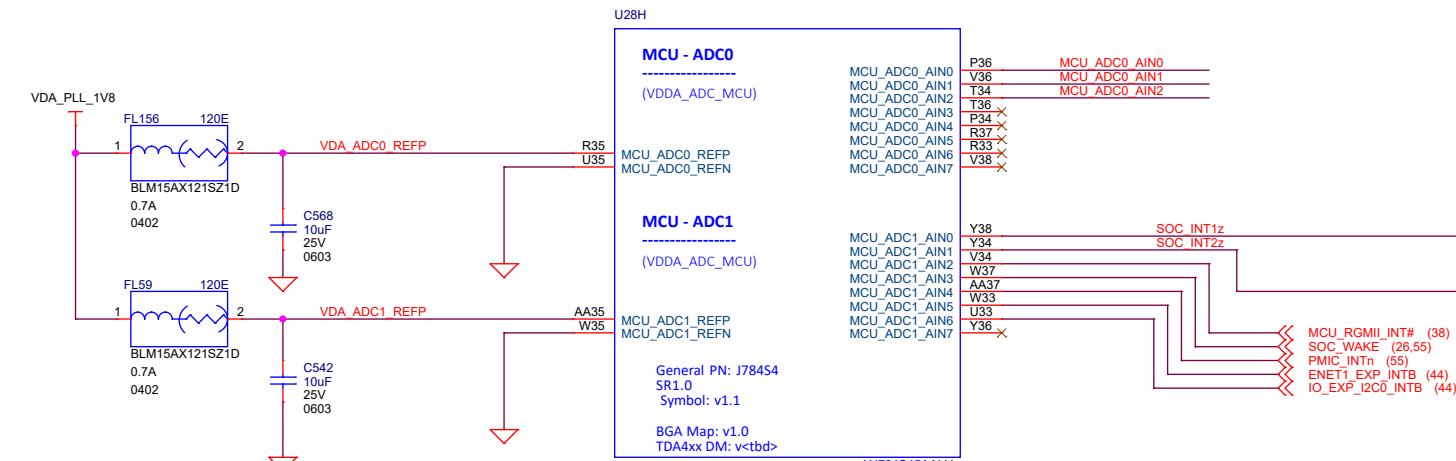
MCU_RGMII



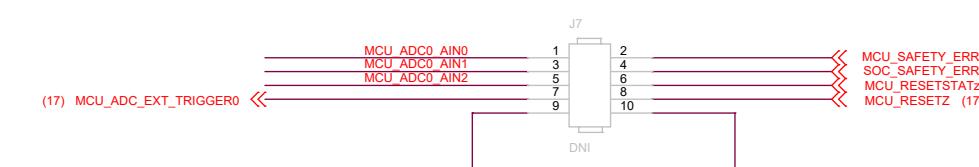
MMC0 and MMC1



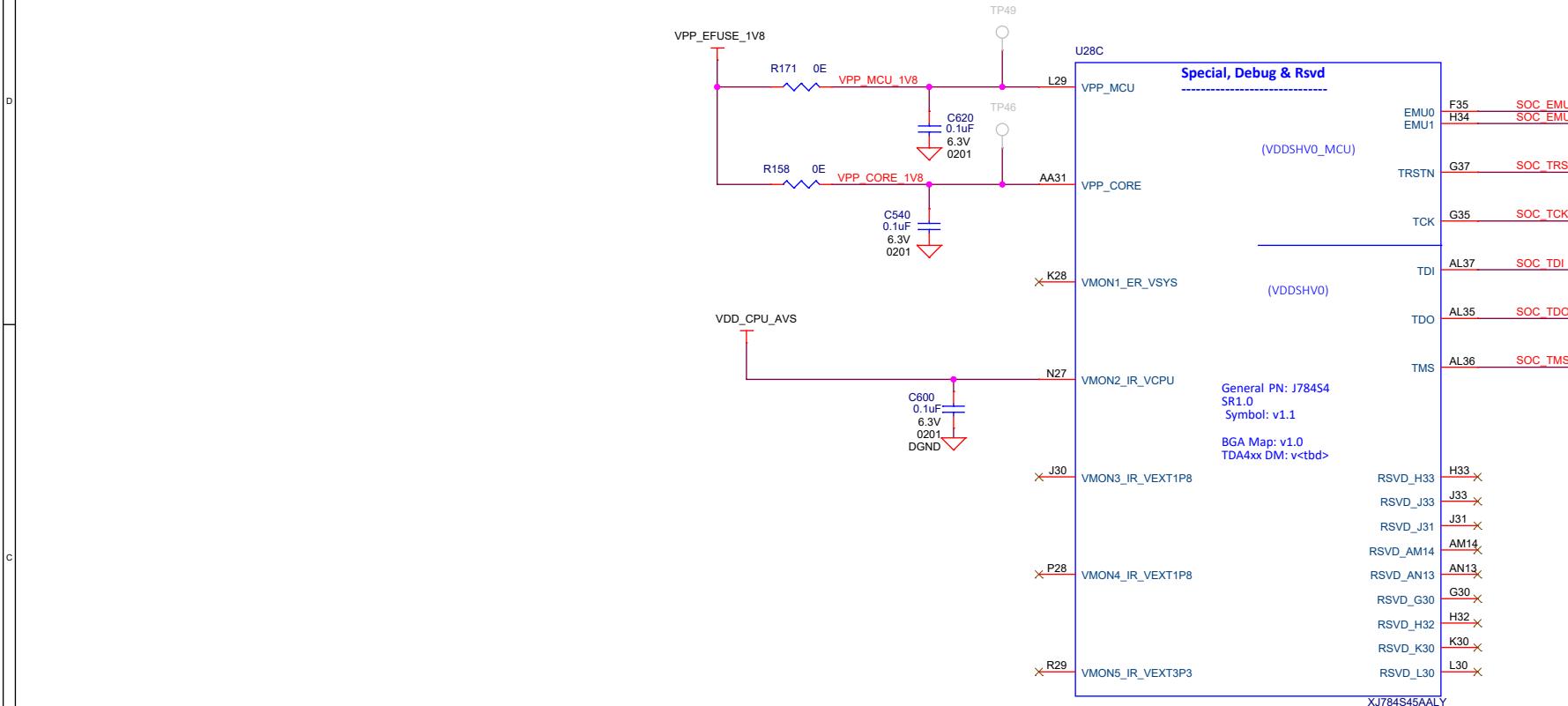
MCU_ADC



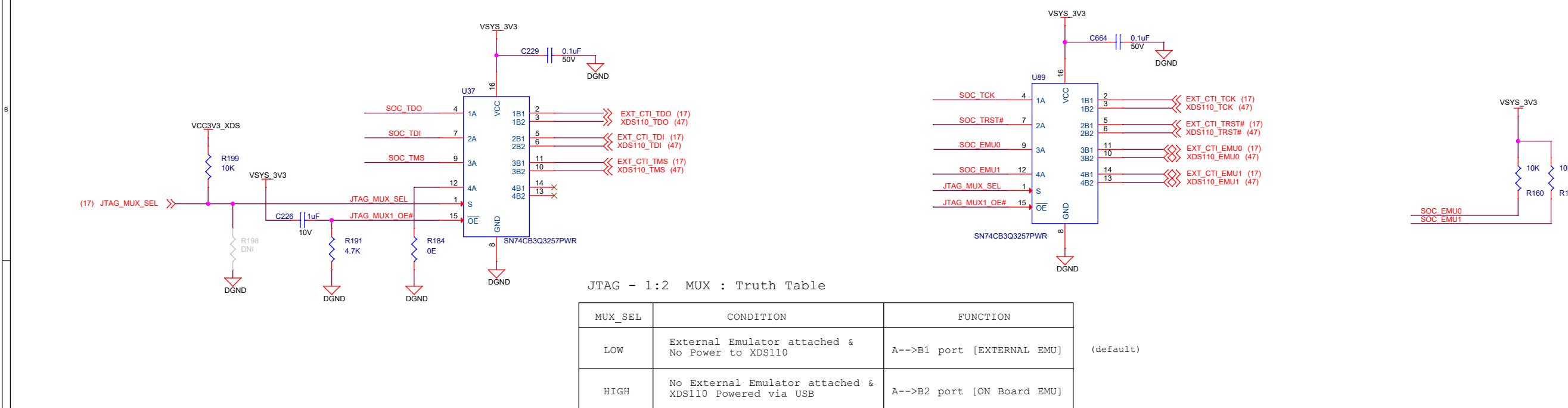
SAFETY STATUS INTERFACE



SPECIAL, DEBUG & RSVD

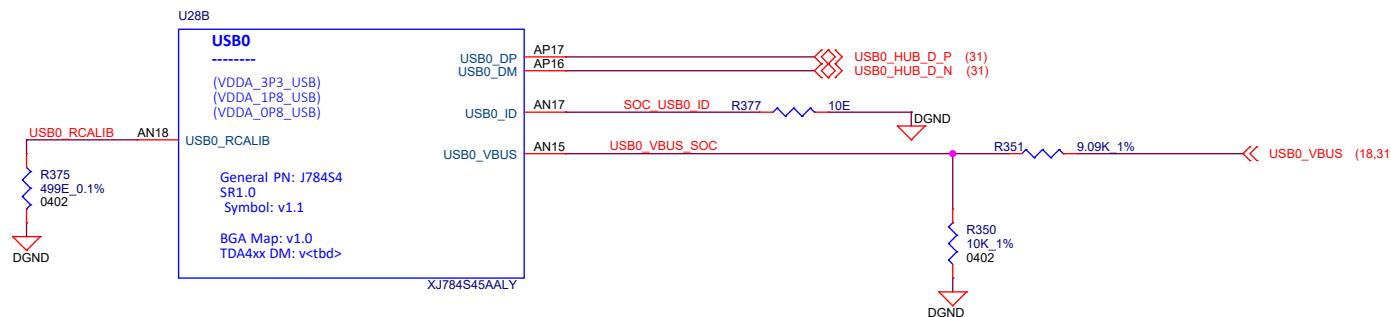


JTAG CONNECTOR AND XDS110 MUX

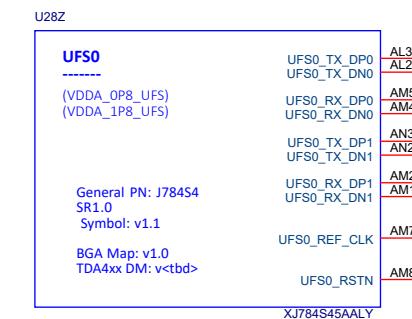


USBO 2.0

USB VBUS Resistor divider circuit



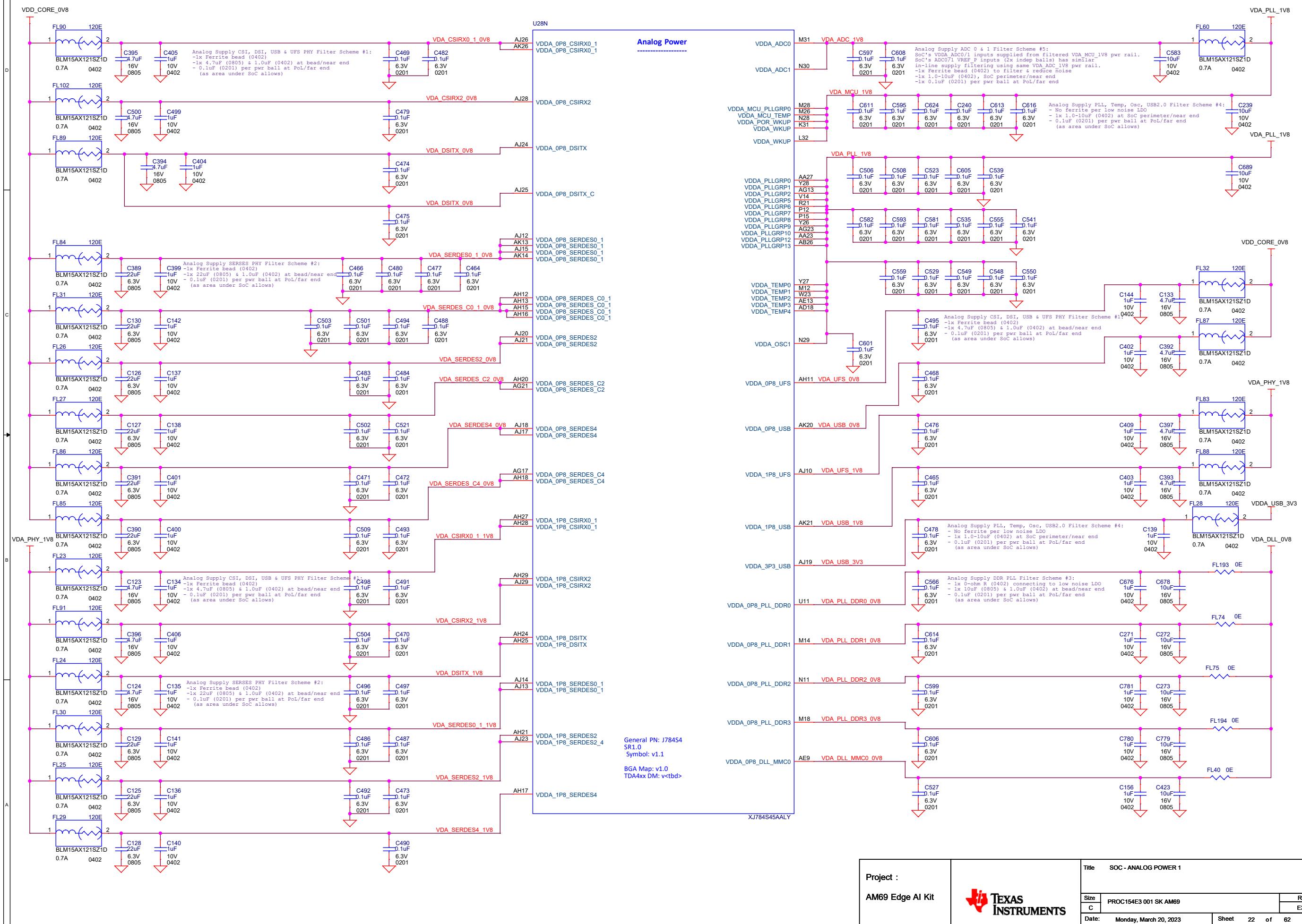
UFS FLASH



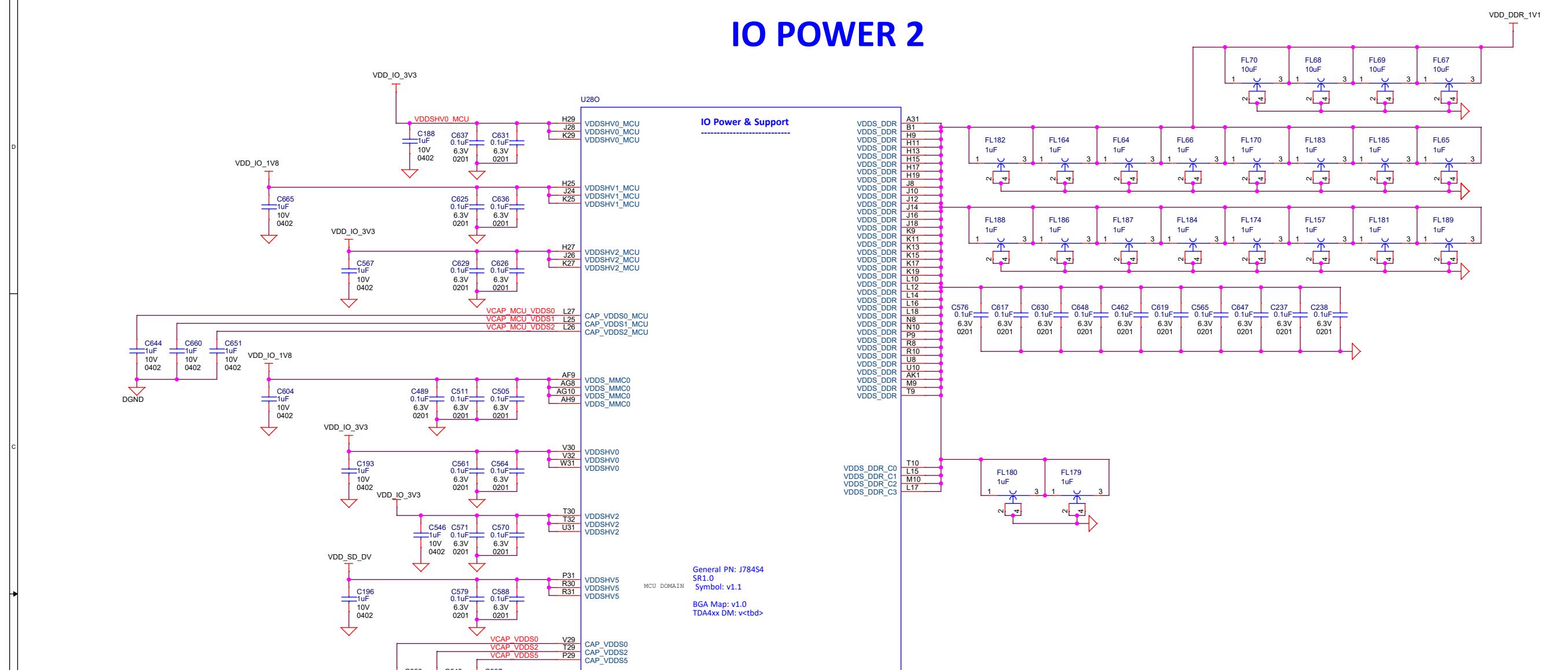
Project :	AM69 Edge AI Kit	Title SOC - USB 2.0
Size	PROC154E3 001 SK AM69	Rev
C	E3	
Date:	Monday, March 20, 2023	Sheet 21 of 62

TEXAS
INSTRUMENTS

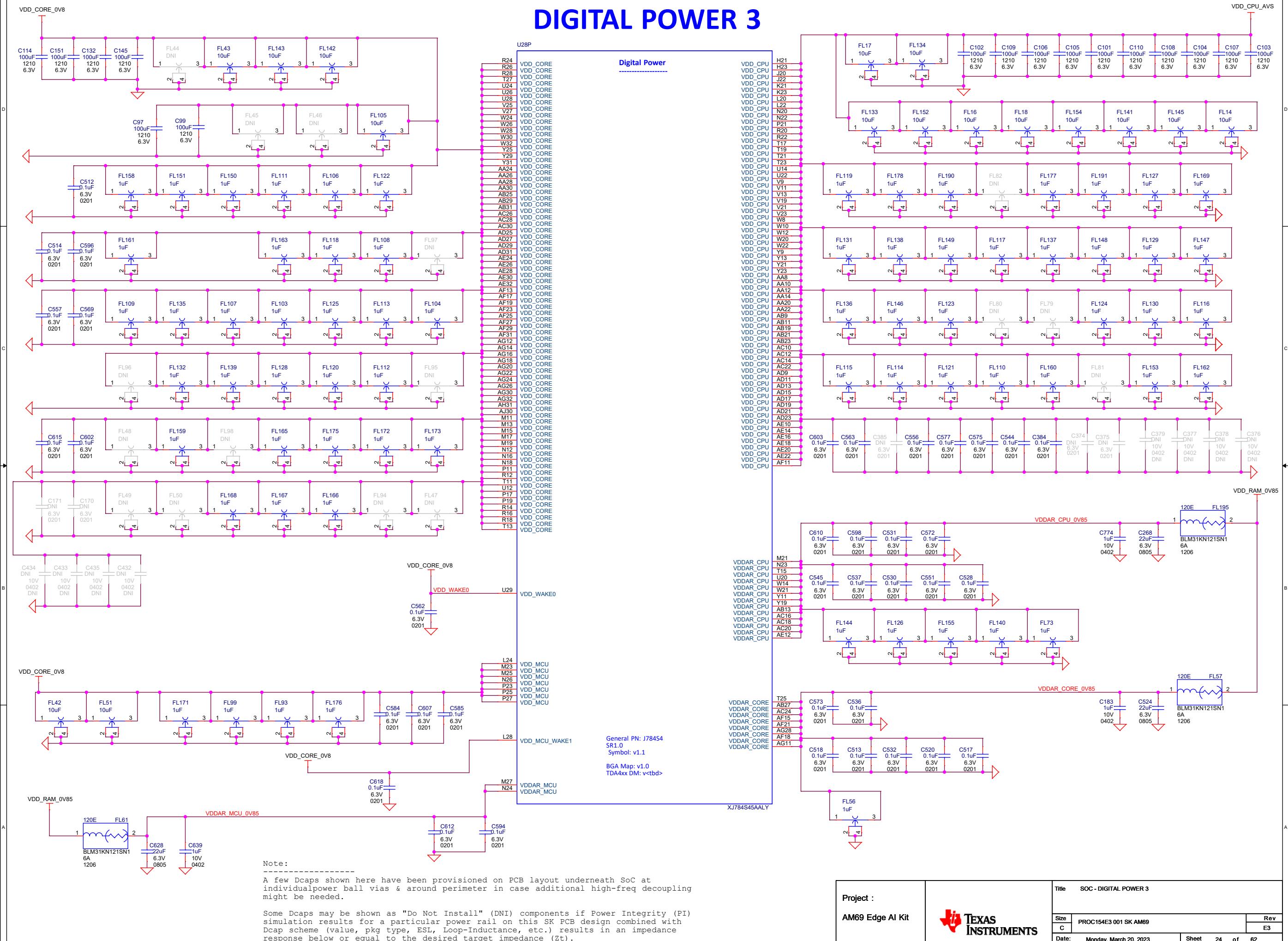
ANALOG POWER 1



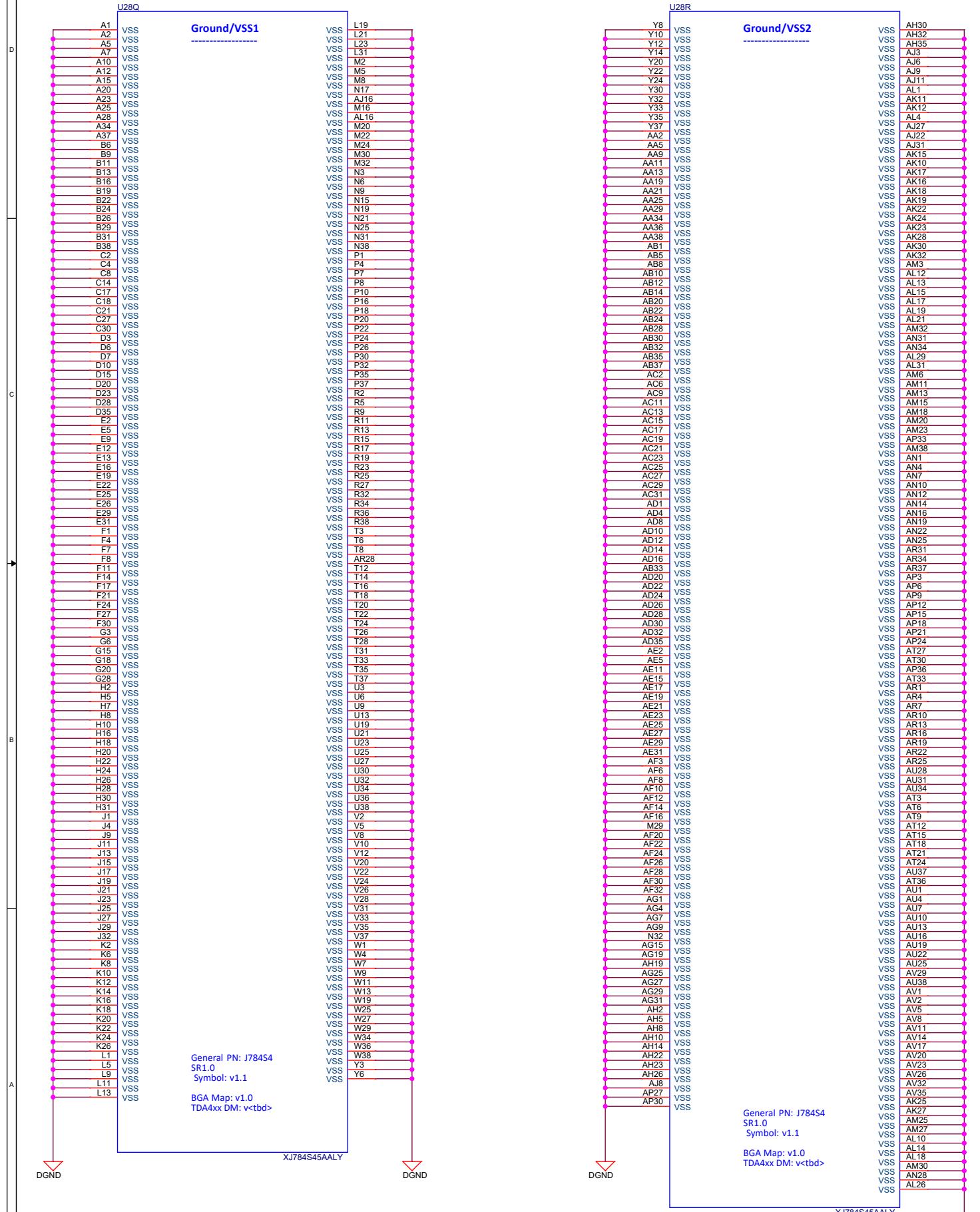
IO POWER 2



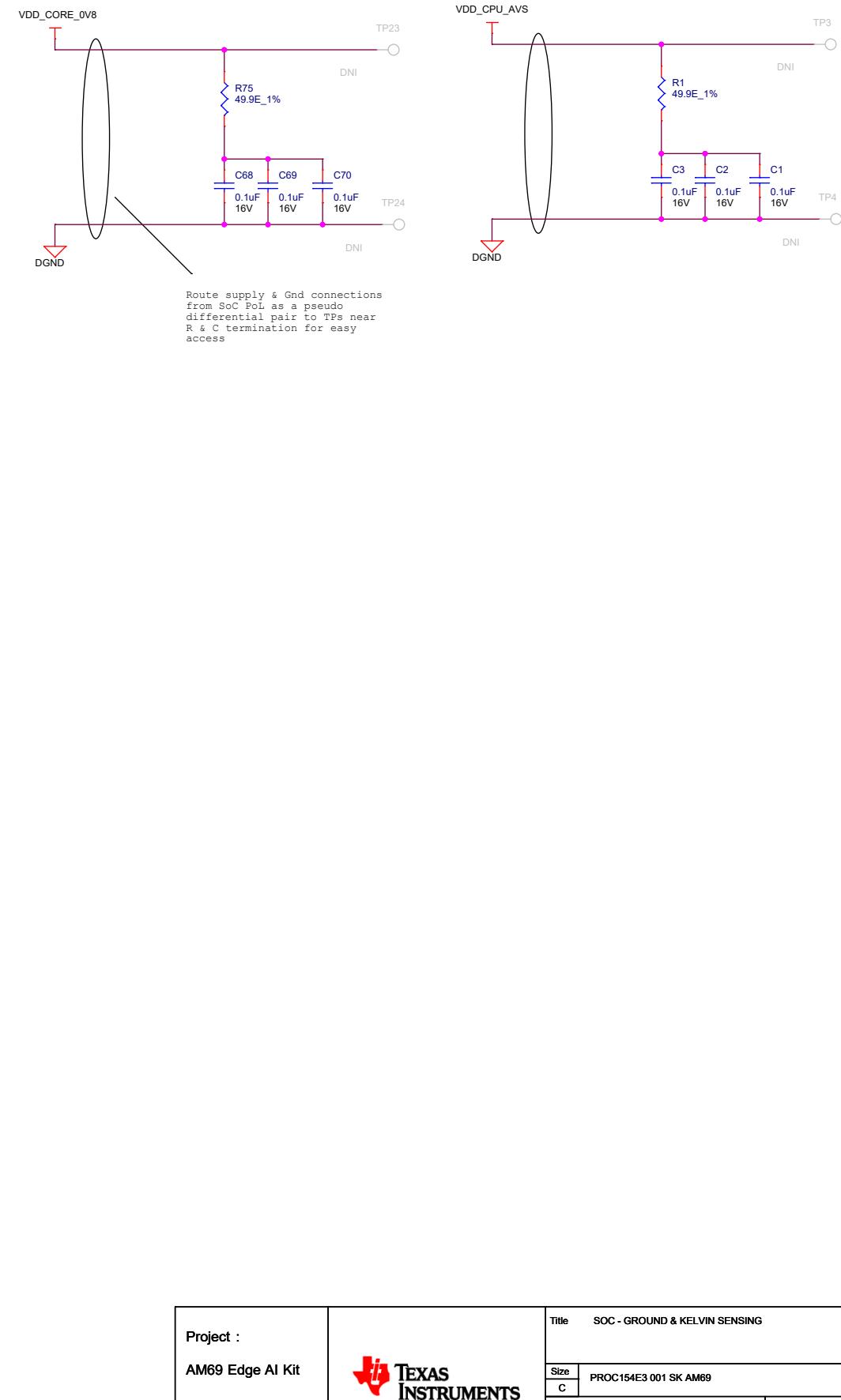
DIGITAL POWER 3



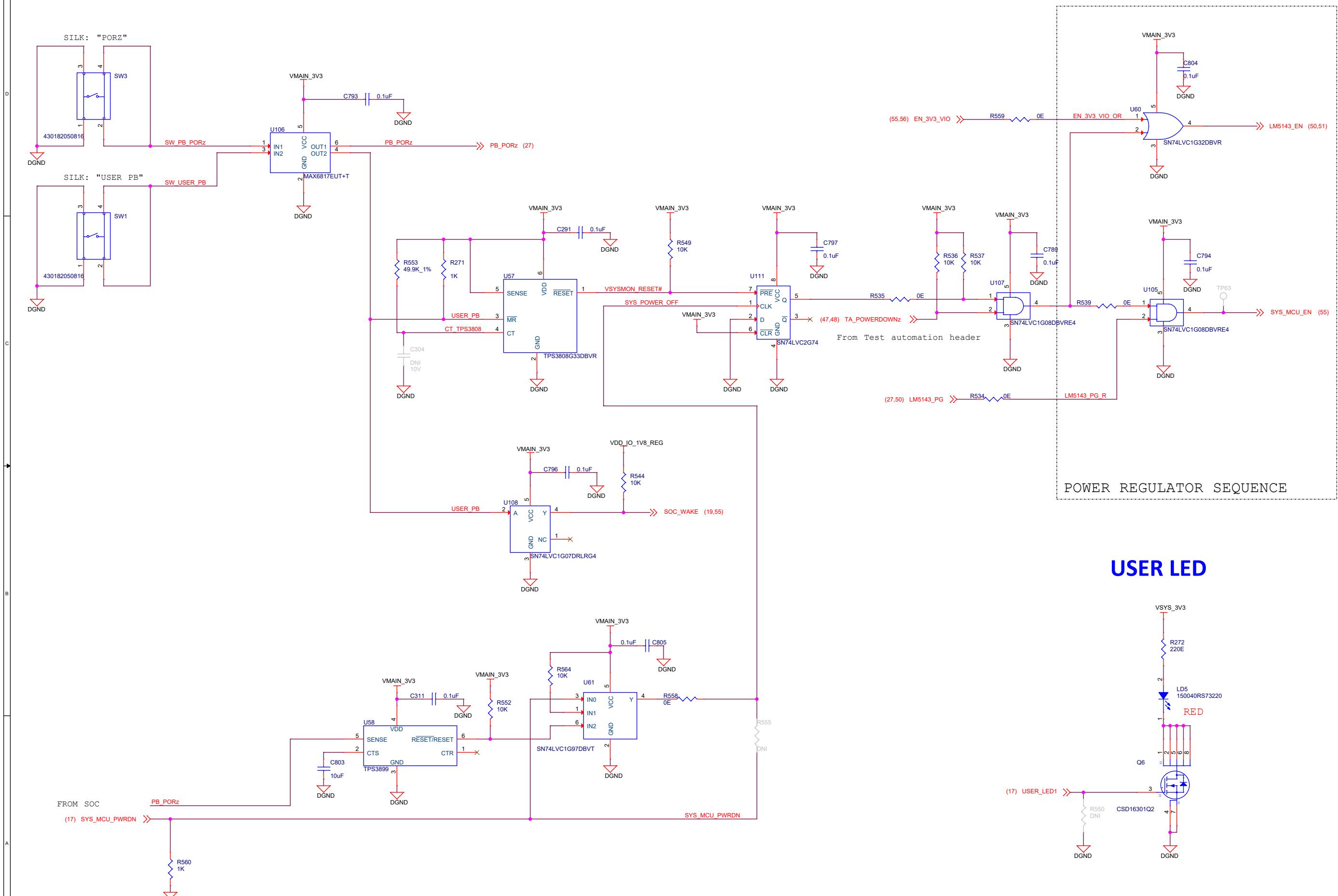
SOC GROUND



SoC Supply Noise Kelvin Sensing



RESET BUTTONs



Project :

 TEXAS
INSTRUMENTS

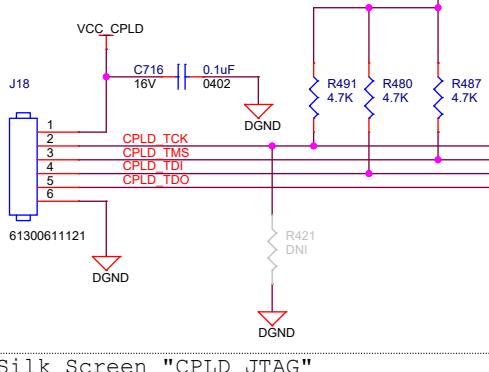
RESET BUTTONs

ze	PROC154E3 001 SK AM69	Rev
C		E3
ate:	Monday, March 20, 2023	Sheet 26 of 62

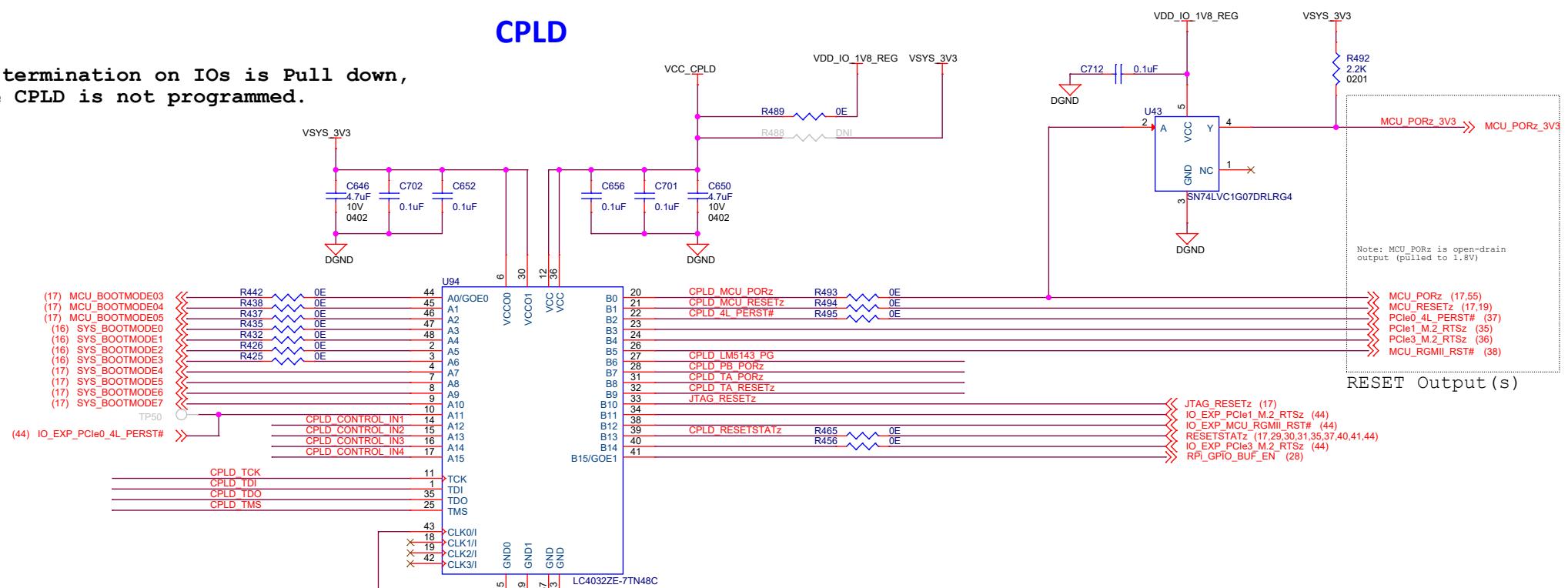
CPLD

Default termination on IOs is Pull down, when the CPLD is not programmed.

PROGRAMMING HEADER



Silk Screen "CPLD JTAG"



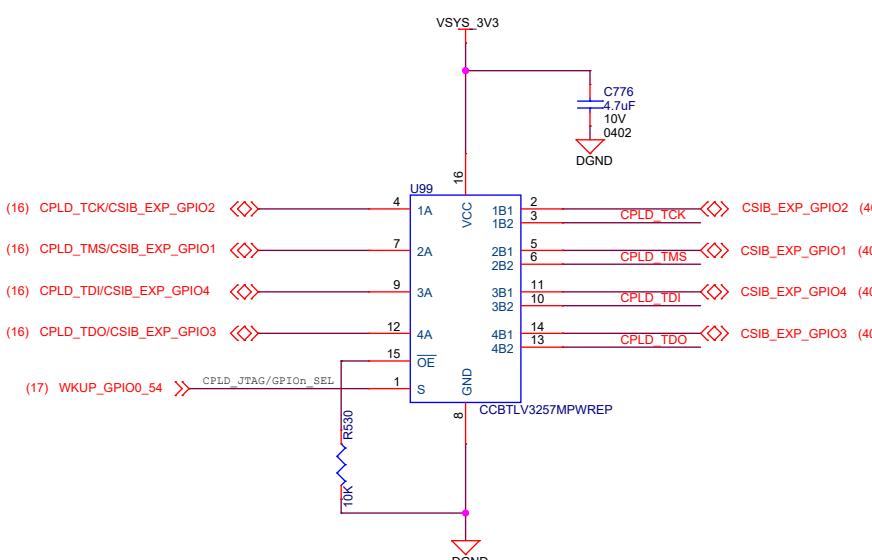
Note: MCU_PORz is open-drain output (pulled to 1.8V)

- MCU_PORz (17.55)
- MCU_RESETz (17.19)
- PCIe0_4L_PERST# (37)
- PCIe1_M2_RTsz (35)
- PCIe3_M2_RTsz (36)
- MCU_RGMI_RST# (38)

RESET Output(s)

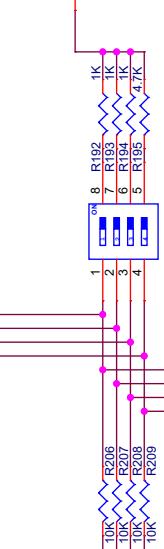
TP53

MCU_PORz_3V3



Test Automation BOOTMODE Logic

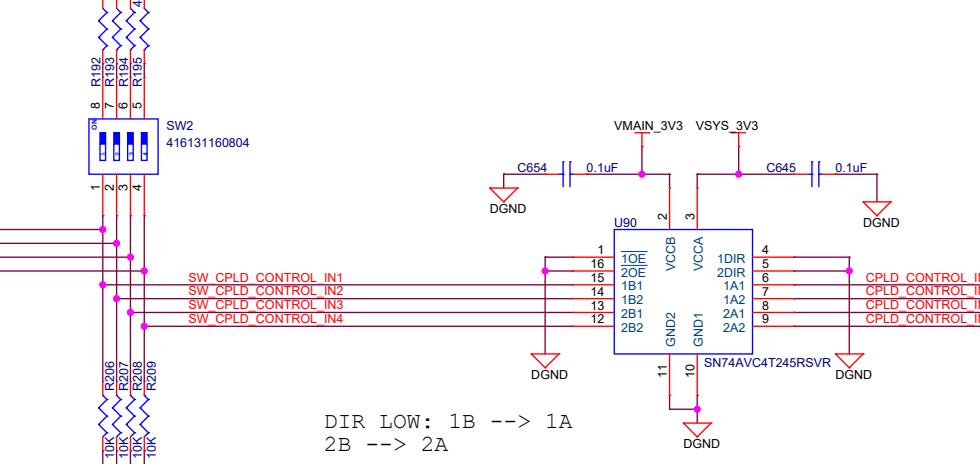
Note: Test Automation logic to set desired BOOTMODE.



DIR LOW: 1B --> 1A
2B --> 2A

I2C ADDRESS: 0x20

SW2.3	SW2.2	SW2.1	BOOTMODE
0	0	0	SD
0	0	1	NO Boot
0	1	0	Ethernet
0	1	1	USB
1	0	0	xSPI - 1S
1	0	1	UART
1	1	0	eMMC
1	1	1	xSPI SFDP



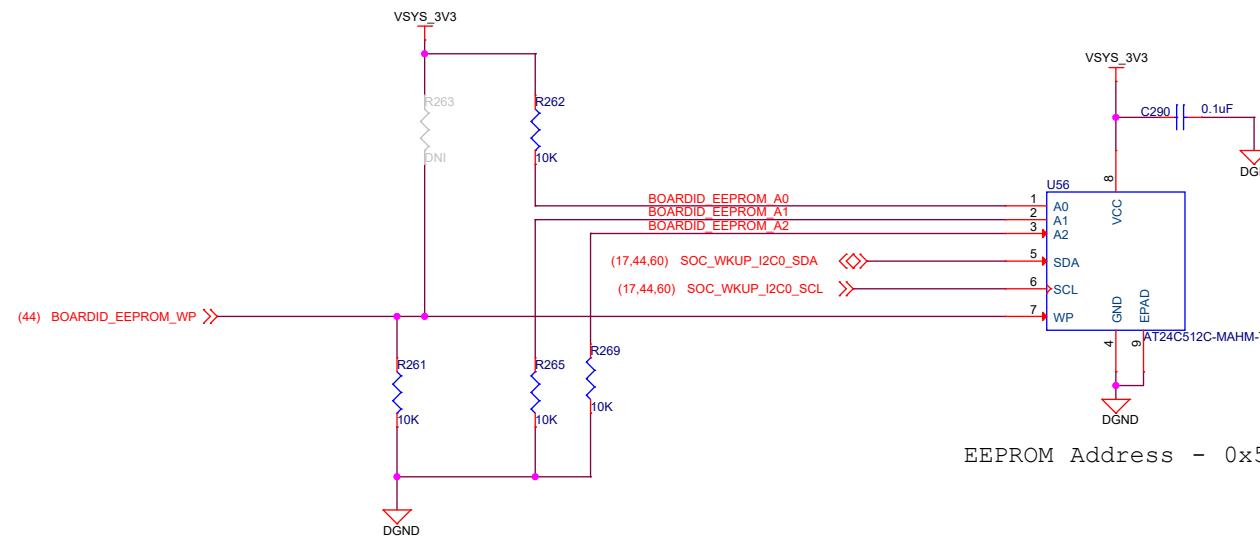
DIR LOW: 1B --> 1A
2B --> 2A

Project : AM69 Edge AI Kit

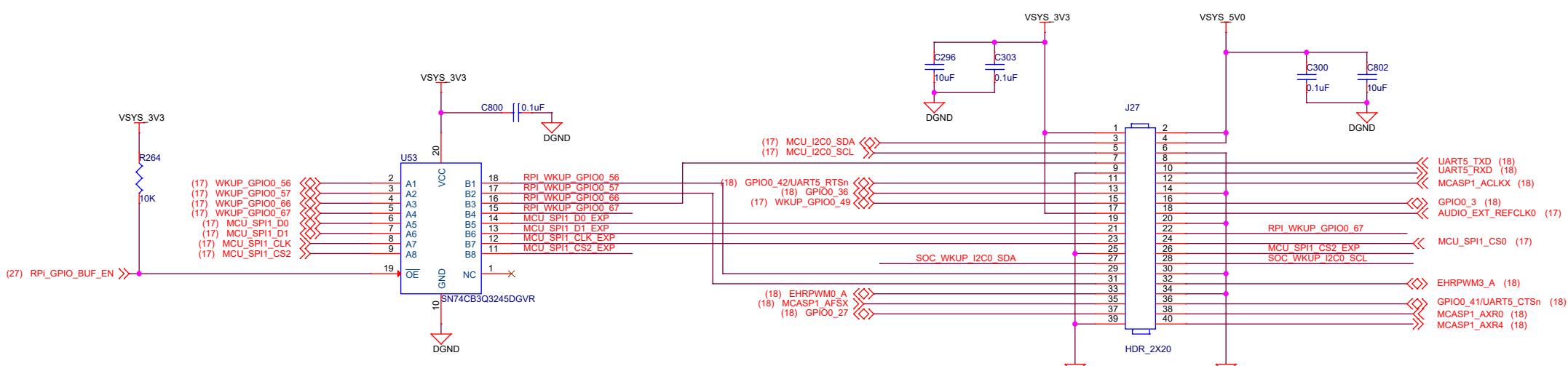


Title CPLD
Size C PROC154E3 001 SK AM69
Rev E3
Date: Wednesday, May 03, 2023 Sheet 27 of 62

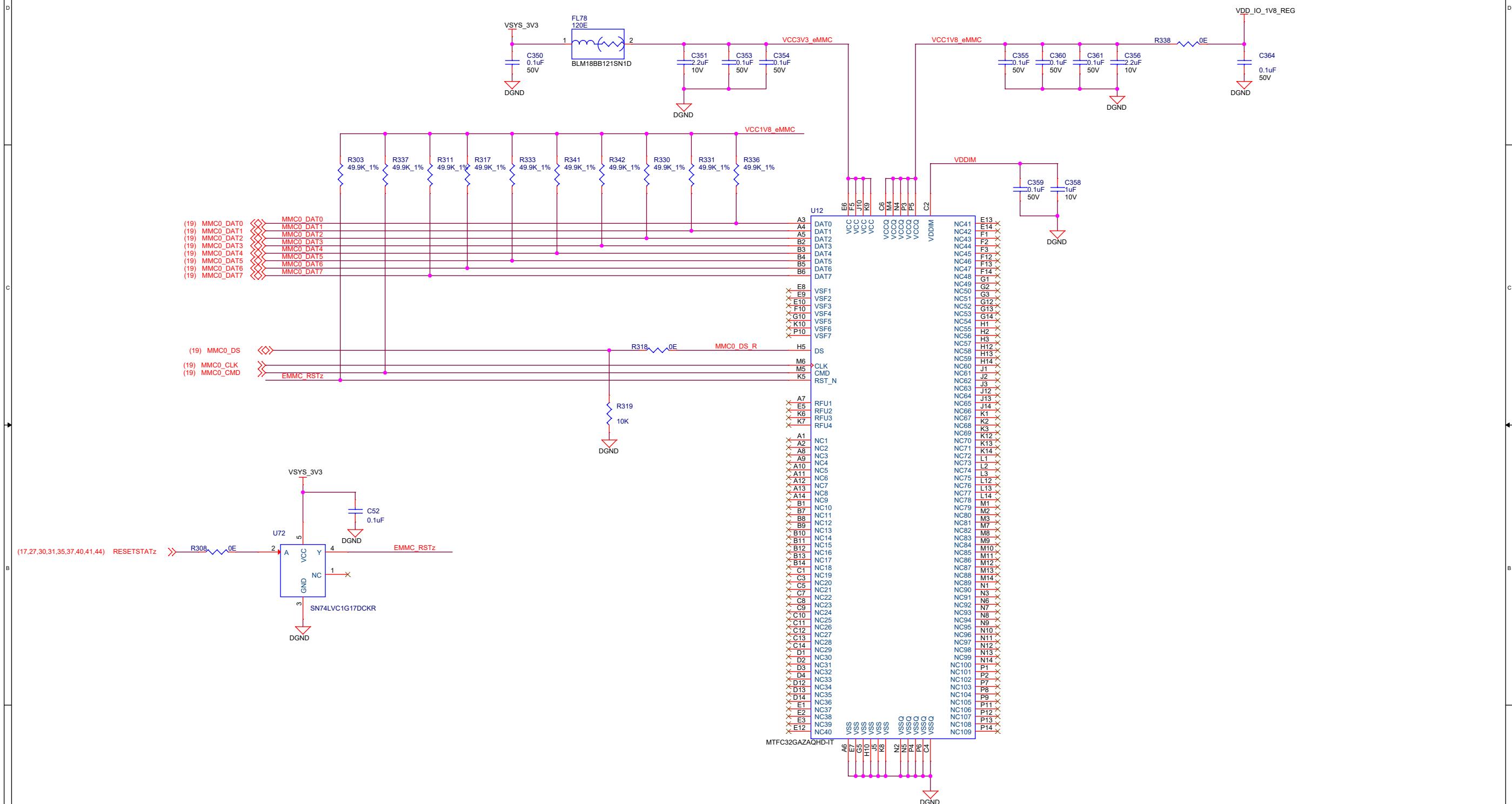
BOARD ID EEPROM



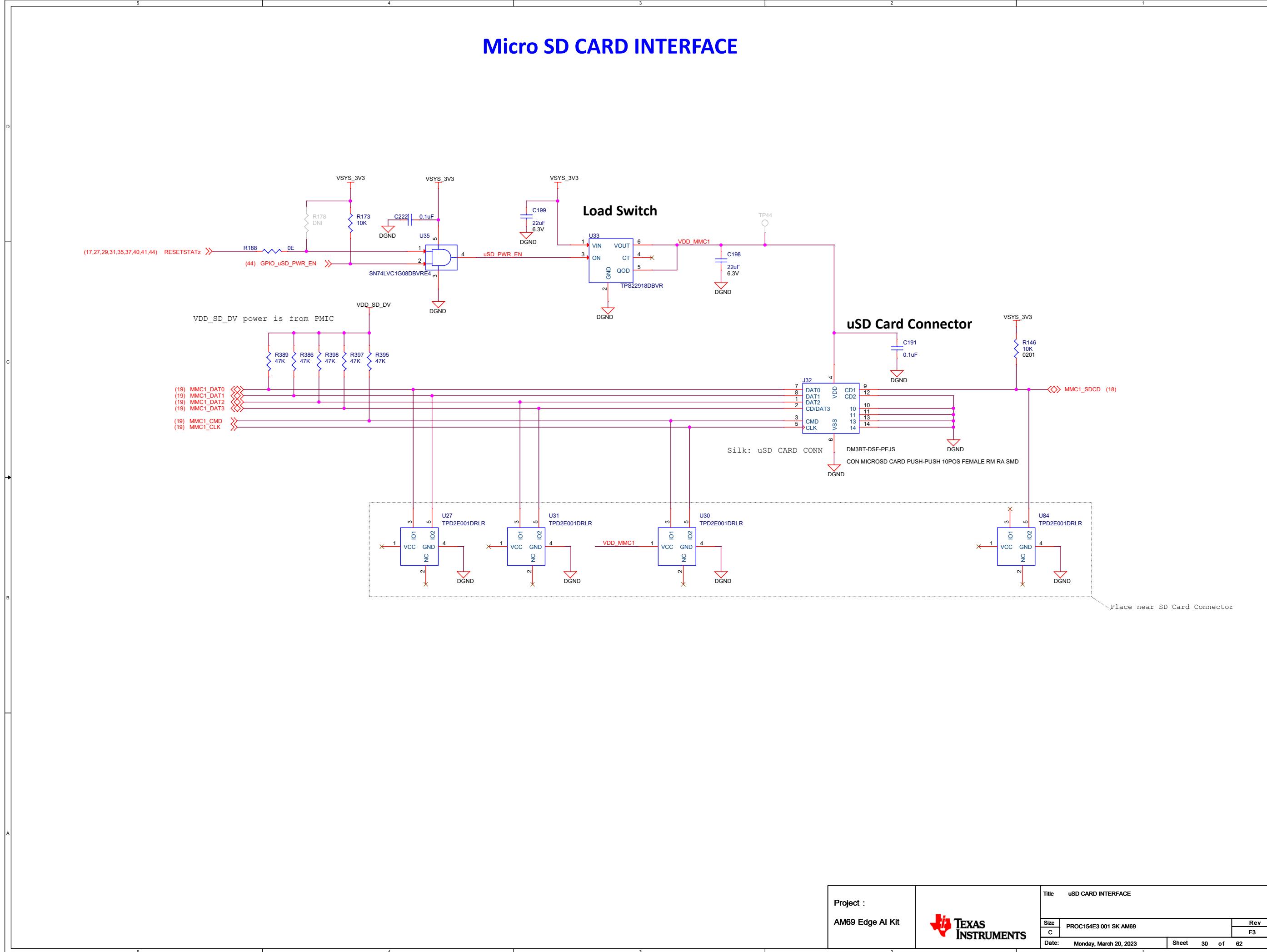
40Pin Expansion Header



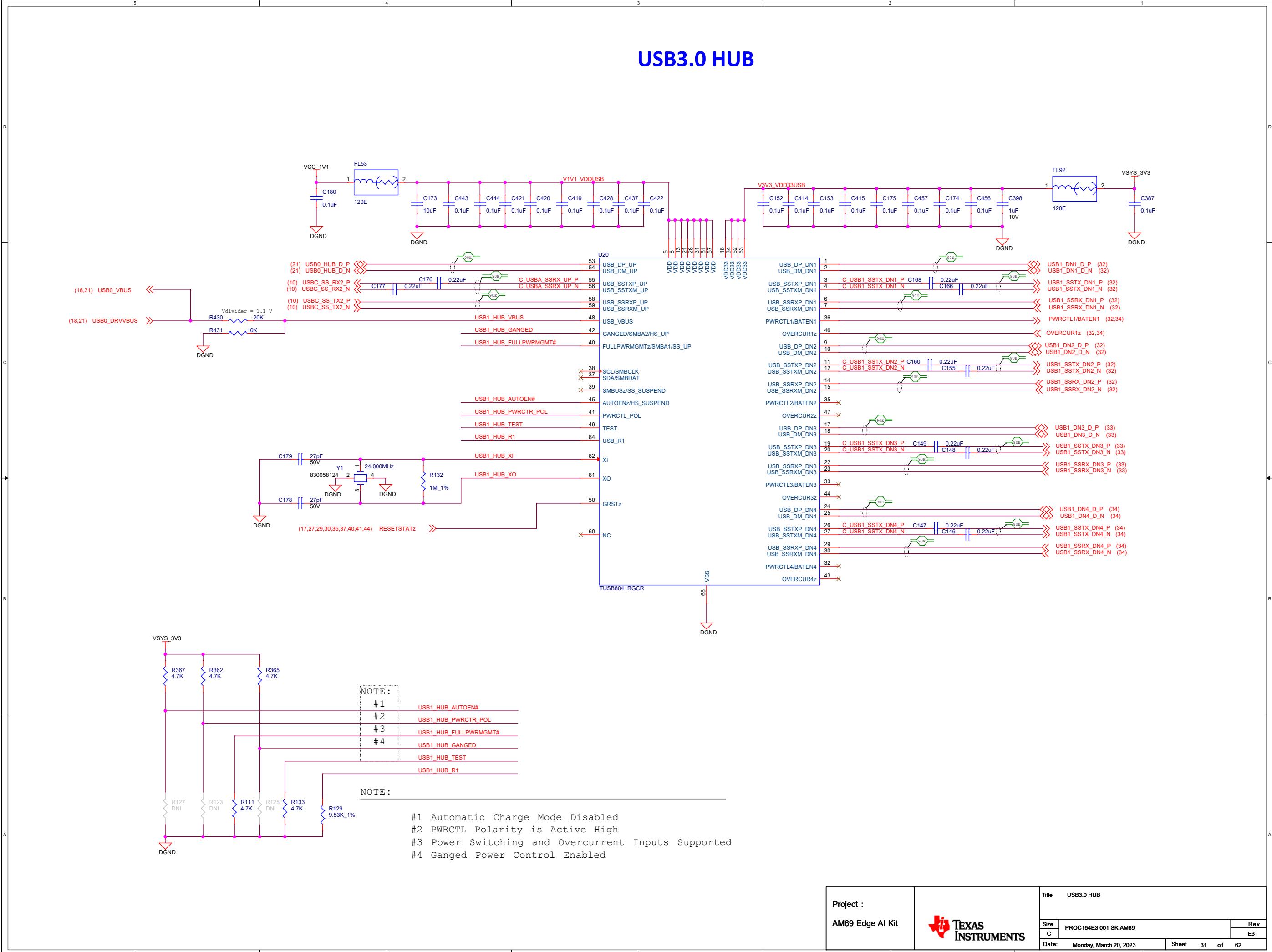
eMMC FLASH



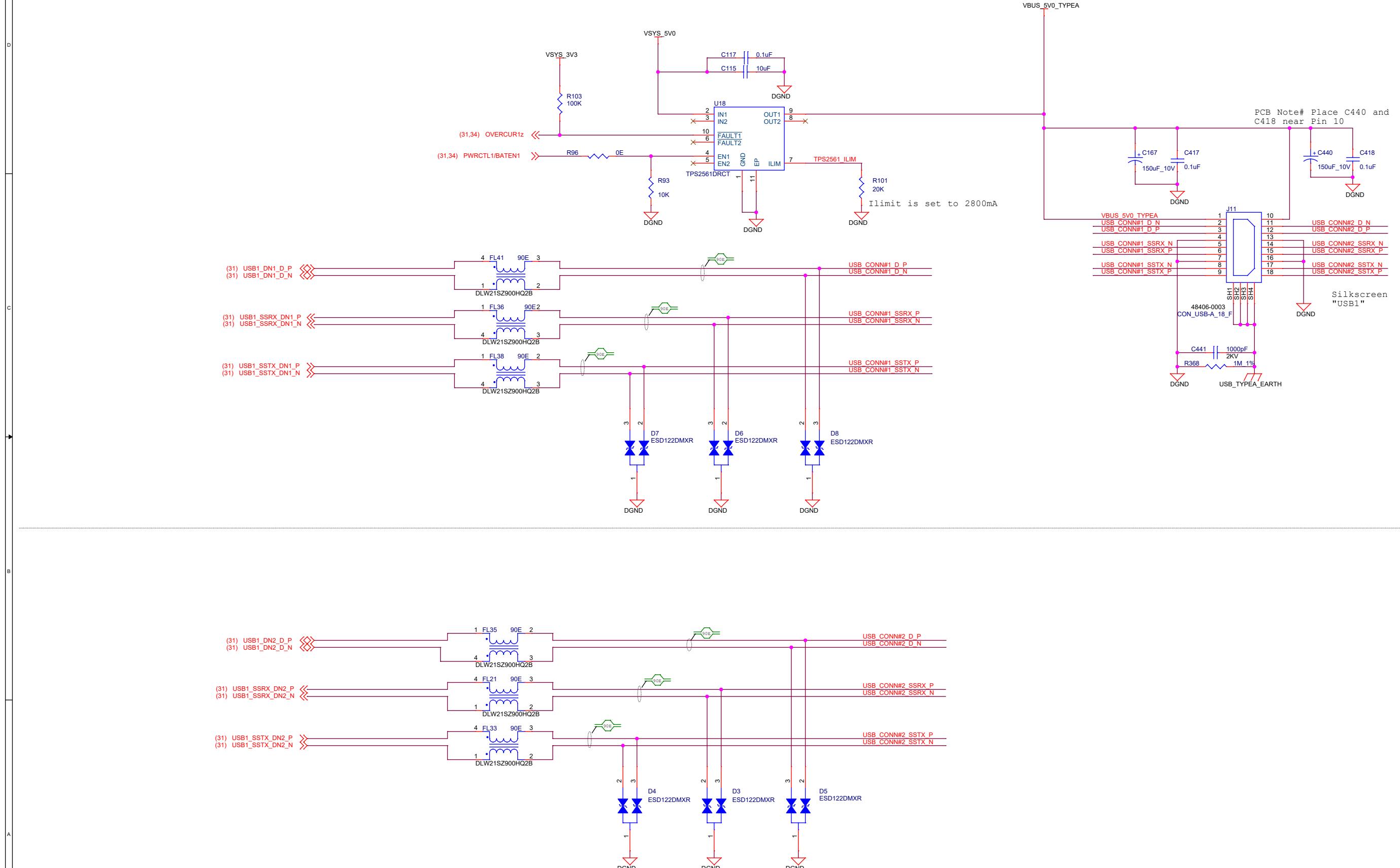
Micro SD CARD INTERFACE



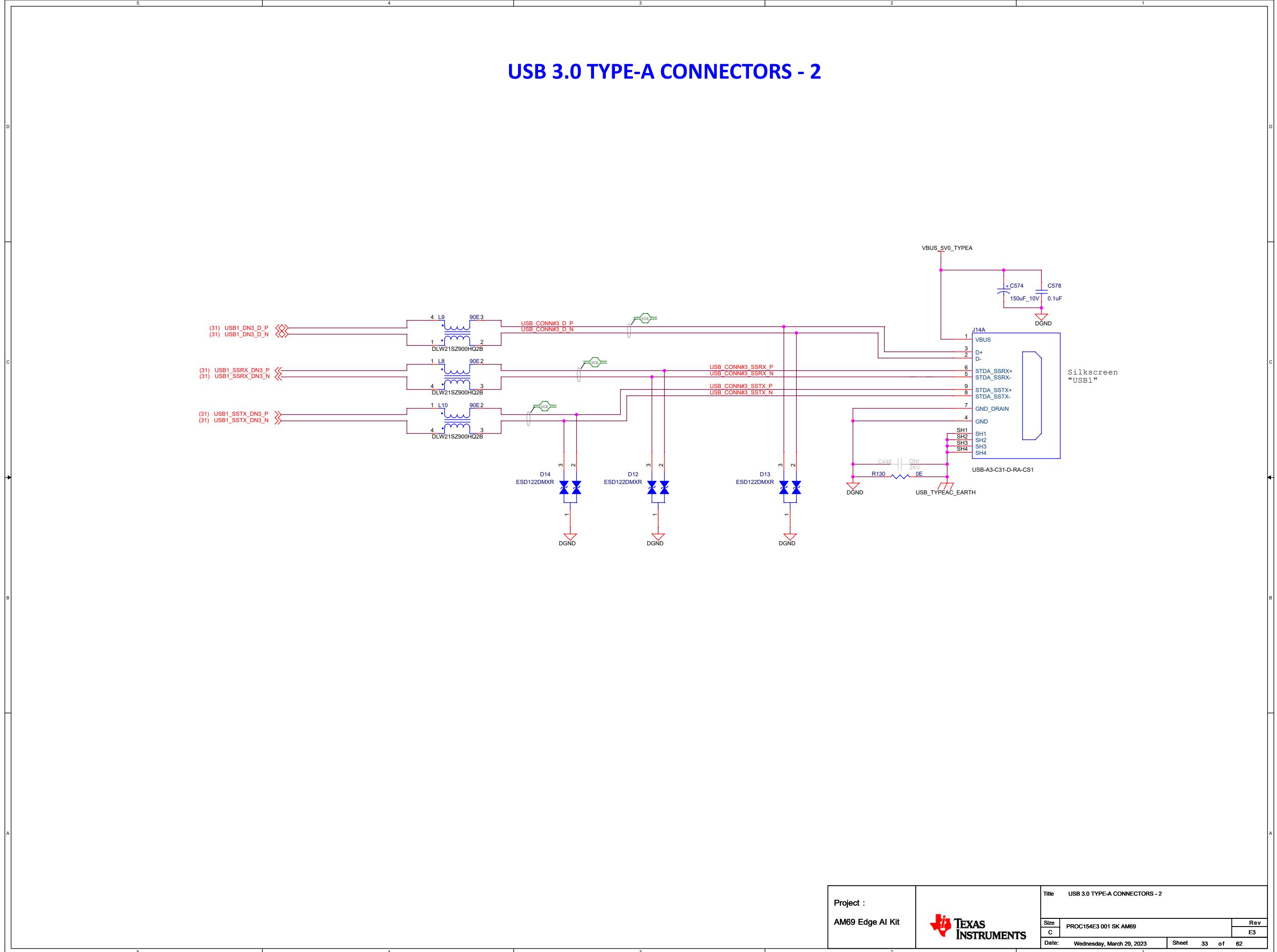
USB3.0 HUB



USB 3.0 TYPE-A CONNECTORS - 1

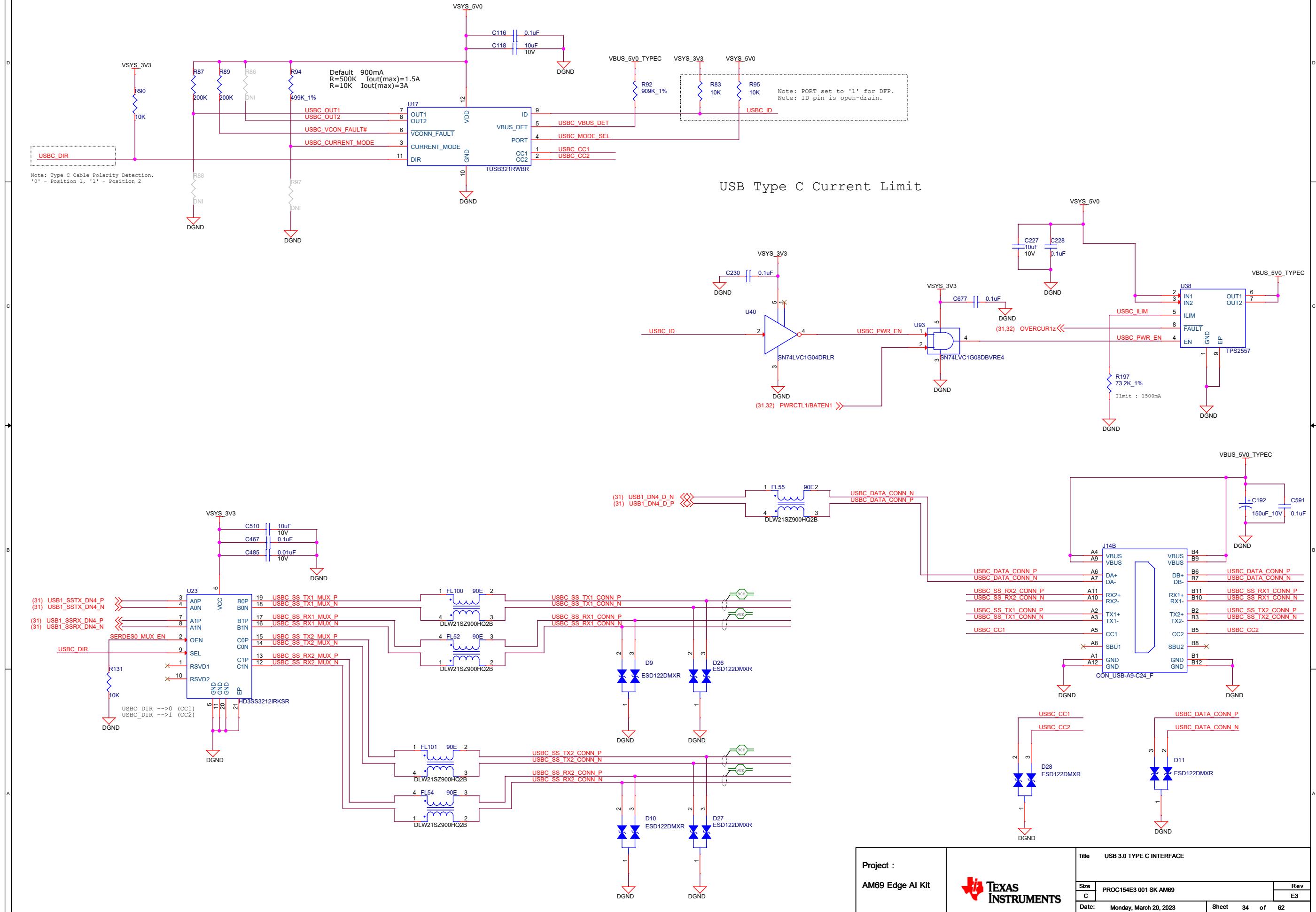


USB 3.0 TYPE-A CONNECTORS - 2



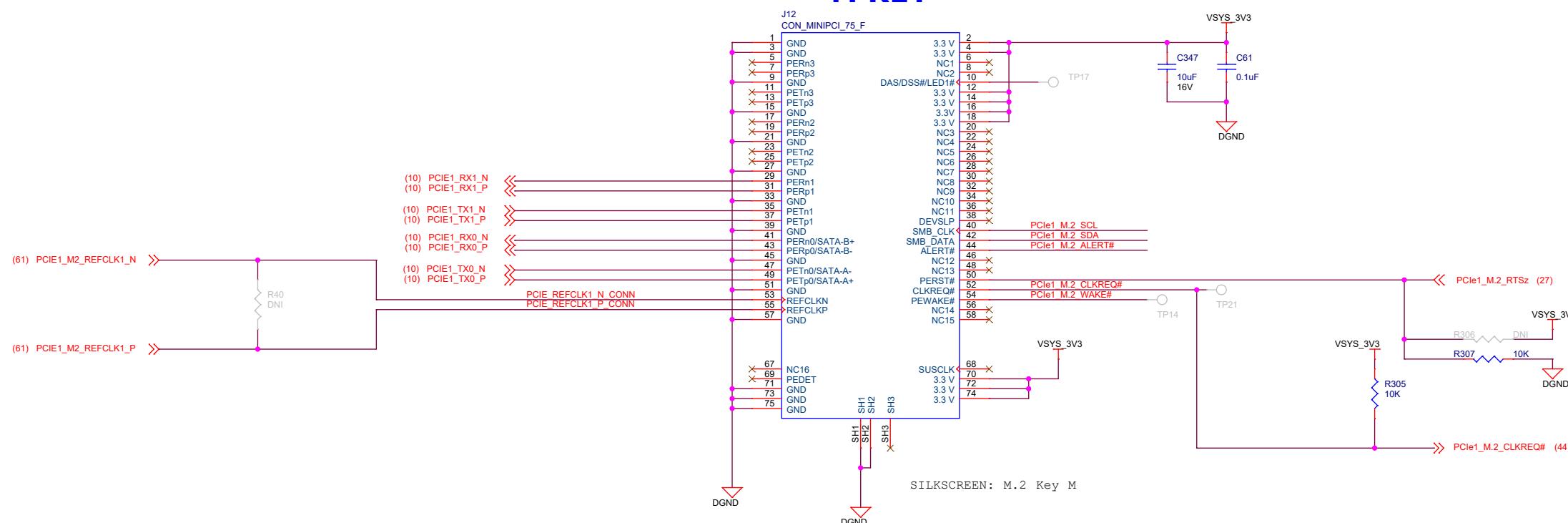
Project : AM69 Edge AI Kit		Title USB 3.0 TYPE-A CONNECTORS - 2	
Size C	Rev E3	PROC154E3 001 SK AM69	
Date: Wednesday, March 29, 2023	Sheet 33 of 62		

USB 3.0 TYPE C INTERFACE

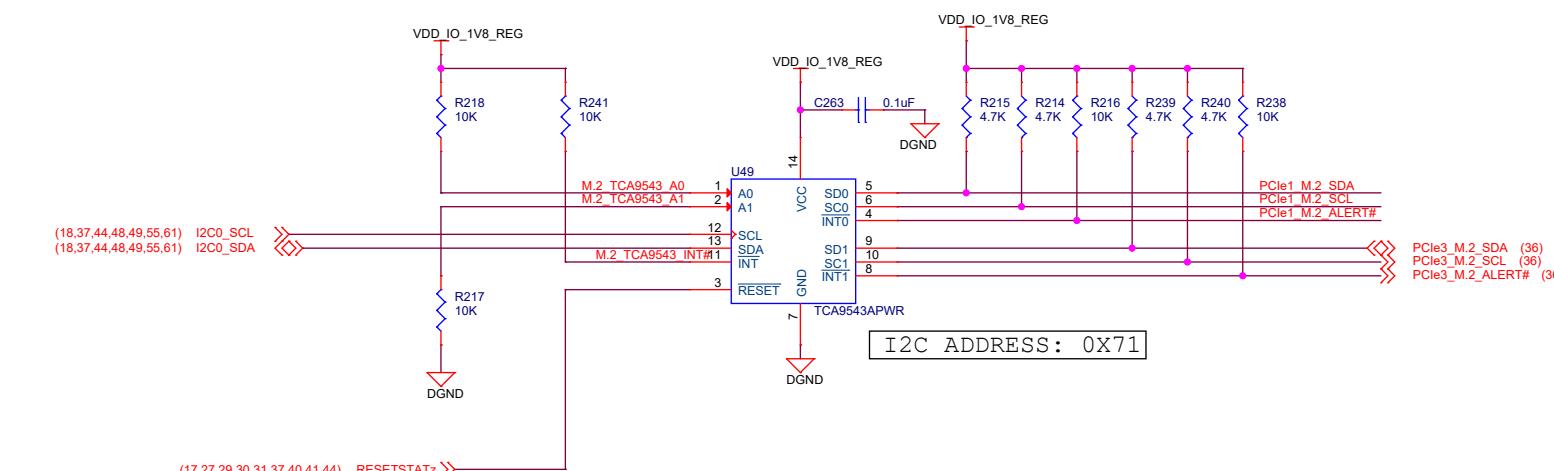


PCIe_M.2_INTERFACE SSD

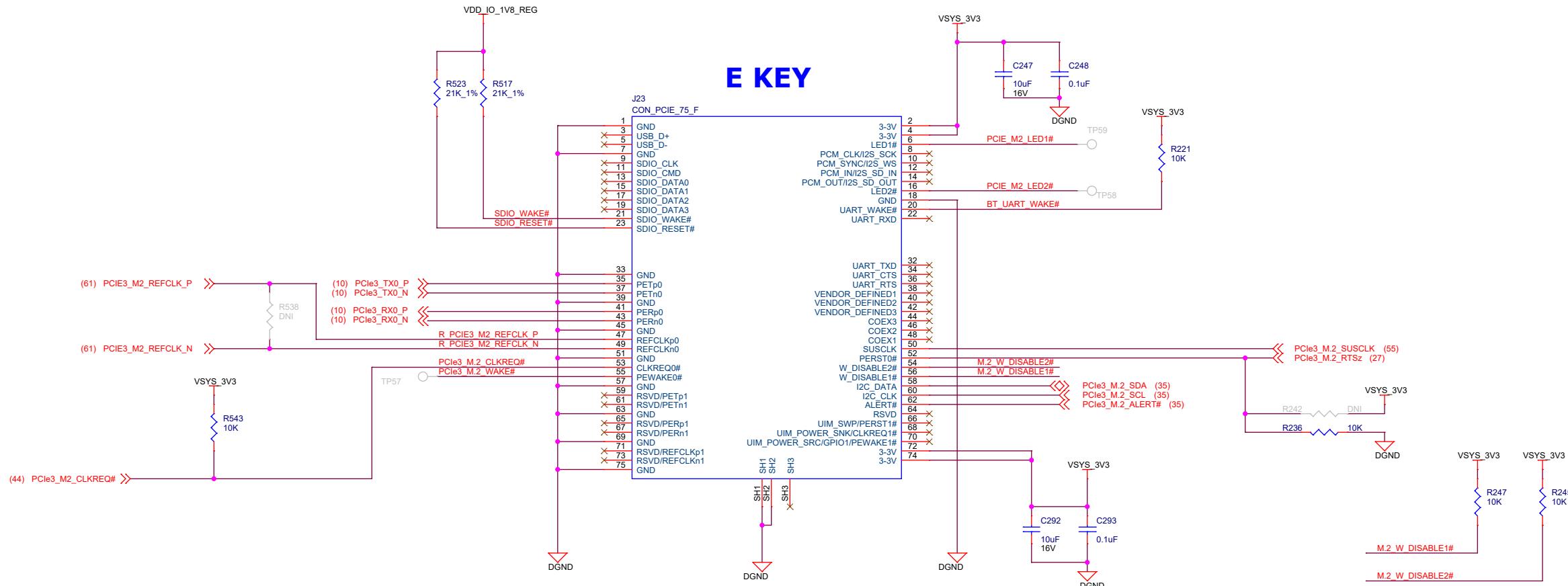
M KEY



3.3V To 1V8 Level translator



PCIe_M.2_INTERFACE - SDIO

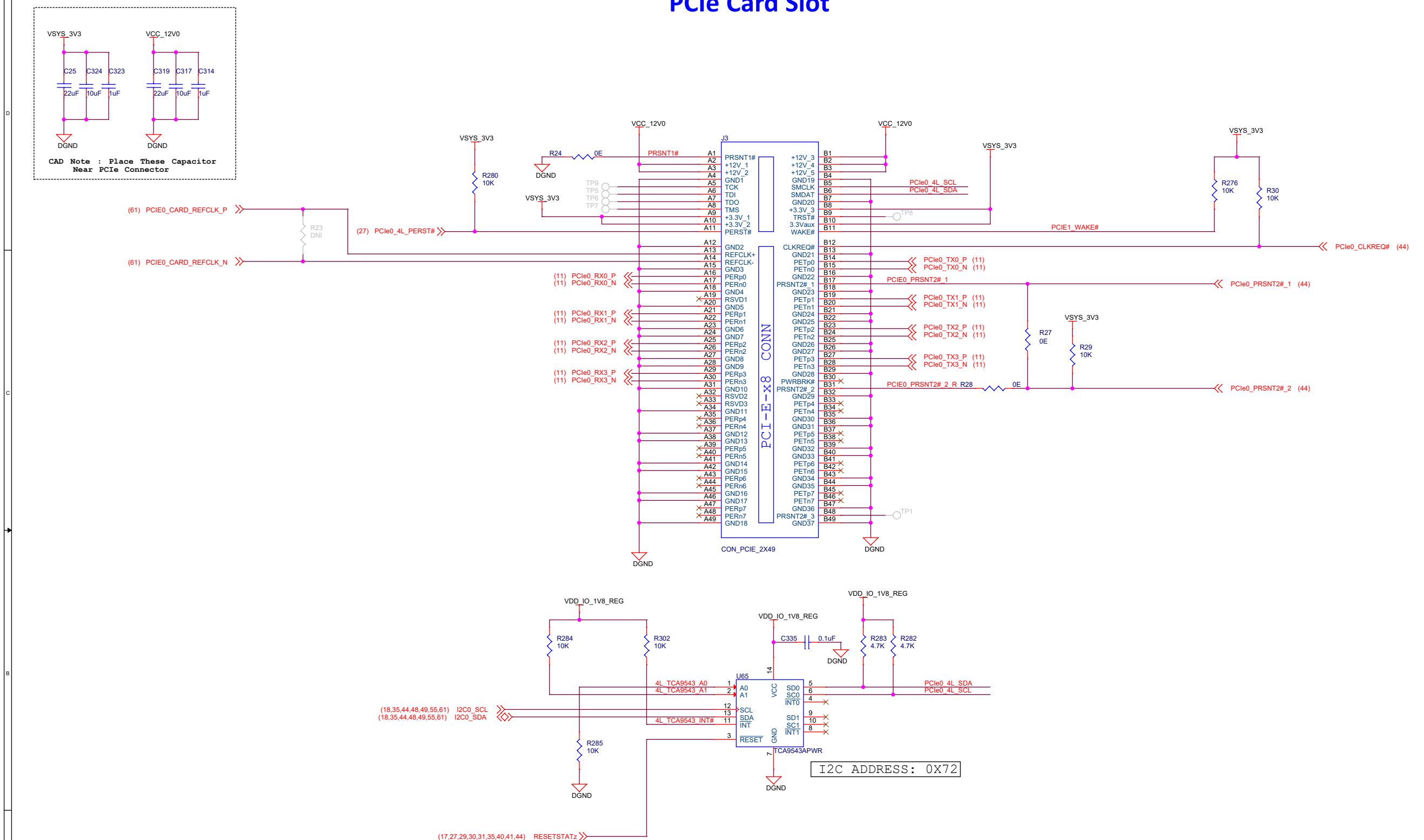


E KEY

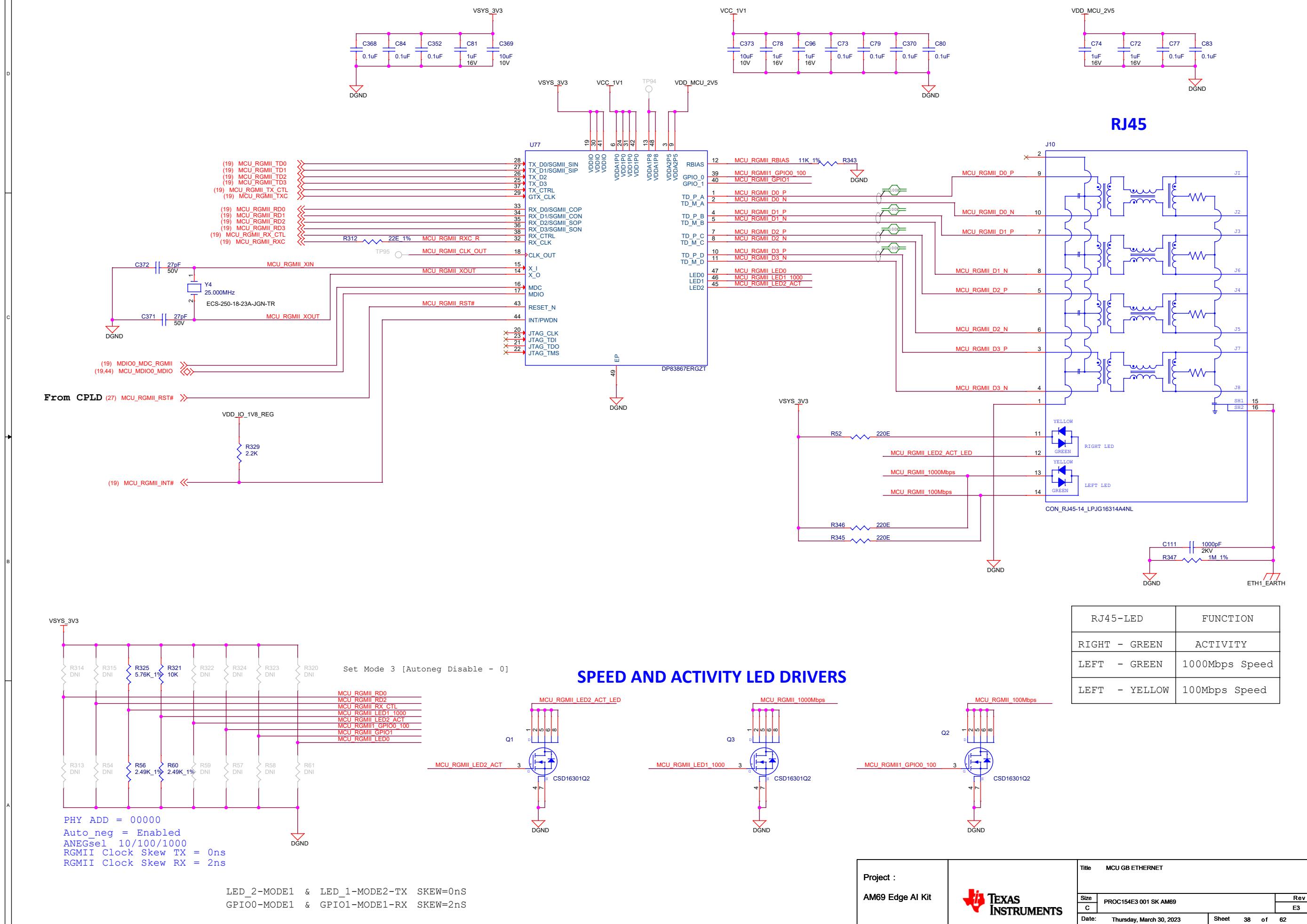
Project :	AM69 Edge AI Kit	Title	PCIe_M.2_INTERFACE (E Key)
Size	PROC154E3 001 SK AM69	Rev	E3
Date:	Monday, March 20, 2023	Sheet	36 of 62



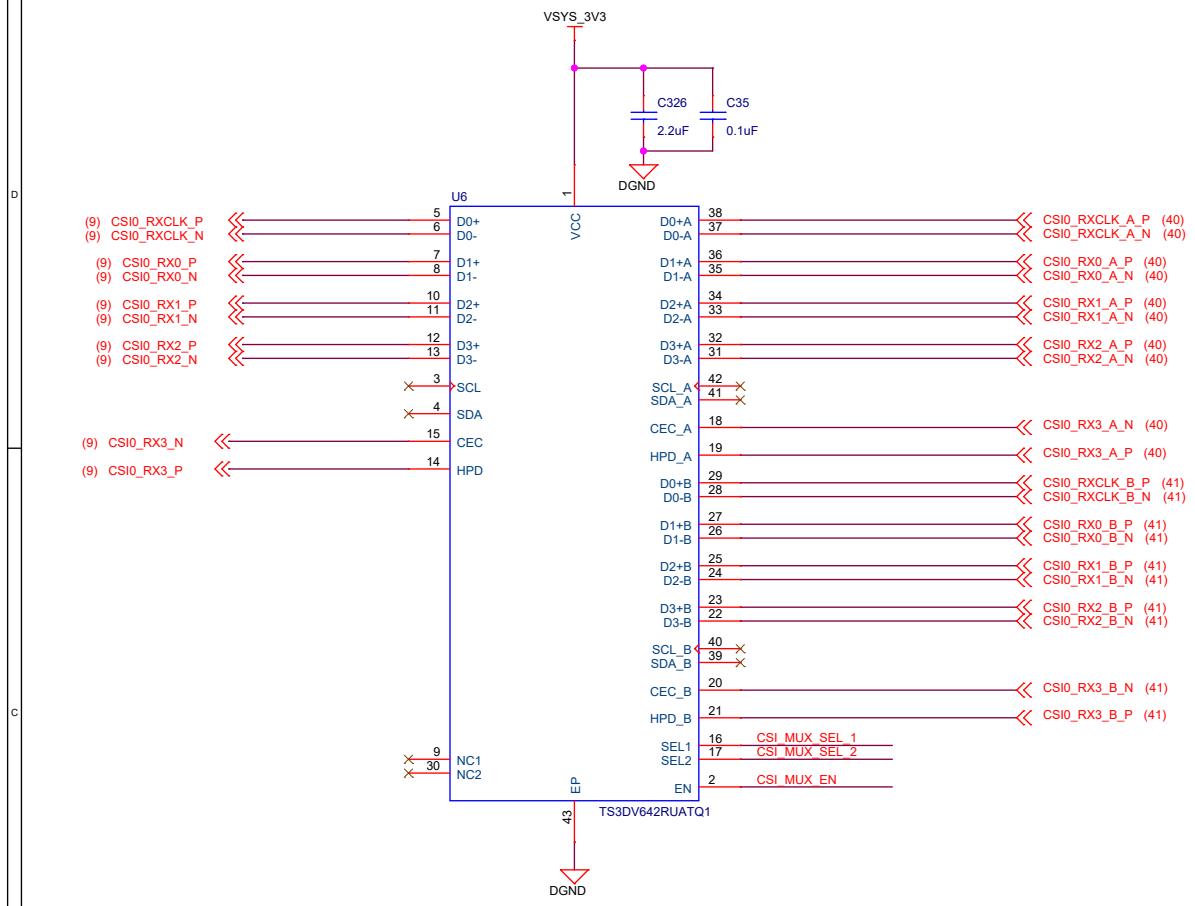
PCIe Card Slot



MCU GB ETHERNET

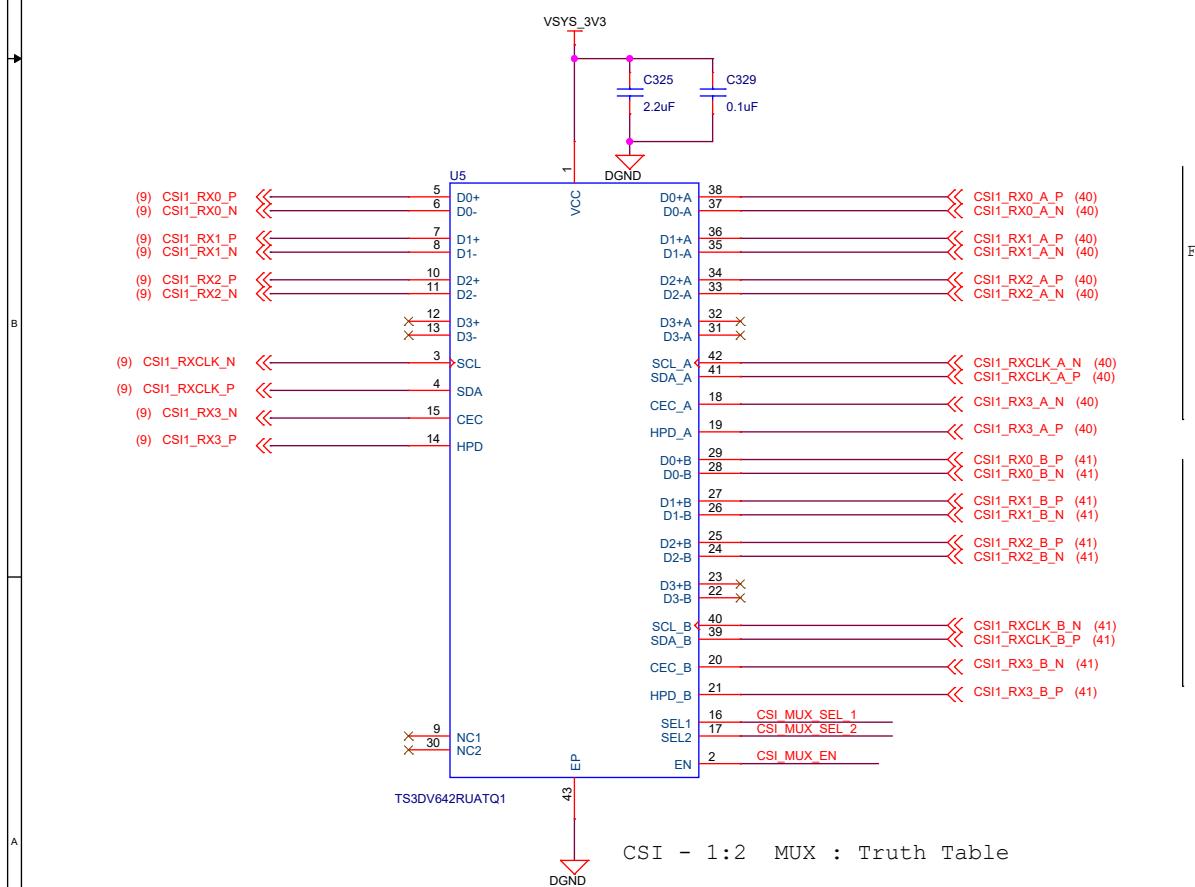


CSI MUX - DATA



From CSI EXP Conn

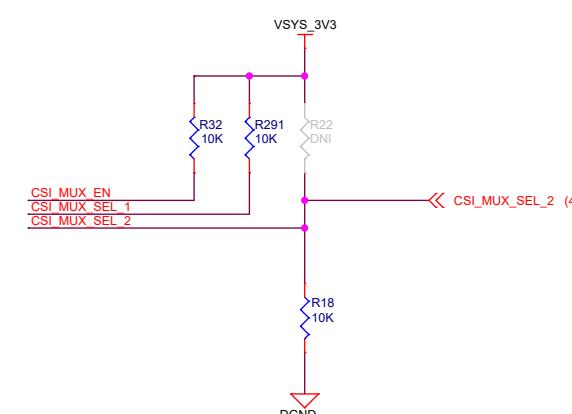
From FPC Camera Conn



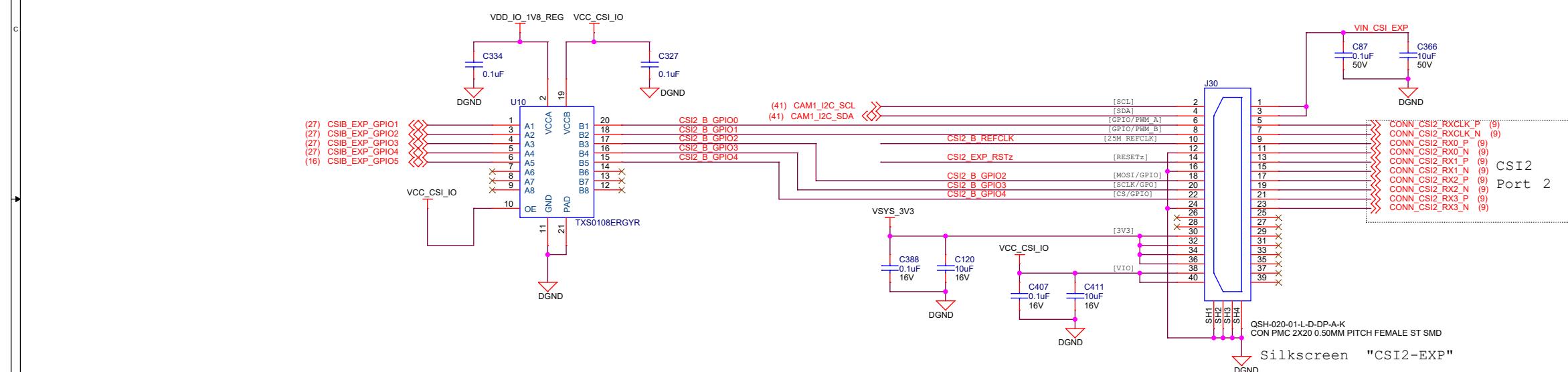
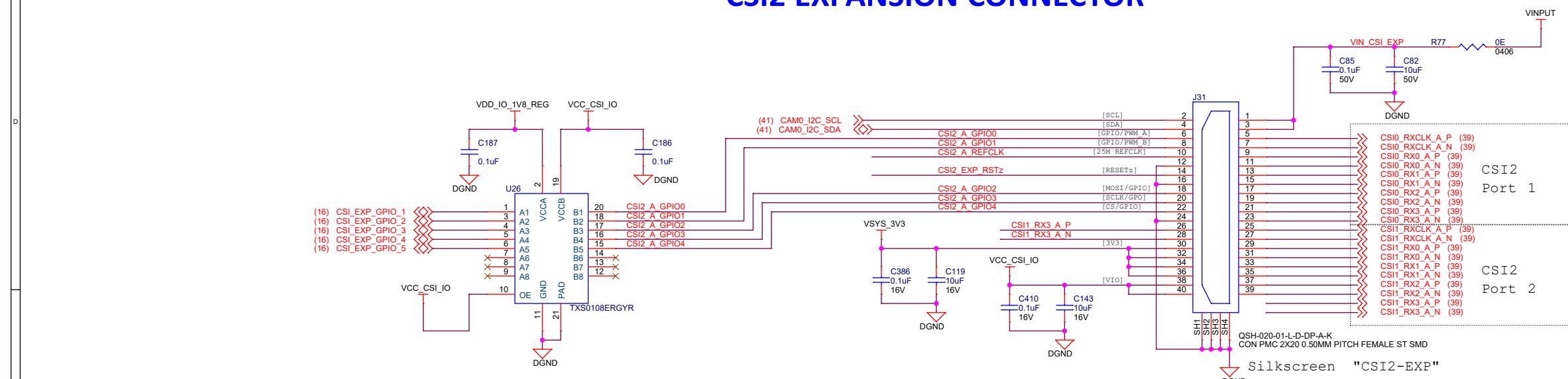
From CSI EXP Conn

From FPC Camera Conn

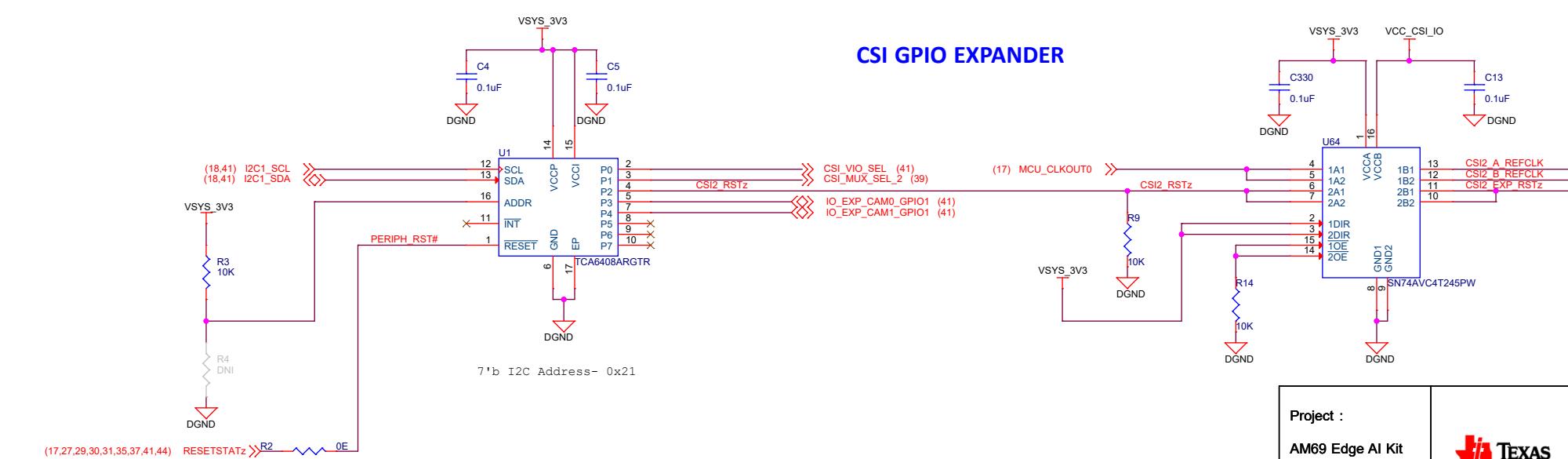
CSI - 1:2 MUX : Truth Table



CSI2 EXPANSION CONNECTOR



CSI GPIO EXPANDER



Project :
AM69 Edge AI Kit



Title CSI2 EXPANSION CONNECTOR

Size C PROC154E3 001 SK AM69

Rev E3

Date Monday, March 20, 2023

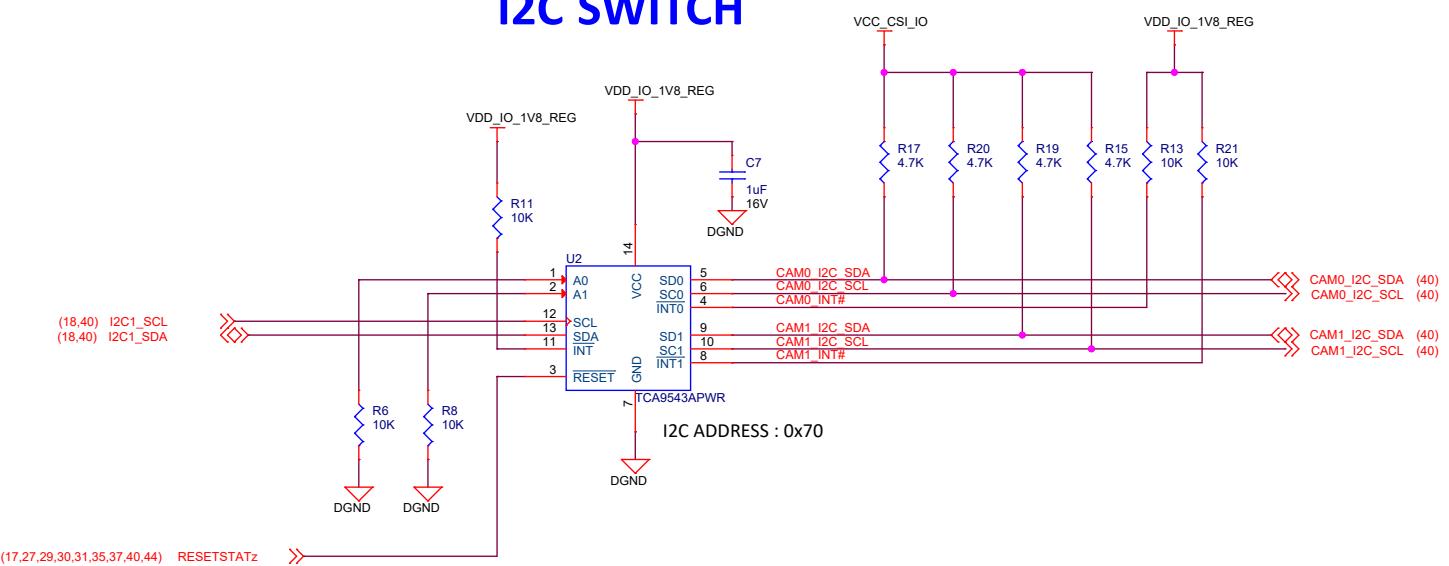
Sheet 40 of 62

CSI FPC CAMERA CONNECTORS

Silk Screen "CAM1"

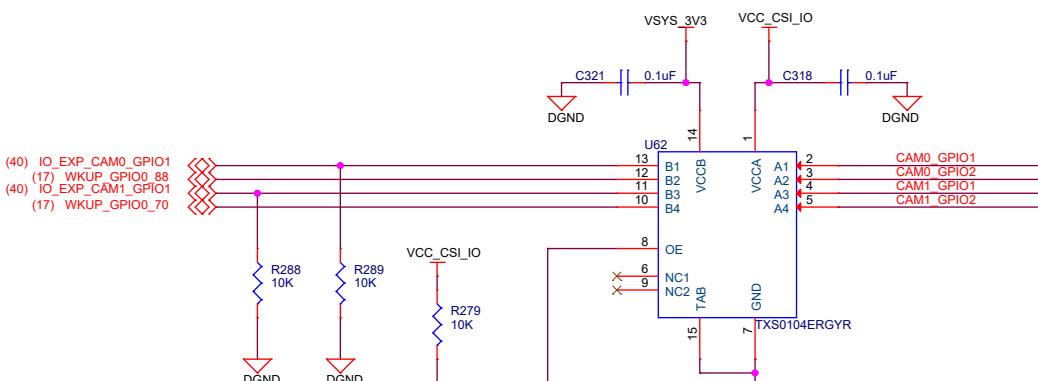
FPC Camera Connector -1

I2C SWITCH

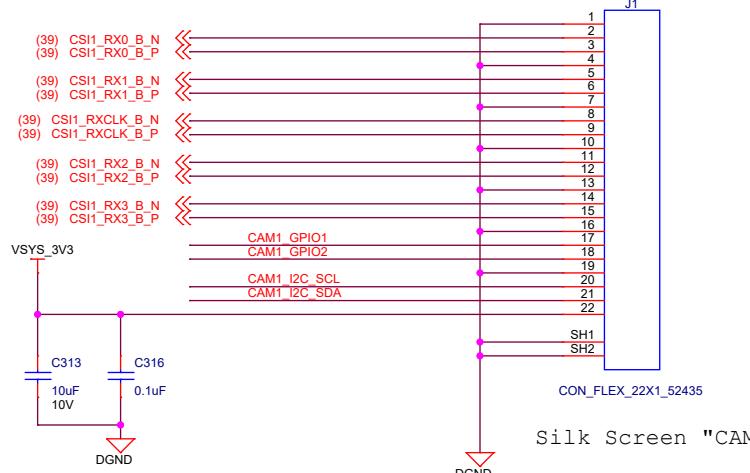
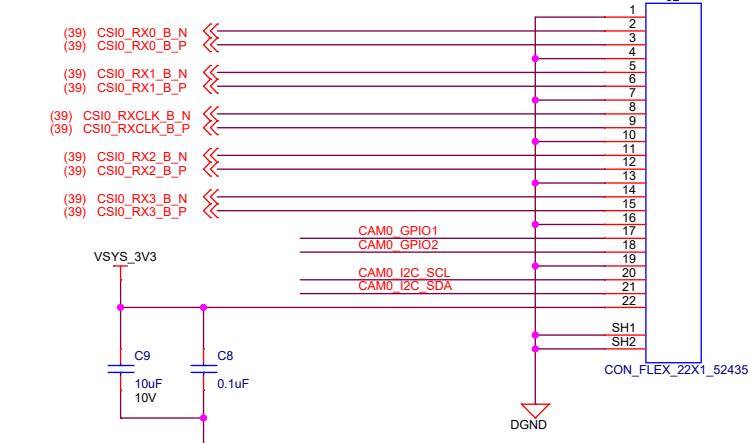
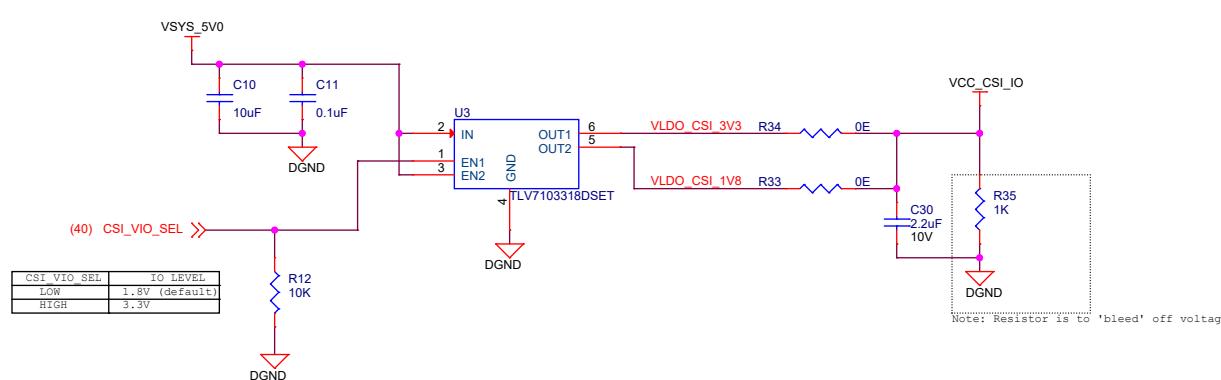


GPIO LEVEL TRANSLATOR

FPC Camera Connector -2

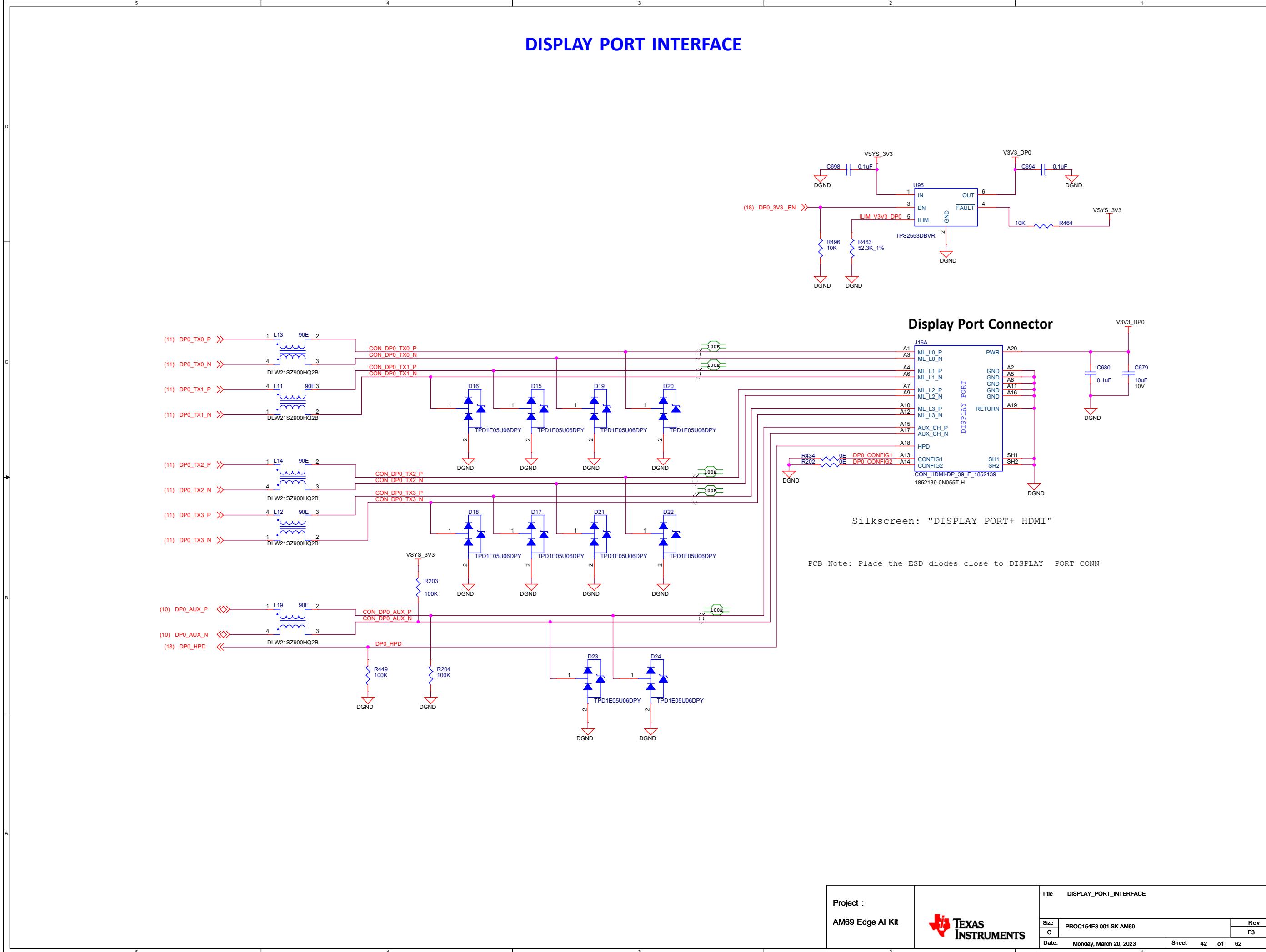


CAMERA IO SUPPLY

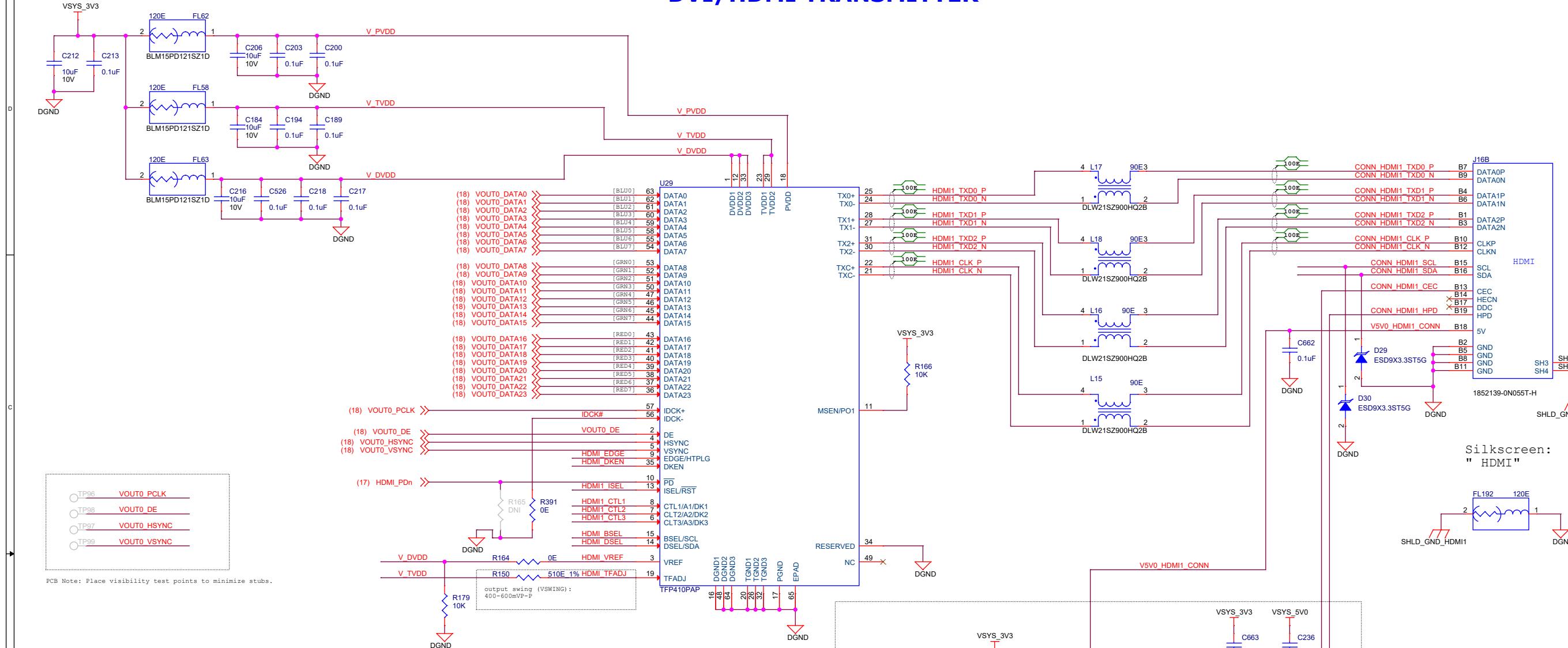


Silk Screen "CAM2"

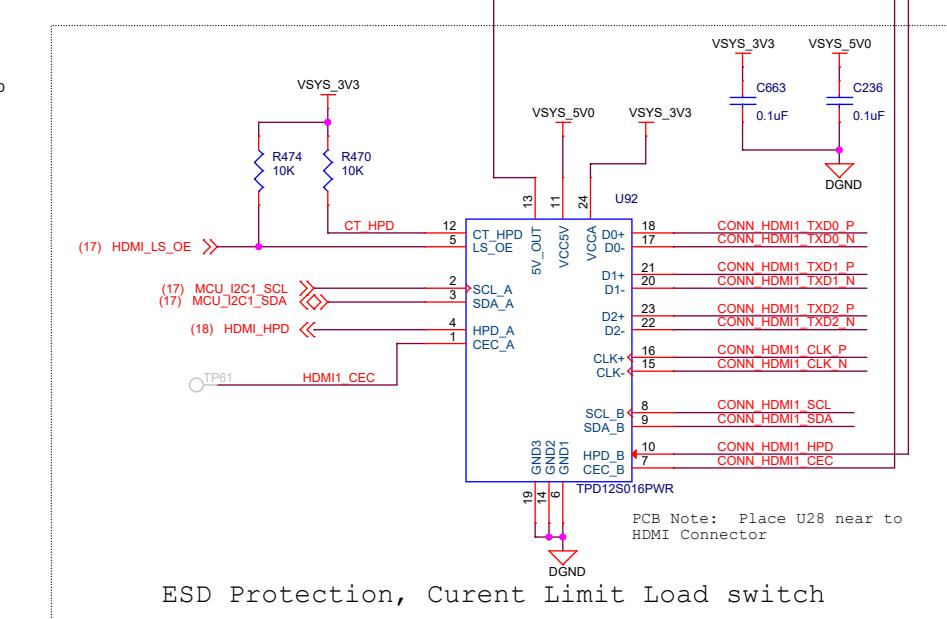
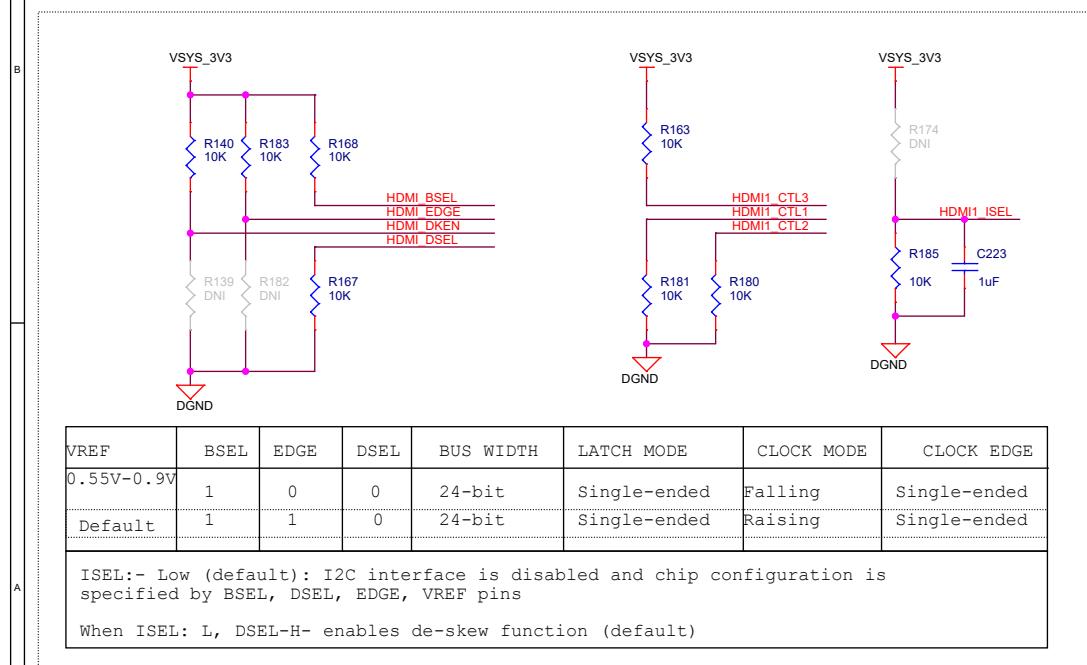
DISPLAY PORT INTERFACE



DVI/HDMI TRANSMITTER

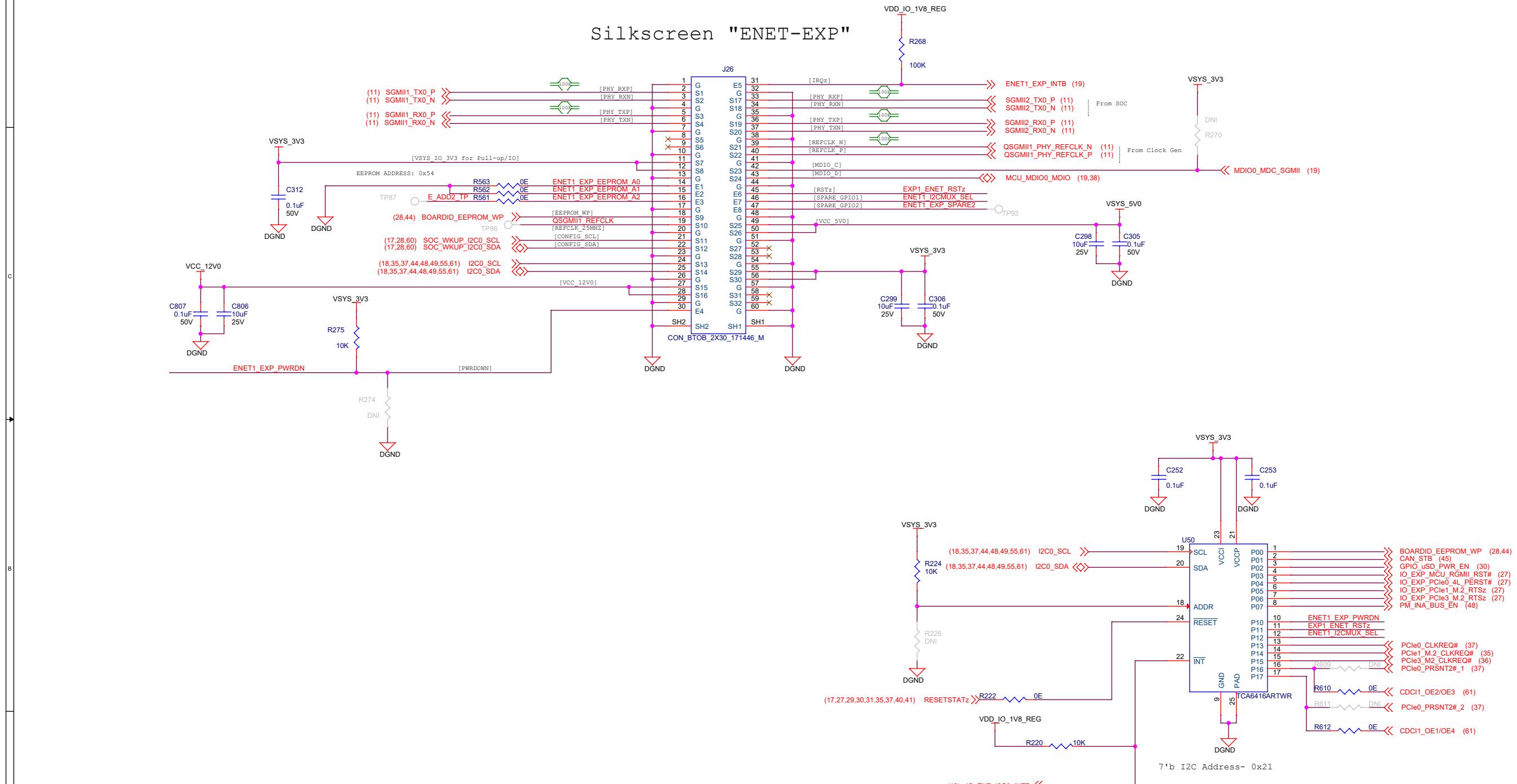


DVI Configuration Settings

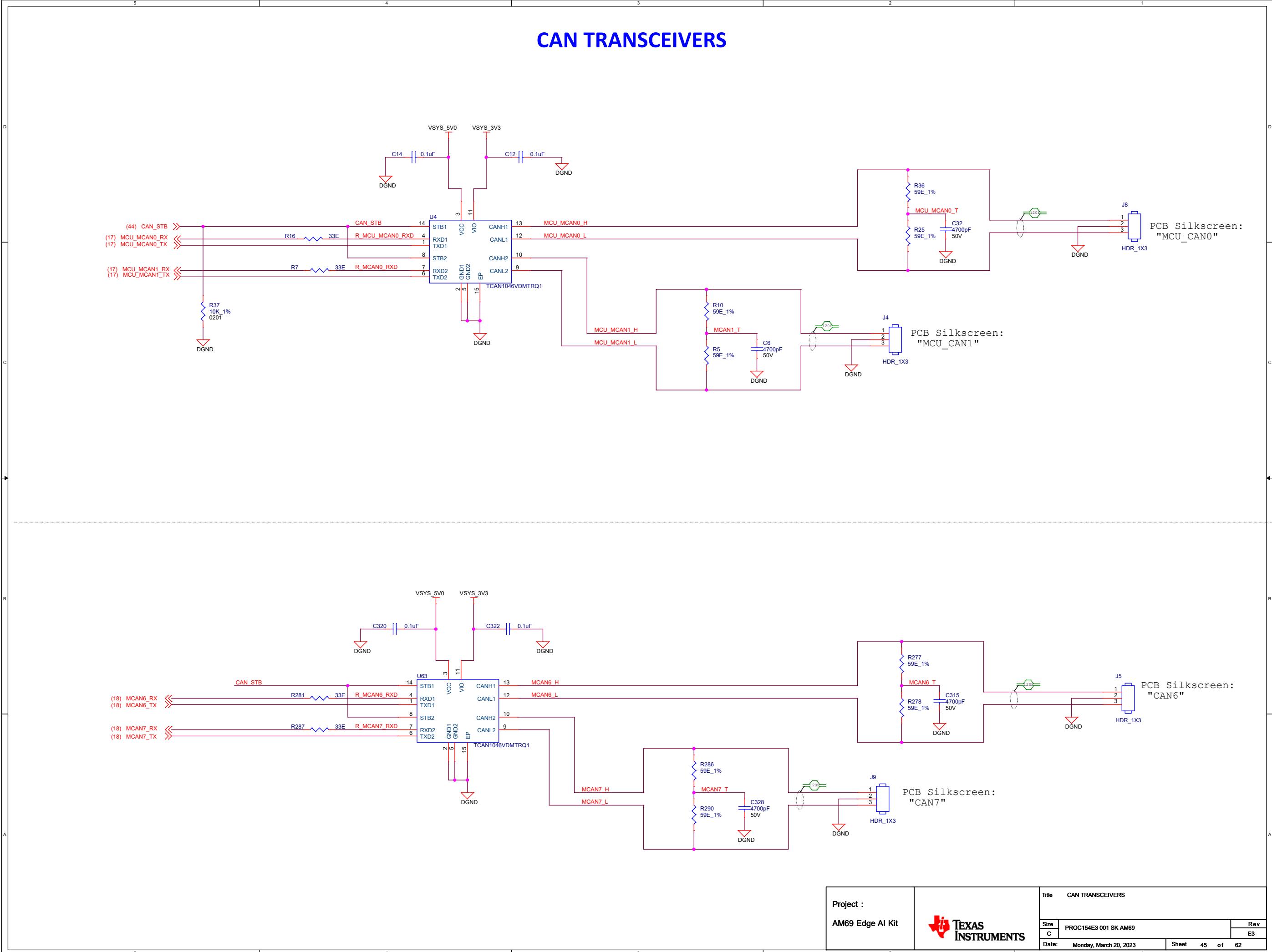


ESD Protection, Current Limit Load switch

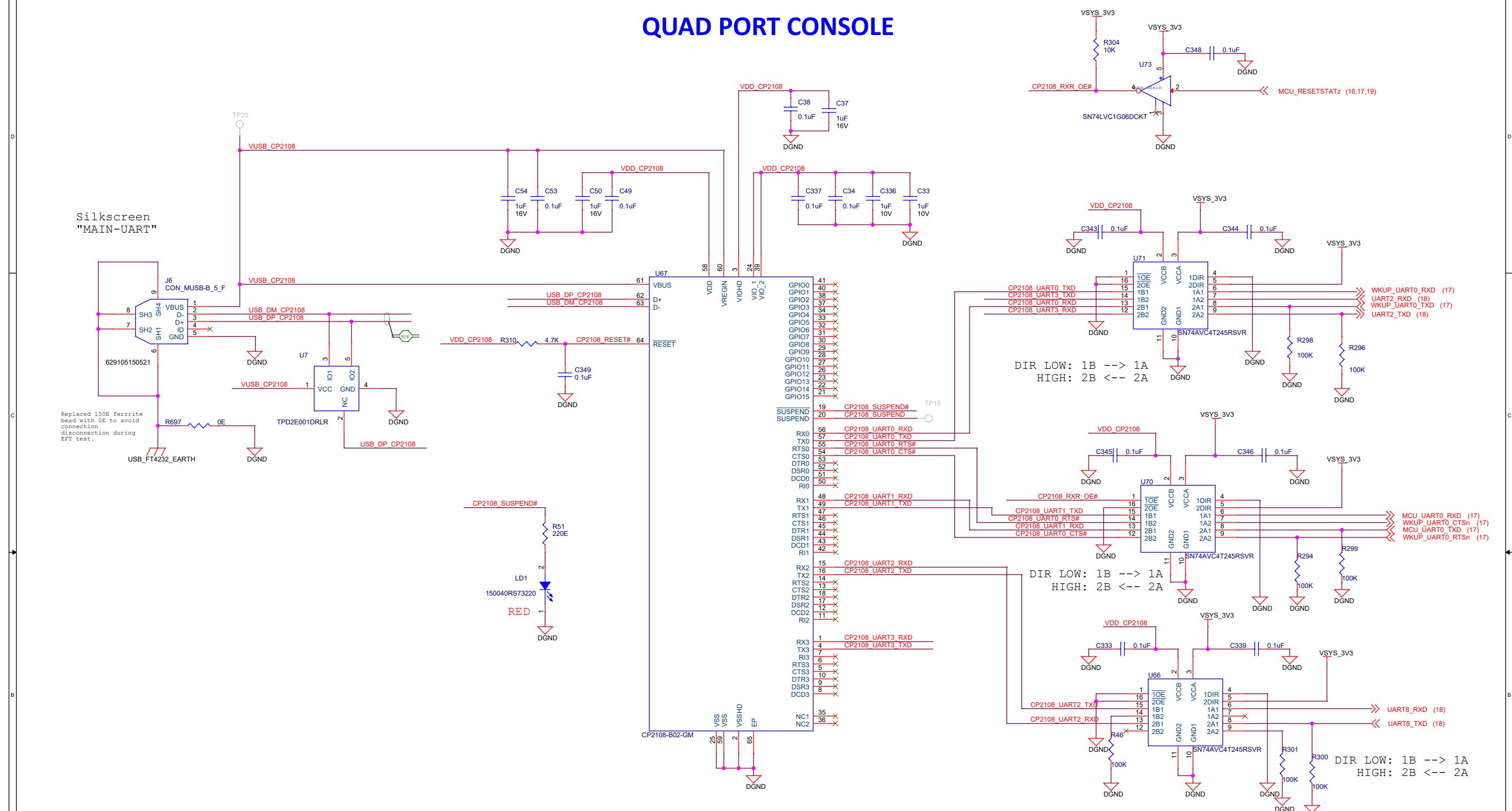
ENET EXPANSION CONNECTOR



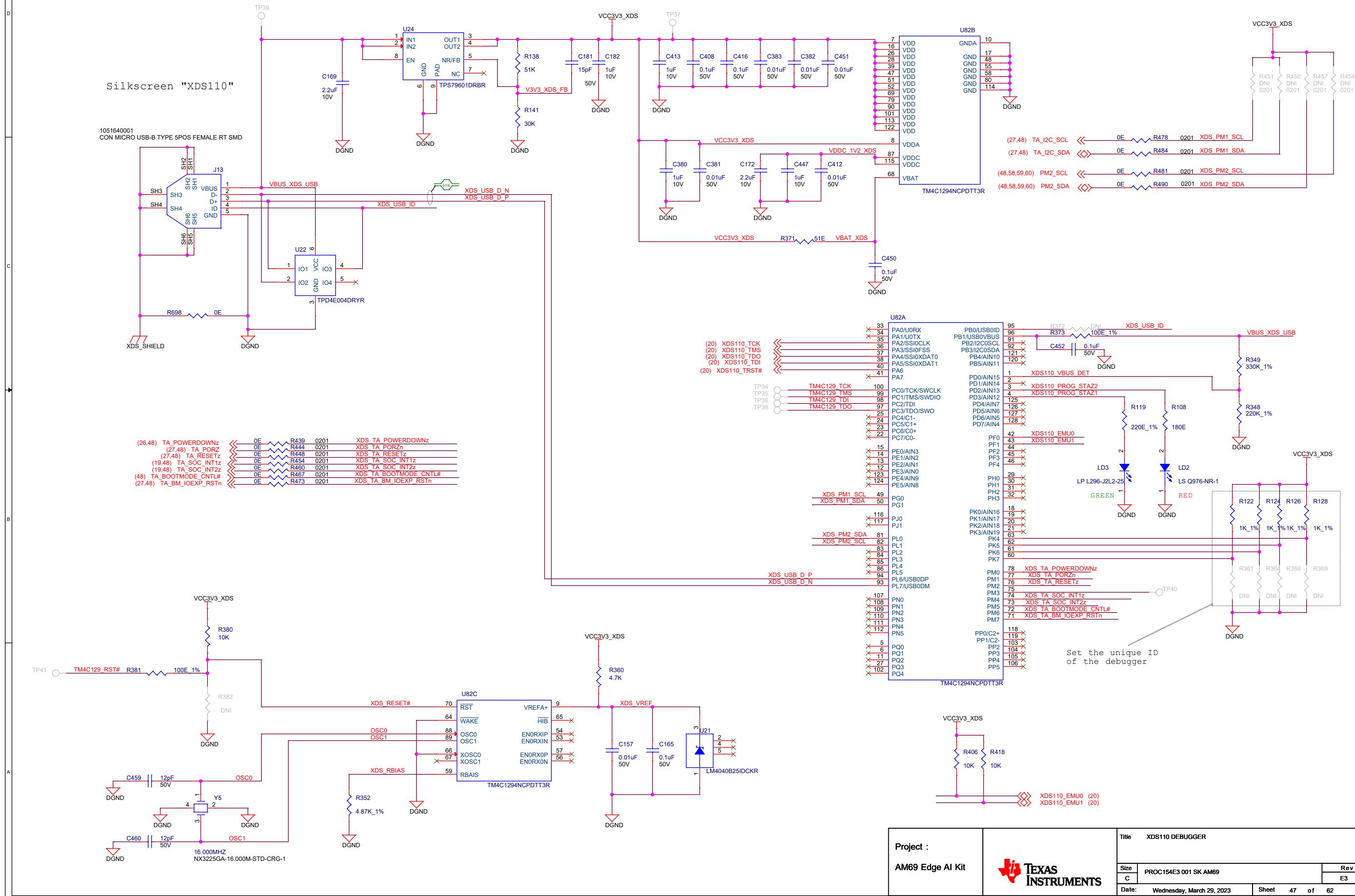
CAN TRANSCEIVERS



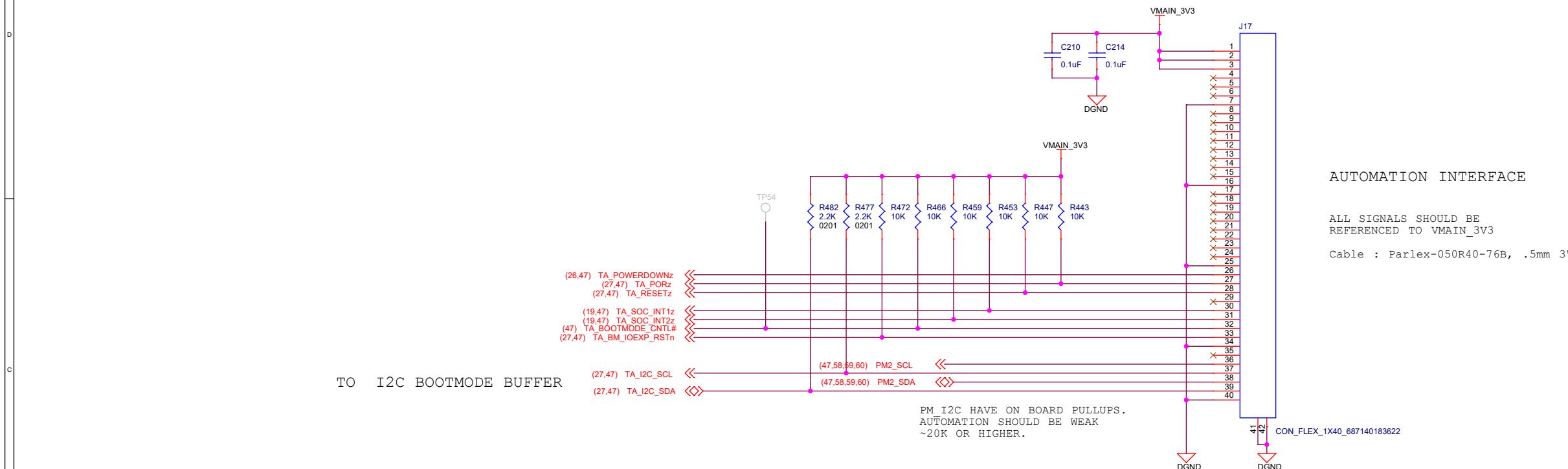
QUAD PORT CONSOLE



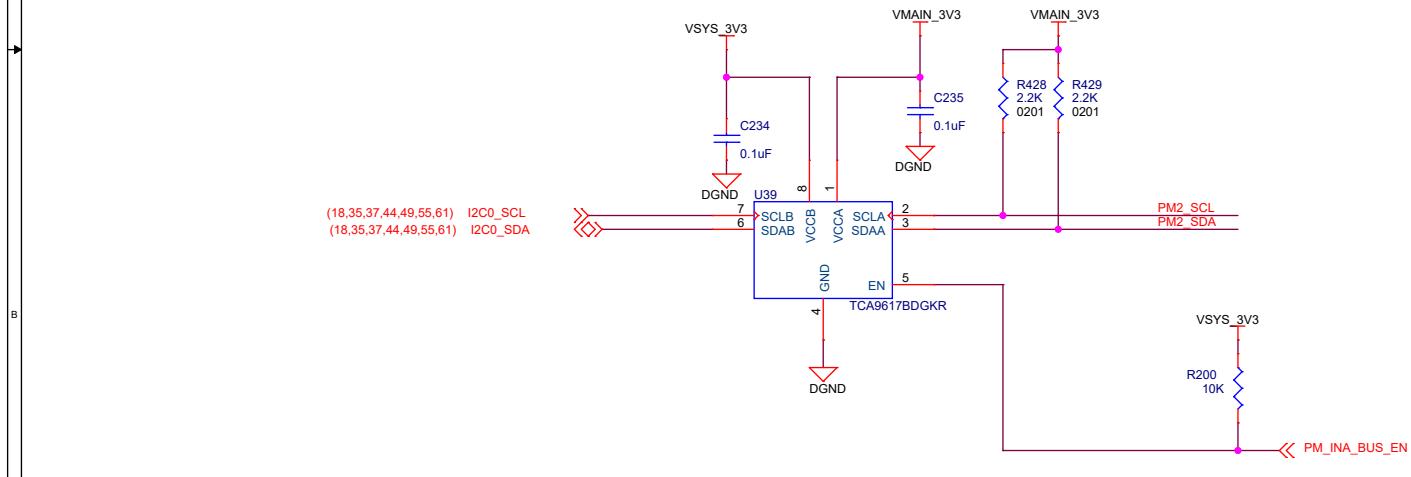
XDS110 DEBUGGER



TEST AUTOMATION HEADER

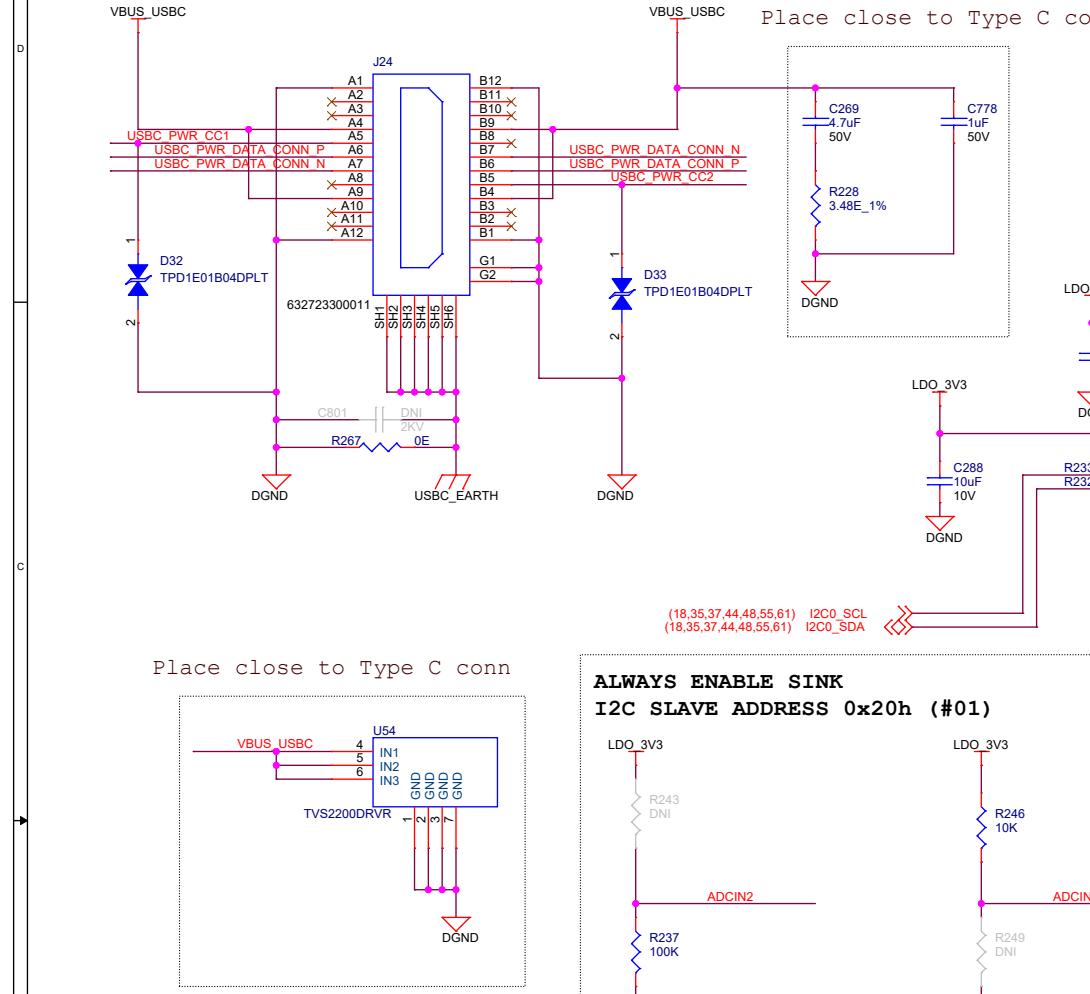


TEST AUTOMATION GPIO MAPPING

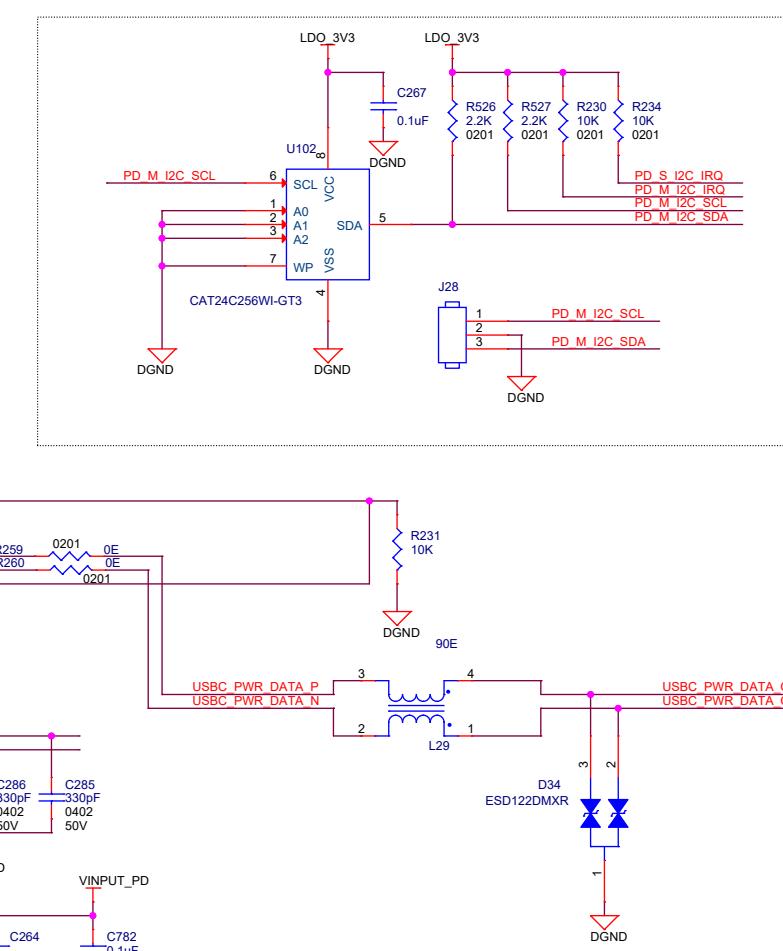


SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TA_POWERDOWN	Used to Power down the system	OUTPUT	External Pullup
TA_PORZn	MCU & Main SoC domain Power ON Reset	OUTPUT	External Pullup
TA_RESETz	SoC Warmreset	OUTPUT	External Pullup
TA_SOC_INT1z	Interrupt to SOC	OUTPUT	External Pullup
TA_SOC_INT2z	Interrupt to SOC	OUTPUT	External Pullup
TA_BM_IOEXP_RSTn	Used to Reset the Bootmode IO Expander	OUTPUT	External Pullup

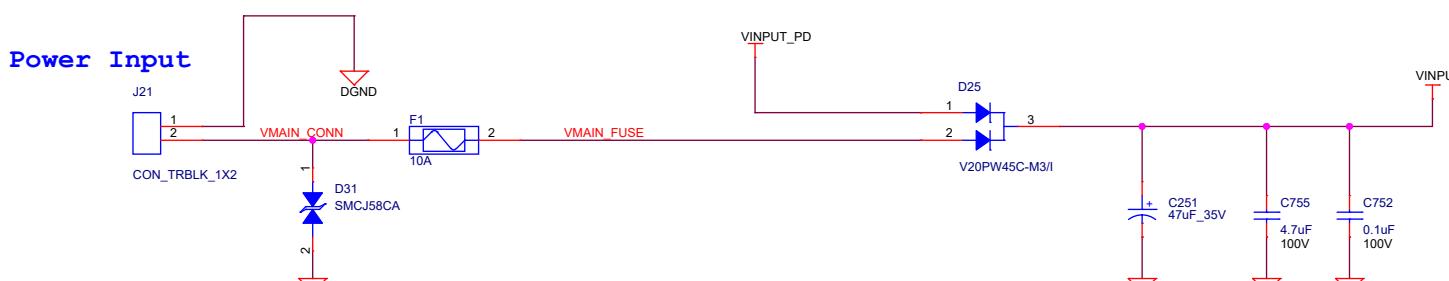
USB-C Power



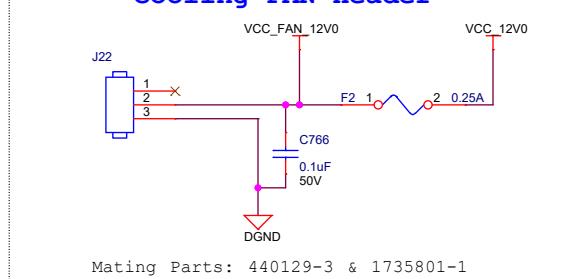
EPPROM & PROGRAMMING HEADER



OPTIONAL POWER INPUT

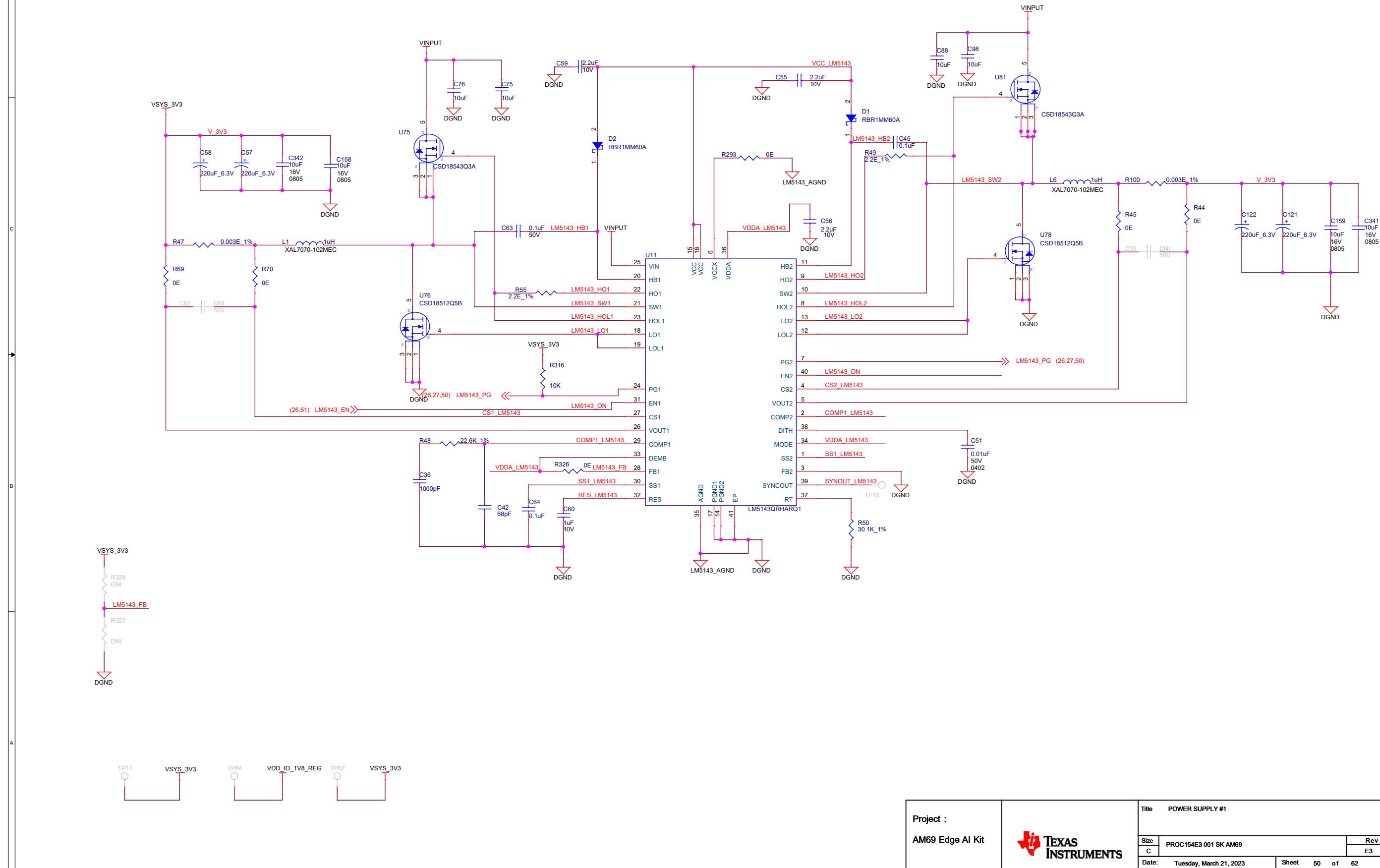


Cooling FAN Header



POWER SUPPLY #1

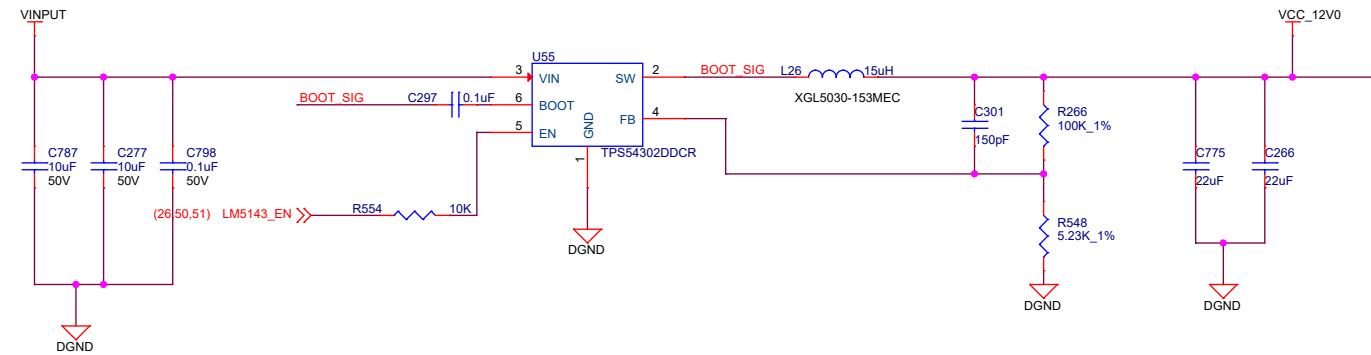
TI WEBENCH Simulation Inputs:
 Vin (min) = 15V Vin (max) = 25V
 Vout = 3.3V@30A
 Ta = 25 deg



POWER SUPPLY #2

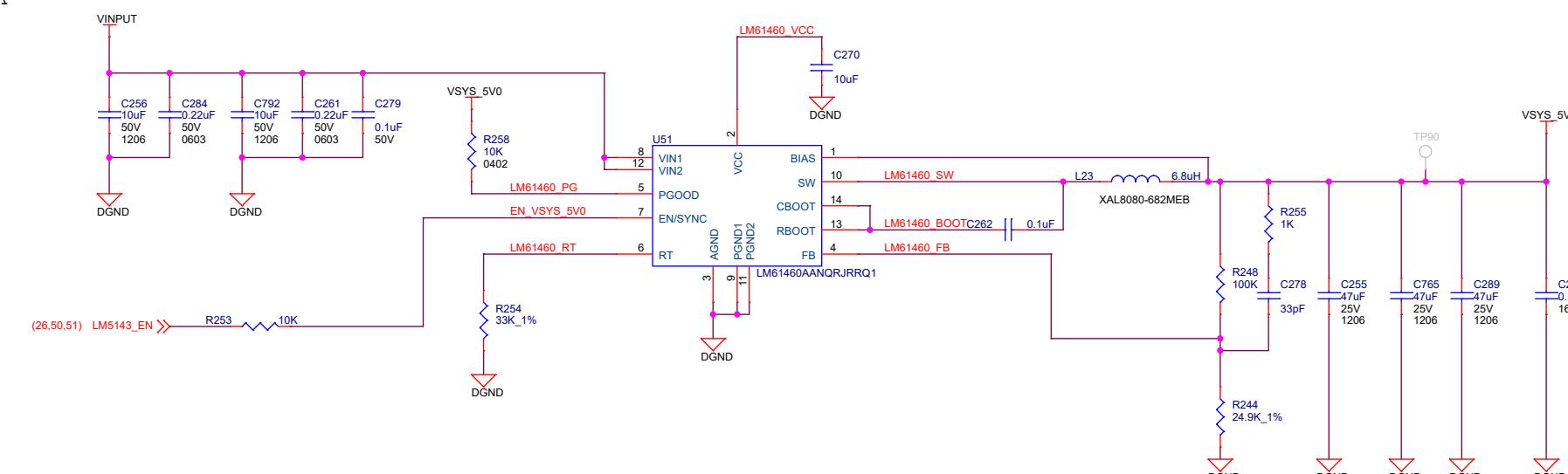
TI WEBENCH Simulation Inputs:
 Vin (min) = 15V Vin (max) = 25V
 Vout = 12V@3A
 Ta = 25 deg

12V GENERATION



LM61460 5V BUCK REGULATOR
 VinMin = 12V
 VinMax = 25V
 Vout = 5.0V
 Iout = 6A

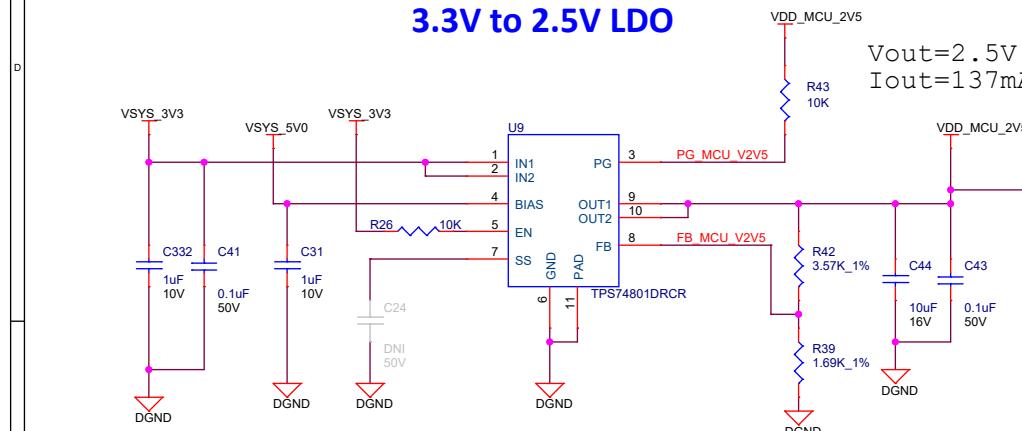
5V GENERATION



POWER SUPPLY #3

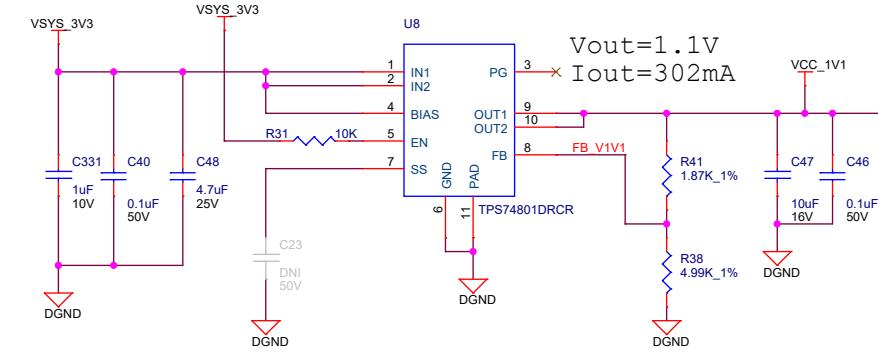
ETHERNET POWER- MCU RGMII

3.3V to 2.5V LDO

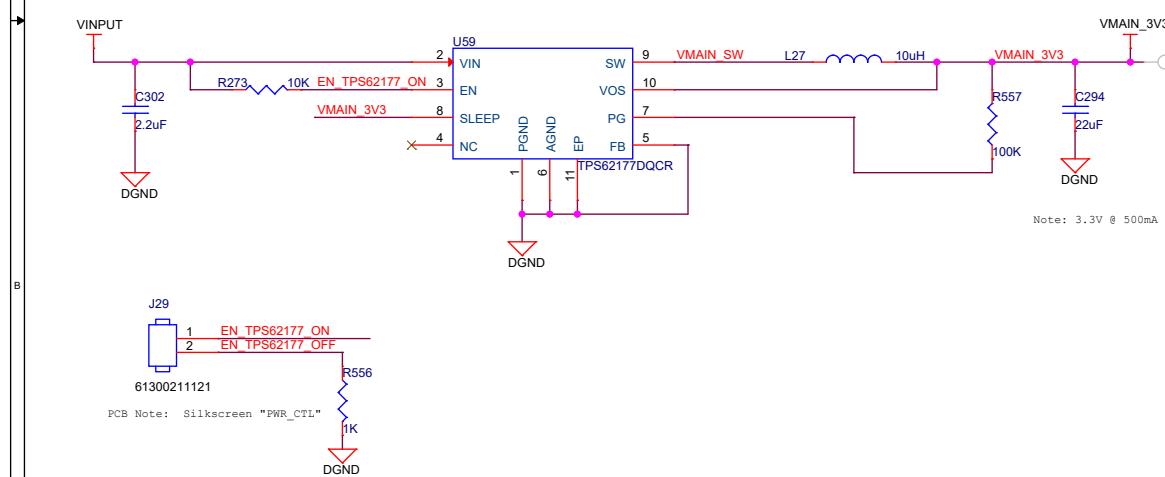


USB HUB POWER & ETHERNET POWER - RGMII1

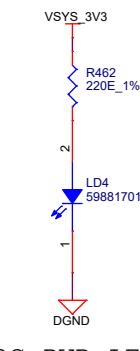
3.3V to 1.1V LDO



SYSTEM MANAGEMENT 3.3V REGULATOR

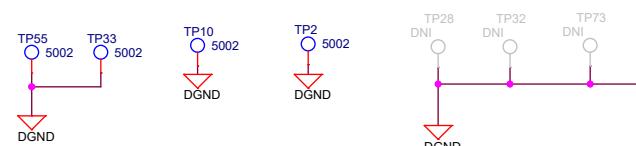


POWER INDICATION LED's



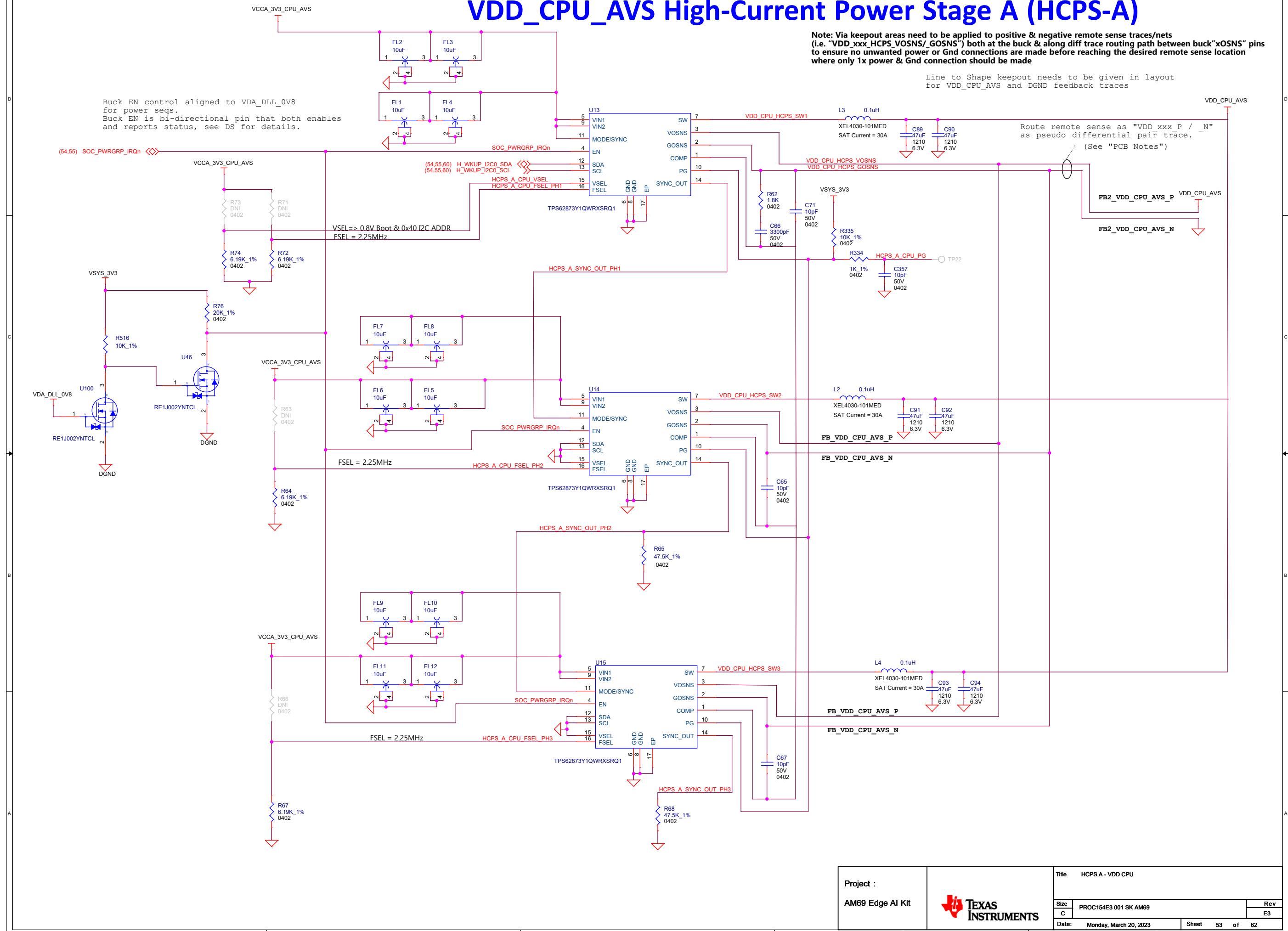
SOC PWR LED

GROUND TEST POINTS

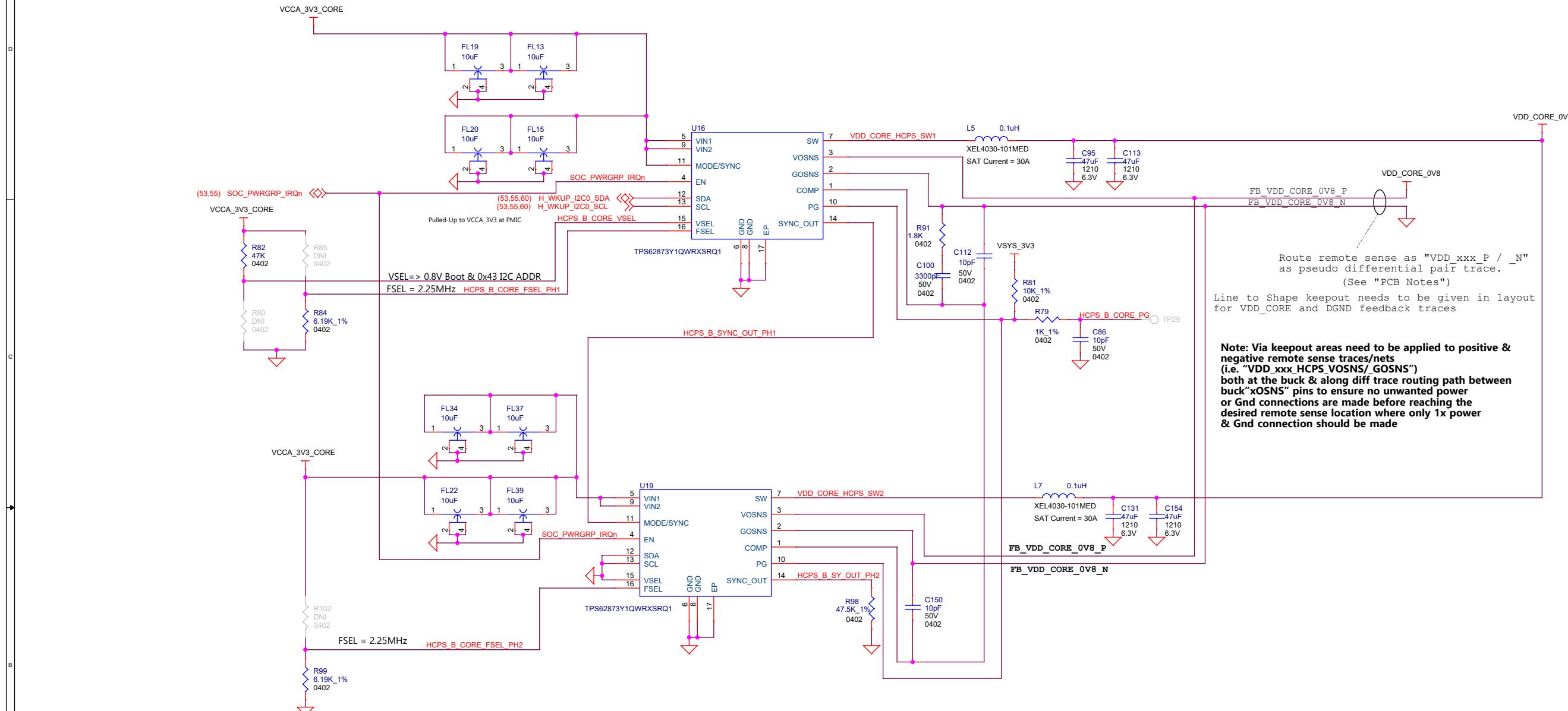


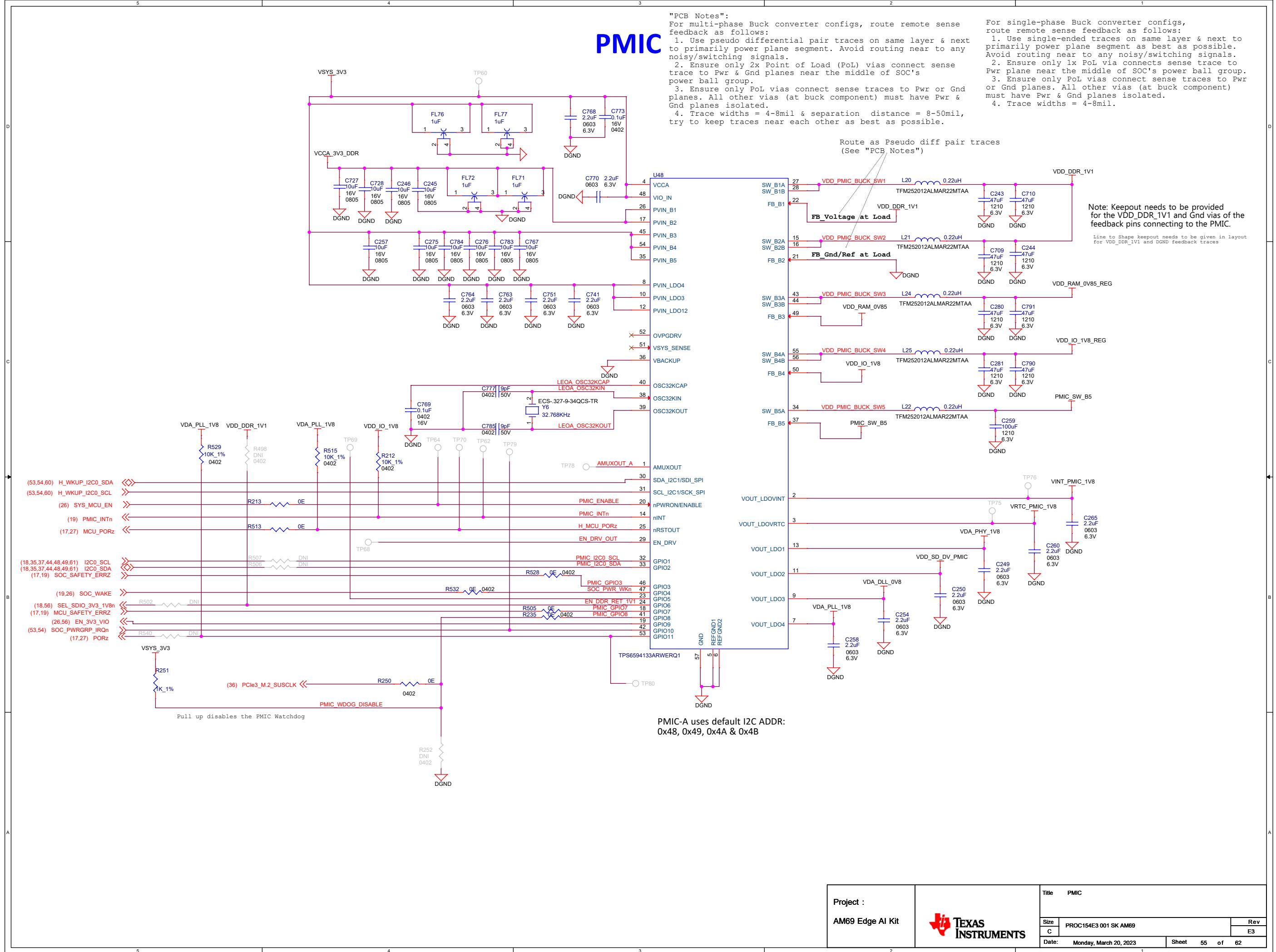
PCB NOTE: Spread the SMD test points Top and Bottom Side of PCB

VDD_CPU_AVs High-Current Power Stage A (HCPS-A)

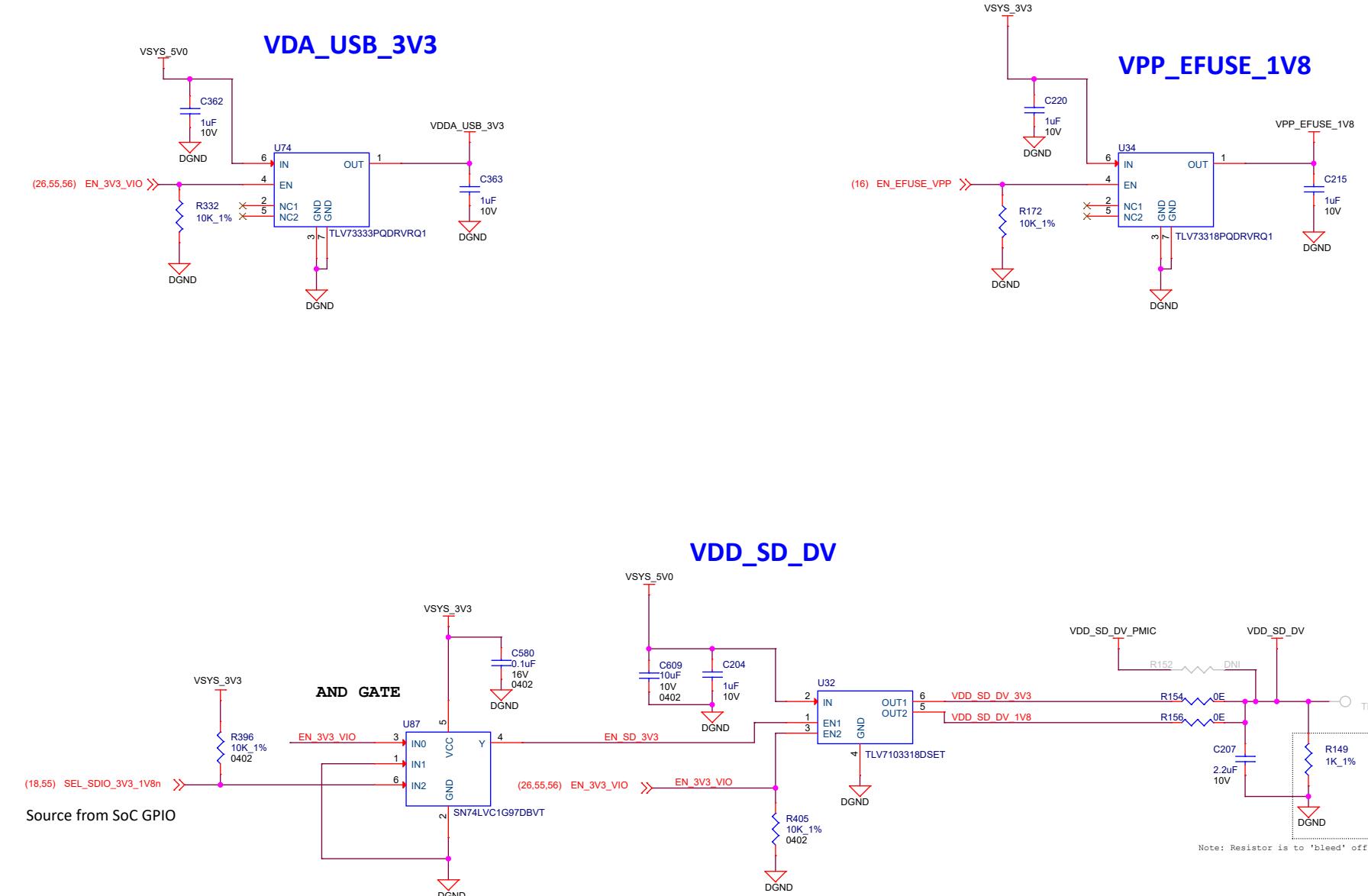


VDD_CORE_0V8 High-Current Power Stage A (HCPS-B)





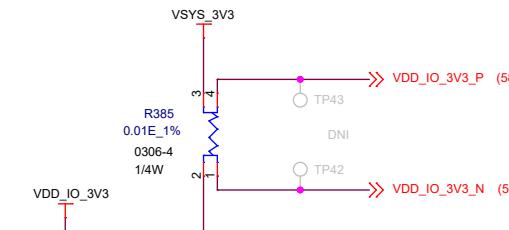
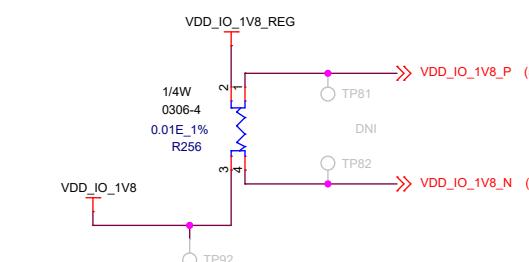
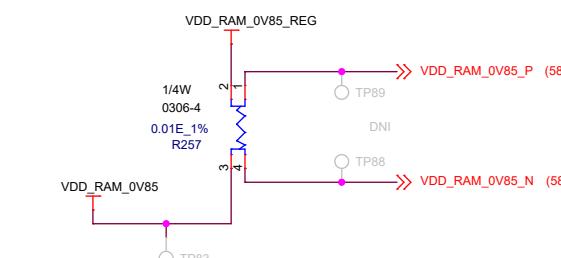
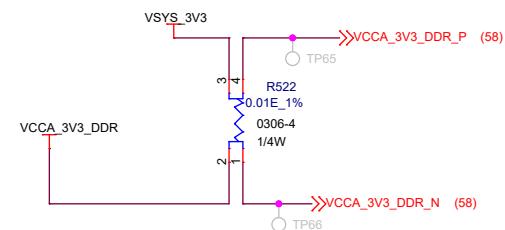
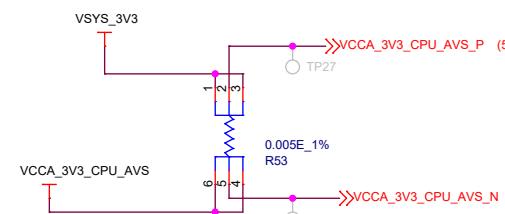
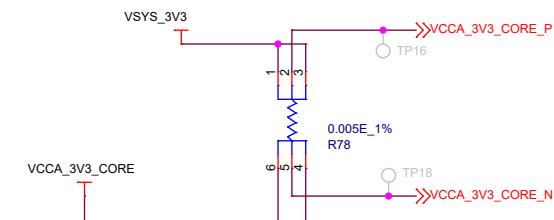
LDOs



Project : AM69 Edge AI Kit	Title : SOC - LDO's
Size : C Rev : E3	Date: Monday, March 20, 2023

SOC Current Sense Resistors

CORE, AVS and DDR input supply sense resistors

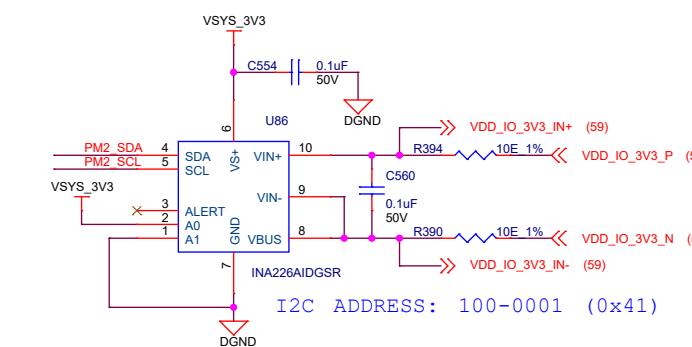
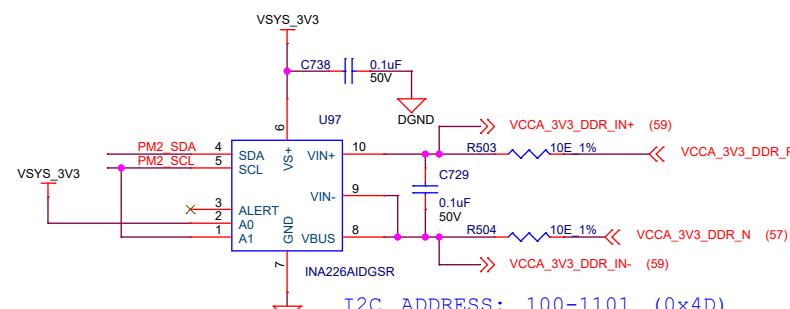
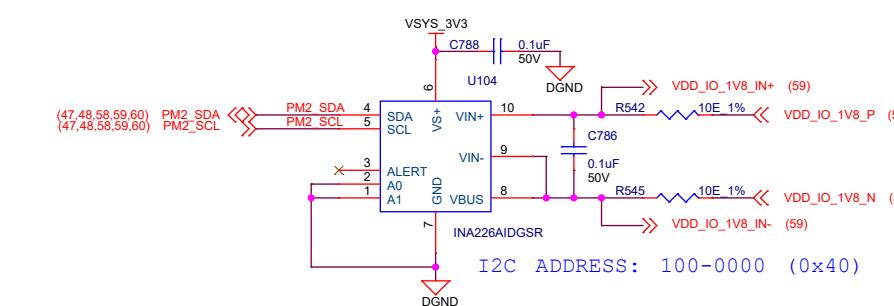
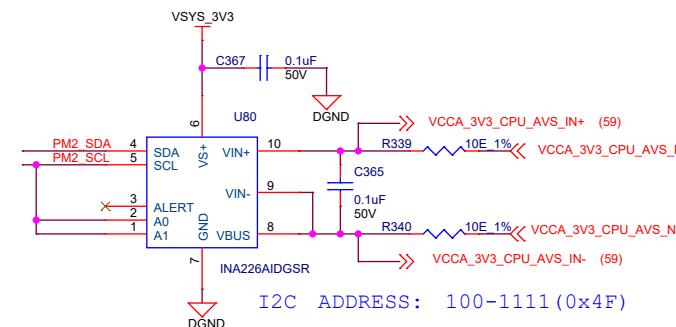
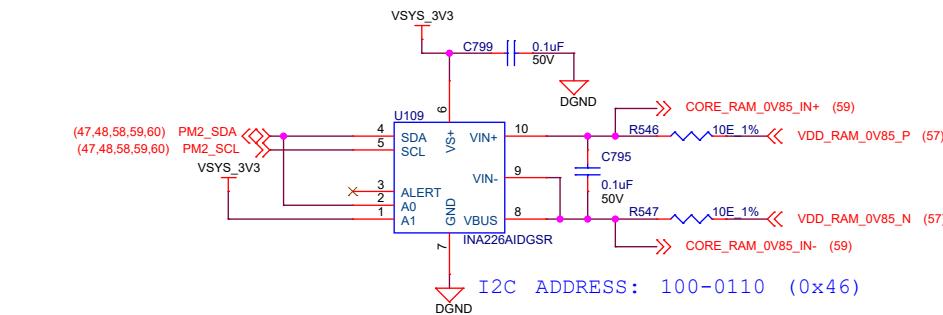
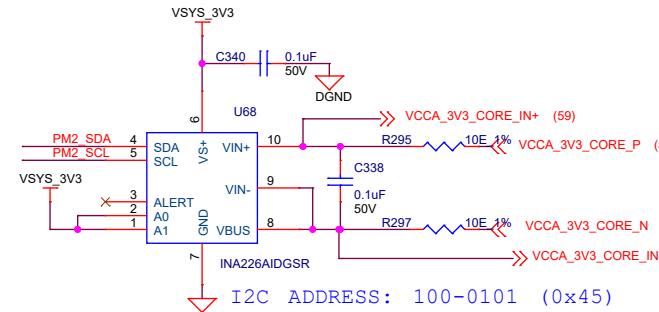


PCB Note: Place all SMT TPs
on PCB top-side & on top of via at
Bd-to-Bd connector

VDD_CPU_AVN
TP30
VDD_CORE_0V8
TP31
VDA_PLL_1V8
TP74
VDA_DLL_0V8
TP72
VDD_DDR_1V1
TP56
VDDA_USB_3V3
TP25

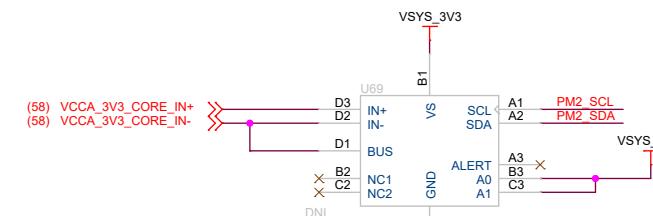
Note: The design supports current/voltage measurements using either INA226 or INA231. The SK will be assembled with either INA226 or INA231, but not both (implemented via dual or stacked PCB footprint). These two INA devices are register compatible so functionality and performance should not be impacted with either INA

CURRENT MONITORS - INA226

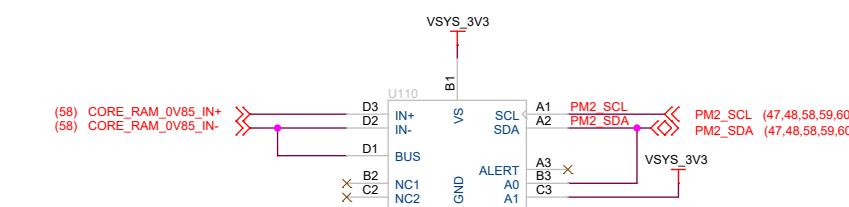


Note: The design supports current/voltage measurements using either INA226 or INA231. The SK will be assembled with either INA226 or INA231, but not both (implemented via dual or stacked PCB footprint). These two INA devices are register compatible so functionality and performance should not be impacted with either INA

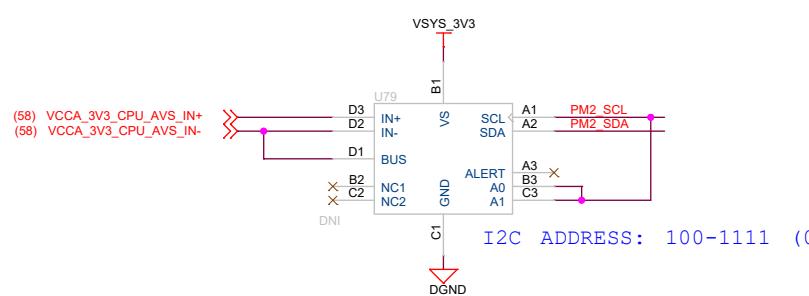
CURRENT MONITORS - INA231



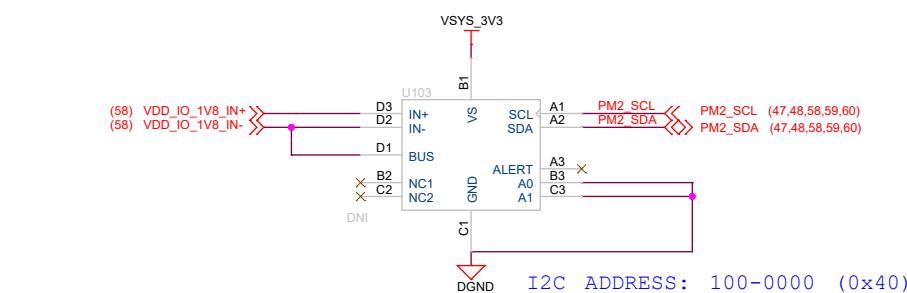
I2C ADDRESS: 100-0101 (0x45)



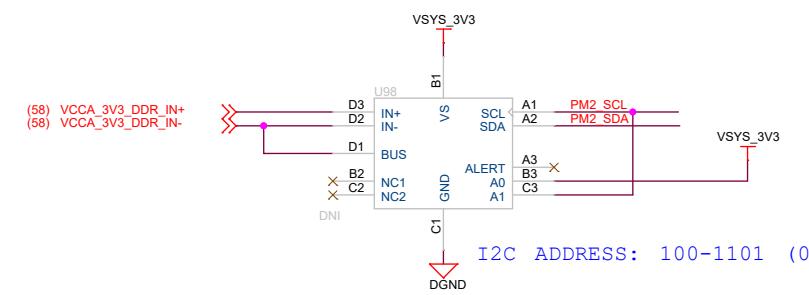
I2C ADDRESS: 100-0110 (0x46)



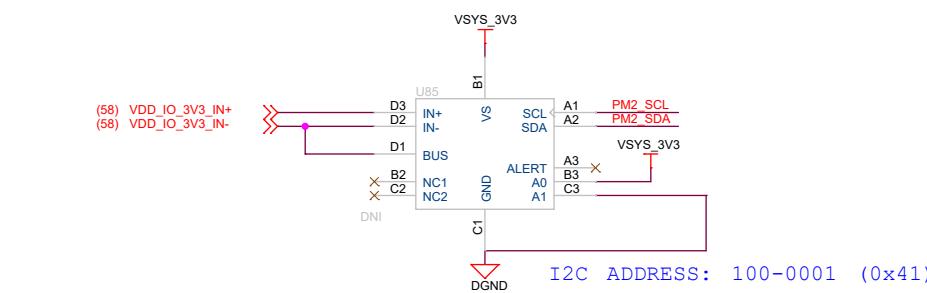
I2C ADDRESS: 100-1111 (0x4F)



I2C ADDRESS: 100-0000 (0x40)

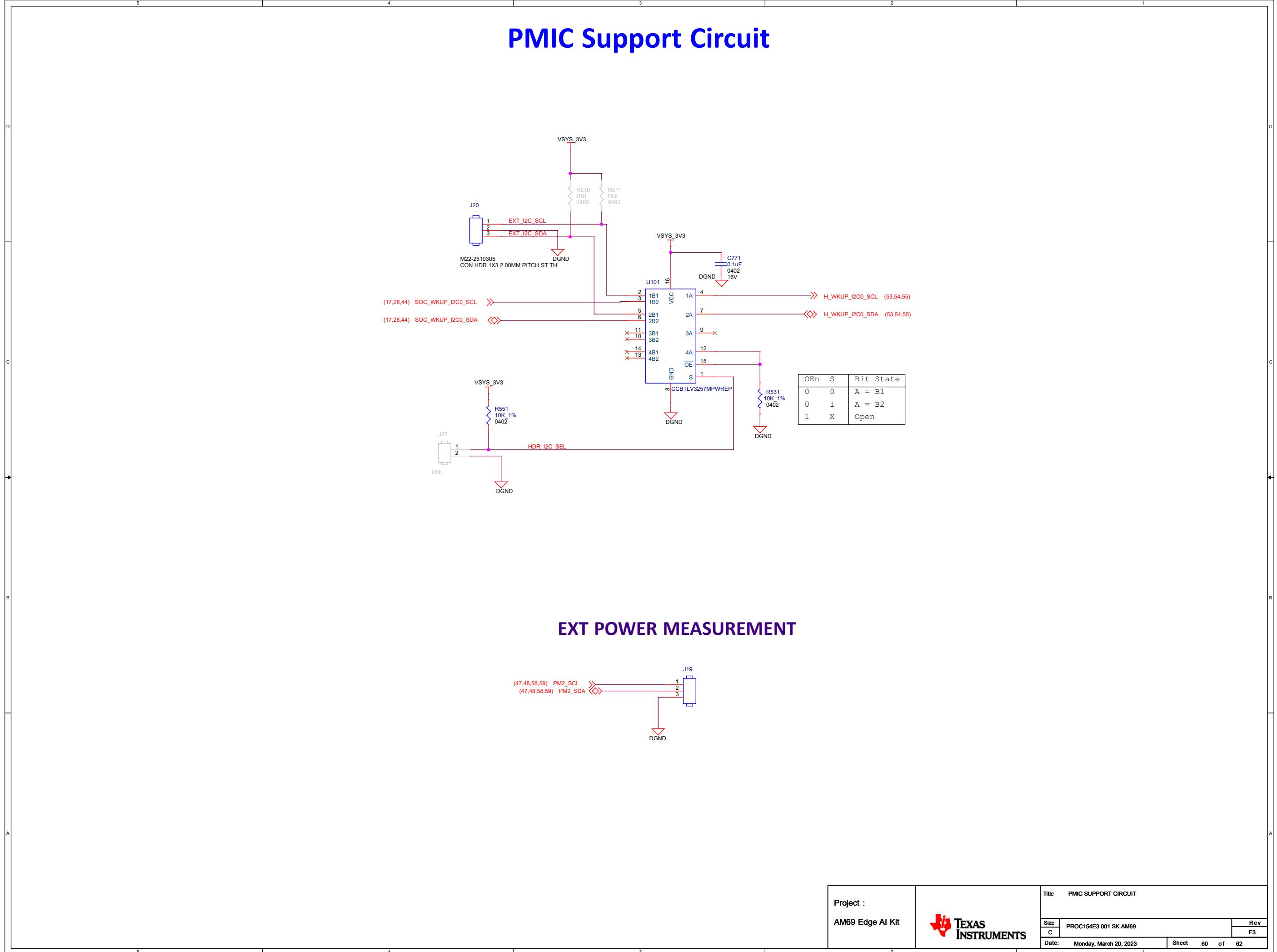


I2C ADDRESS: 100-1101 (0x4D)



I2C ADDRESS: 100-0001 (0x41)

PMIC Support Circuit

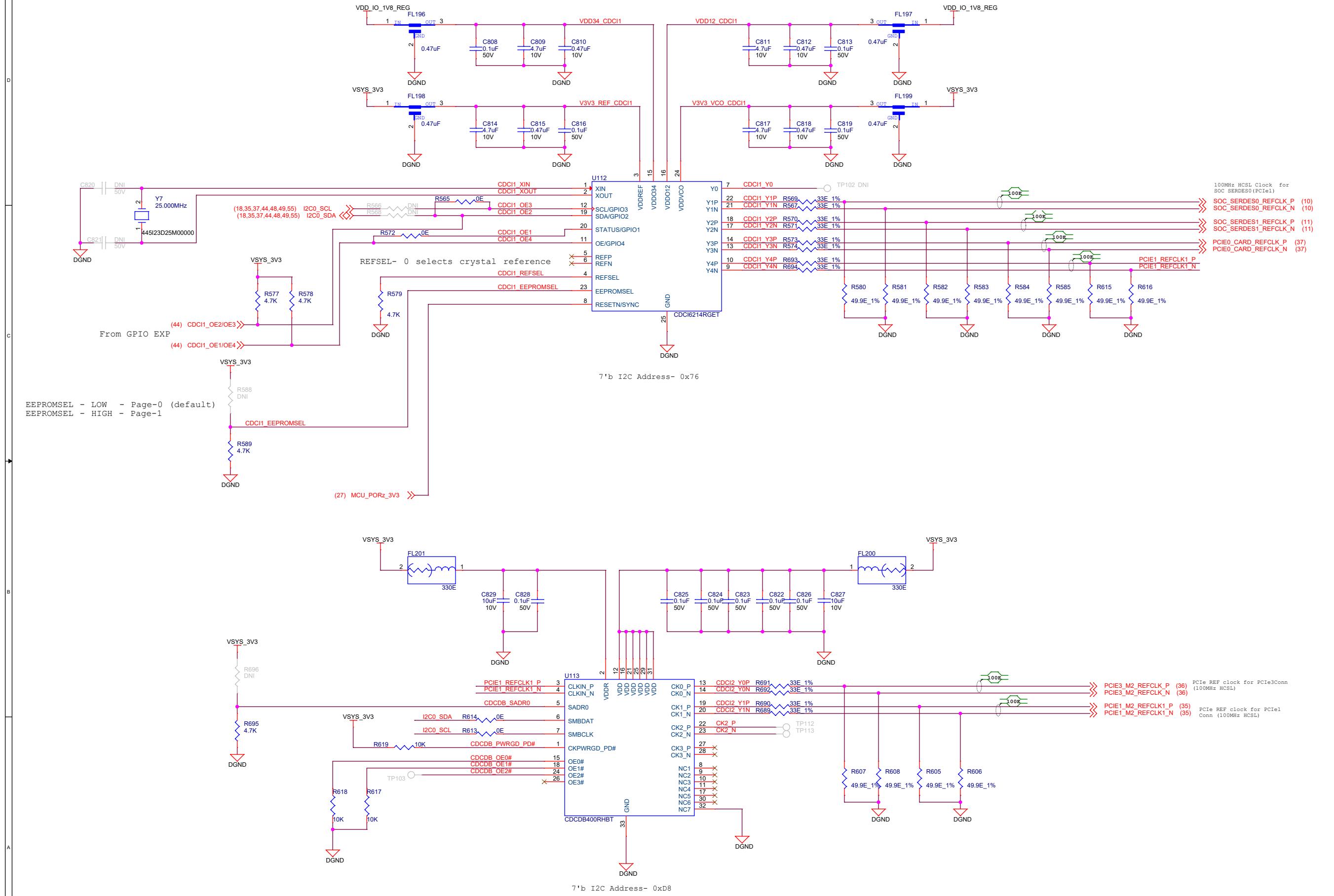


EXT POWER MEASUREMENT

Project :	AM69 Edge AI Kit	Title	PMIC SUPPORT CIRCUIT
Size	PROC154E3 001 SK AM69	Rev	E3
C		Date:	Monday, March 20, 2023
		Sheet	60 of 62

TEXAS
INSTRUMENTS

SERDES CLOCK GENERATORS



Project :



SERDES CLOCK GENERATORS

PROC154E3 001 SK AM69

NOTES, HW & LABELS

ASSEMBLY NOTES

- All MSL components should be baked as per JEDEC standard.
- PCB should be baked at 120 degree for 8 hours.
- Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
- These assemblies are ESD sensitive, ESD precautions shall be observed.
- These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- Provide serial numbers to the assembled boards for identification.
- The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

LABELS

Board Serial No.



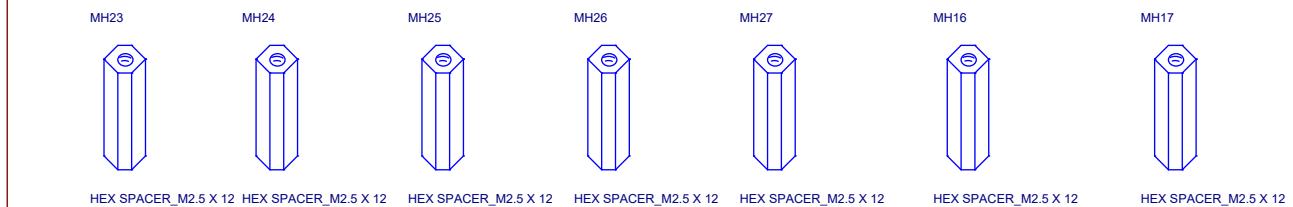
Assembly Revision.



SCREWS



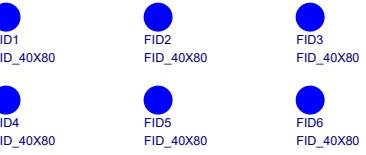
STANDOFFS



WASHER



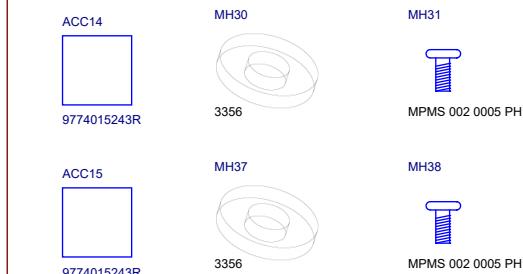
FIDUCIALS



BARE PCB



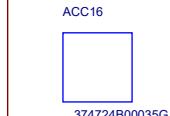
SCREW & WASHER FOR PCIe M.2



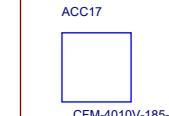
LOGOs



HEAT SINK



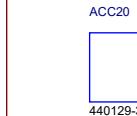
FAN



CRIMP PIN



CONN HOUSING



SCREW FOR FAN ASSEMBLY

