
STM32
CubeMX

1. Description

1.1. Project

Project Name	PLC STM32
Board Name	custom
Generated with:	STM32CubeMX 6.3.0
Date	08/18/2021

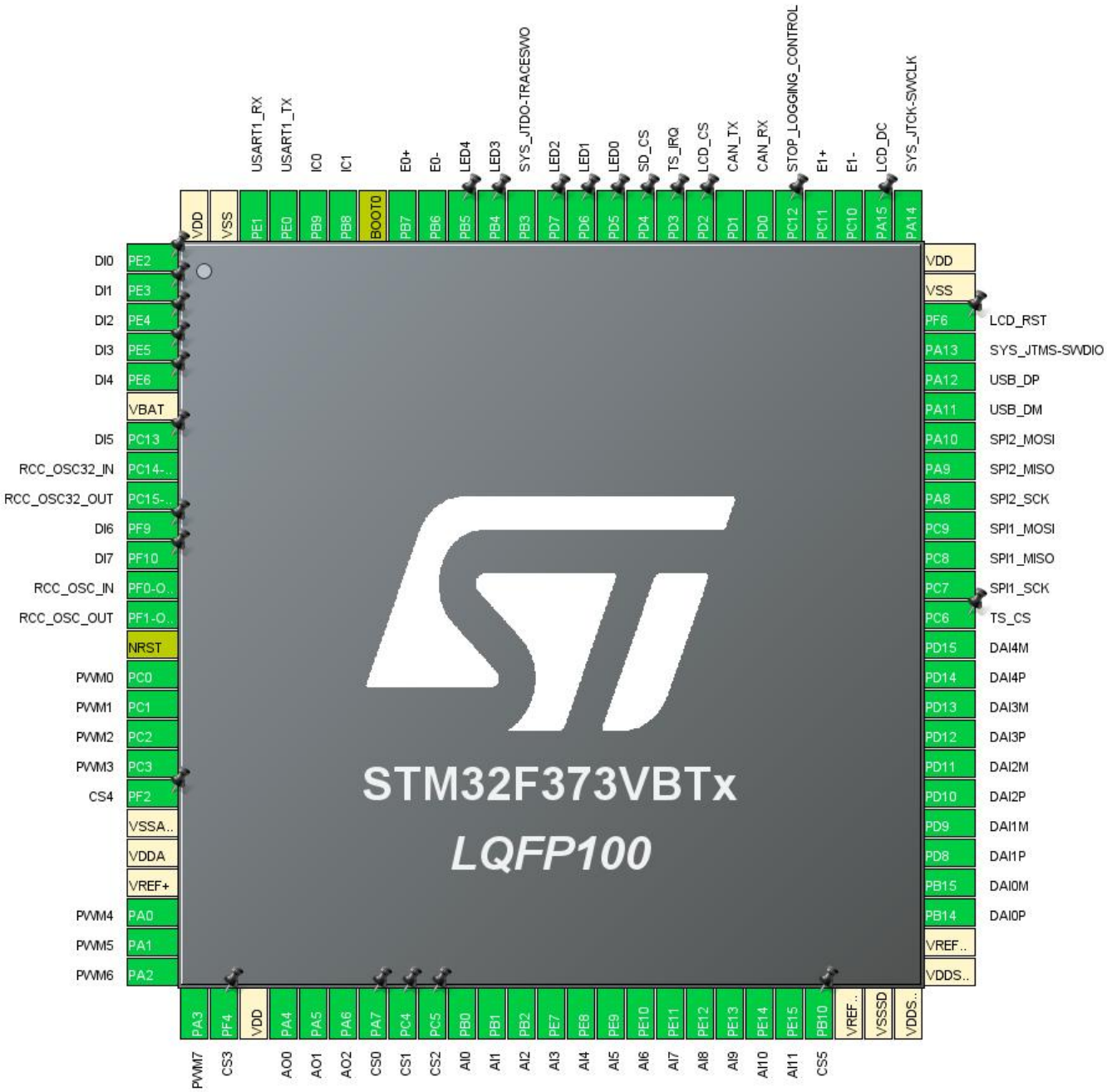
1.2. MCU

MCU Series	STM32F3
MCU Line	STM32F373
MCU name	STM32F373VBTx
MCU Package	LQFP100
MCU Pin number	100

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration



3. Pins Configuration

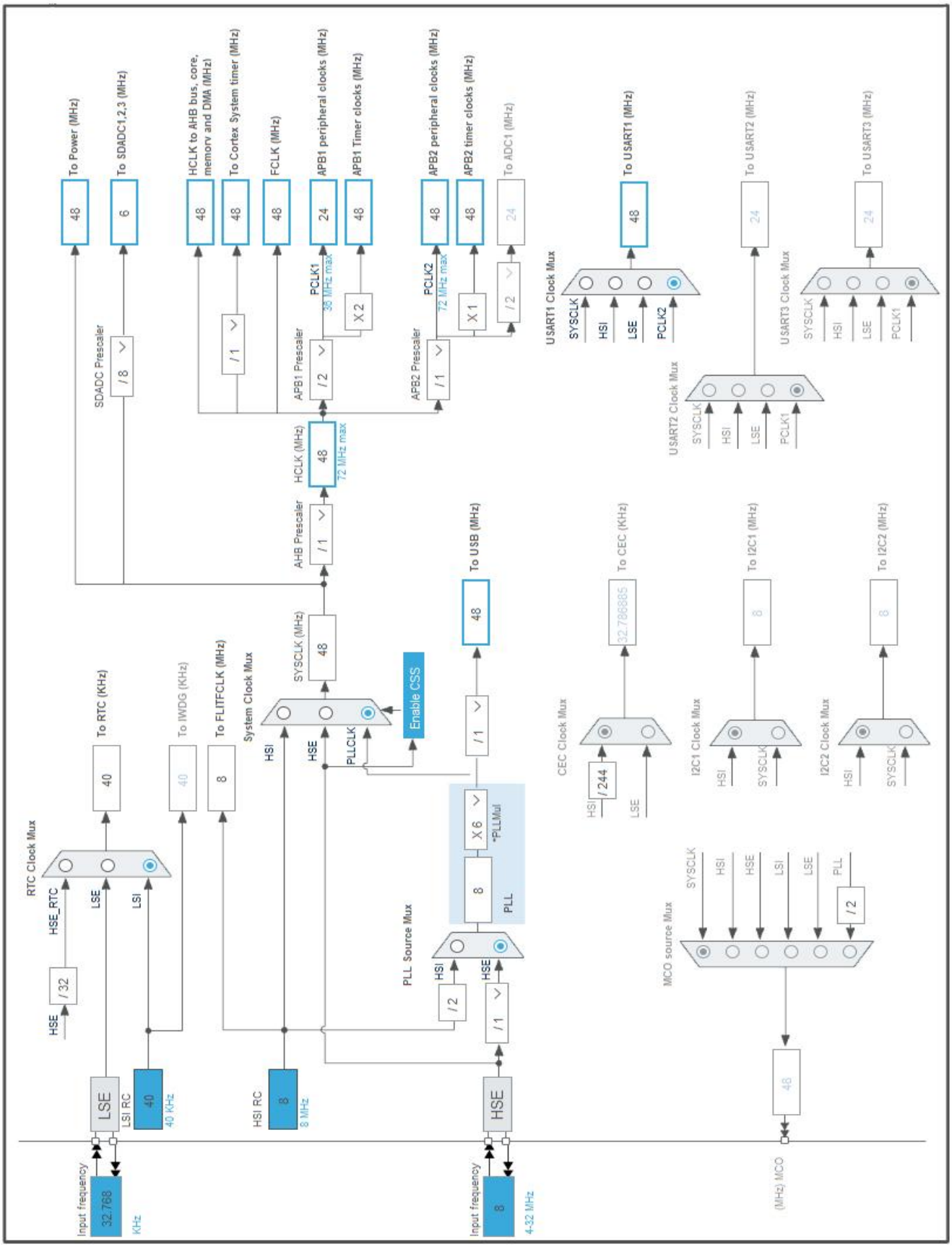
Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Input	DI0
2	PE3 *	I/O	GPIO_Input	DI1
3	PE4 *	I/O	GPIO_Input	DI2
4	PE5 *	I/O	GPIO_Input	DI3
5	PE6 *	I/O	GPIO_Input	DI4
6	VBAT	Power		
7	PC13 *	I/O	GPIO_Input	DI5
8	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
10	PF9 *	I/O	GPIO_Input	DI6
11	PF10 *	I/O	GPIO_Input	DI7
12	PF0-OSC_IN	I/O	RCC_OSC_IN	
13	PF1-OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
15	PC0	I/O	TIM5_CH1	PWM0
16	PC1	I/O	TIM5_CH2	PWM1
17	PC2	I/O	TIM5_CH3	PWM2
18	PC3	I/O	TIM5_CH4	PWM3
19	PF2 *	I/O	GPIO_Output	CS4
20	VSSA/VREF-	Power		
21	VDDA	Power		
22	VREF+	Power		
23	PA0	I/O	TIM2_CH1	PWM4
24	PA1	I/O	TIM2_CH2	PWM5
25	PA2	I/O	TIM2_CH3	PWM6
26	PA3	I/O	TIM2_CH4	PWM7
27	PF4 *	I/O	GPIO_Output	CS3
28	VDD	Power		
29	PA4	I/O	DAC1_OUT1	AO0
30	PA5	I/O	DAC1_OUT2	AO1
31	PA6	I/O	DAC2_OUT1	AO2
32	PA7 *	I/O	GPIO_Output	CS0
33	PC4 *	I/O	GPIO_Output	CS1
34	PC5 *	I/O	GPIO_Output	CS2
35	PB0	I/O	SDADC1_AIN6P	AI0
36	PB1	I/O	SDADC1_AIN5P	AI1

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
37	PB2	I/O	SDADC1_AIN4P	AI2
38	PE7	I/O	SDADC1_AIN3P	AI3
39	PE8	I/O	SDADC1_AIN8P	AI4
40	PE9	I/O	SDADC1_AIN7P	AI5
41	PE10	I/O	SDADC1_AIN2P	AI6
42	PE11	I/O	SDADC1_AIN1P	AI7
43	PE12	I/O	SDADC1_AIN0P	AI8
44	PE13	I/O	SDADC2_AIN2P	AI9
45	PE14	I/O	SDADC2_AIN1P	AI10
46	PE15	I/O	SDADC2_AIN0P	AI11
47	PB10 *	I/O	GPIO_Output	CS5
48	VREFSD-	Power		
49	VSSSD	Power		
50	VDDSD12	Power		
51	VDDSD3	Power		
52	VREFSD+	Power		
53	PB14	I/O	SDADC3_AIN8P	DAI0P
54	PB15	I/O	SDADC3_AIN8M	DAI0M
55	PD8	I/O	SDADC3_AIN6P	DAI1P
56	PD9	I/O	SDADC3_AIN6M	DAI1M
57	PD10	I/O	SDADC3_AIN4P	DAI2P
58	PD11	I/O	SDADC3_AIN4M	DAI2M
59	PD12	I/O	SDADC3_AIN2P	DAI3P
60	PD13	I/O	SDADC3_AIN2M	DAI3M
61	PD14	I/O	SDADC3_AIN0P	DAI4P
62	PD15	I/O	SDADC3_AIN0M	DAI4M
63	PC6 *	I/O	GPIO_Output	TS_CS
64	PC7	I/O	SPI1_SCK	
65	PC8	I/O	SPI1_MISO	
66	PC9	I/O	SPI1_MOSI	
67	PA8	I/O	SPI2_SCK	
68	PA9	I/O	SPI2_MISO	
69	PA10	I/O	SPI2_MOSI	
70	PA11	I/O	USB_DM	
71	PA12	I/O	USB_DP	
72	PA13	I/O	SYS_JTMS-SWDIO	
73	PF6 *	I/O	GPIO_Output	LCD_RST
74	VSS	Power		
75	VDD	Power		

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
76	PA14	I/O	SYS_JTCK-SWCLK	
77	PA15 *	I/O	GPIO_Output	LCD_DC
78	PC10	I/O	TIM19_CH1	E1-
79	PC11	I/O	TIM19_CH2	E1+
80	PC12 *	I/O	GPIO_Input	STOP_LOGGING_CONTROL
81	PD0	I/O	CAN_RX	
82	PD1	I/O	CAN_TX	
83	PD2 *	I/O	GPIO_Output	LCD_CS
84	PD3 *	I/O	GPIO_Input	TS_IRQ
85	PD4 *	I/O	GPIO_Output	SD_CS
86	PD5 *	I/O	GPIO_Output	LED0
87	PD6 *	I/O	GPIO_Output	LED1
88	PD7 *	I/O	GPIO_Output	LED2
89	PB3	I/O	SYS_JTDO-TRACESWO	
90	PB4 *	I/O	GPIO_Output	LED3
91	PB5 *	I/O	GPIO_Output	LED4
92	PB6	I/O	TIM4_CH1	E0-
93	PB7	I/O	TIM4_CH2	E0+
94	BOOT0	Boot		
95	PB8	I/O	TIM16_CH1	IC1
96	PB9	I/O	TIM17_CH1	IC0
97	PE0	I/O	USART1_TX	
98	PE1	I/O	USART1_RX	
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	PLC STM32
Project Folder	C:\Users\danie\Documents\STM32CubeIDE-Workspace\PLC STM32
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F3 V1.11.3
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_DAC1_Init	DAC1
4	MX_DAC2_Init	DAC2
5	MX_RTC_Init	RTC
6	MX_SPI2_Init	SPI2
7	MX_TIM2_Init	TIM2
8	MX_TIM5_Init	TIM5
9	MX_SPI1_Init	SPI1
10	MX_TIM4_Init	TIM4
11	MX_SDADC1_Init	SDADC1

Rank	Function Name	Peripheral Instance Name
12	MX_SDADC2_Init	SDADC2
13	MX_SDADC3_Init	SDADC3
14	MX_CAN_Init	CAN
15	MX_USART1_UART_Init	USART1
16	MX_TIM6_Init	TIM6
17	MX_TIM12_Init	TIM12
18	MX_TIM13_Init	TIM13
19	MX_TIM16_Init	TIM16
20	MX_USB_DEVICE_Init	USB_DEVICE
21	MX_FATFS_Init	FATFS
22	MX_TIM17_Init	TIM17
23	MX_DMA_Init	DMA
24	MX_TIM19_Init	TIM19

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F3
Line	STM32F373
MCU	STM32F373VBTx
Datasheet	DS8845_Rev7

6.2. Parameter Selection

Temperature	25
Vdd	3.6

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

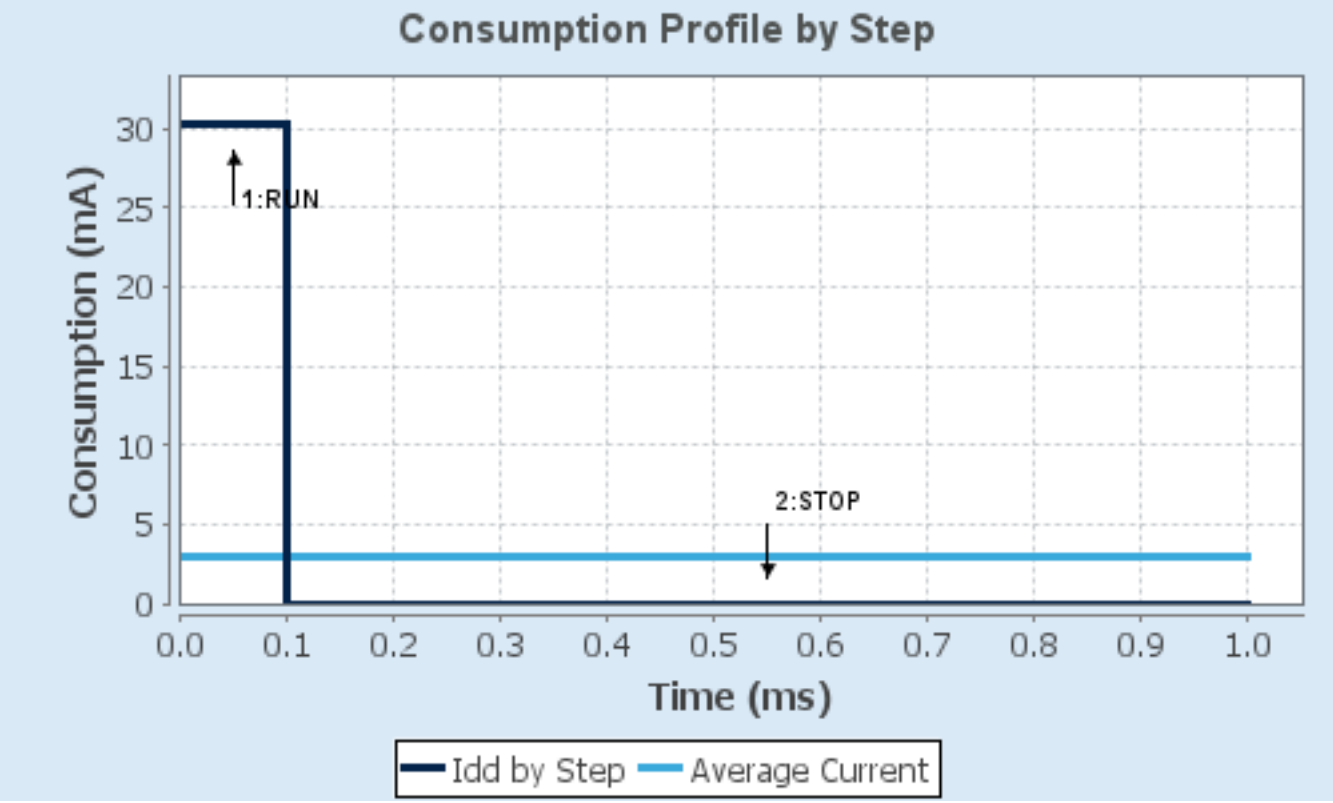
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.6	3.6
Voltage Source	Battery	Battery
Range	No Scale	No Scale
Fetch Type	RAM	n/a
CPU Frequency	72 MHz	0 Hz
Clock Configuration	HSEBYP PLL	Regulator_LP
Clock Source Frequency	8 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	30.25 mA	10.9 µA
Duration	0.1 ms	0.9 ms
DMIPS	90.0	0.0
Ta Max	99.99	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	3.03 mA
Battery Life	1 month, 16 days, 4 hours	Average DMIPS	90.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
30
25
20
15
10
5
0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. CAN

mode: Activated

7.1.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum)	16
Time Quantum	**666.6666666666666 ***
Time Quanta in Bit Segment 1	**3 Times ***
Time Quanta in Bit Segment 2	**2 Times ***
Time for one Bit	**3999.99 ***
Baud Rate	**250000 ***
ReSynchronization Jump Width	1 Time

Basic Parameters:

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	Disable
Automatic Wake-Up Mode	Disable
Automatic Retransmission	Disable
Receive Fifo Locked Mode	Disable
Transmit Fifo Priority	Disable

Advanced Parameters:

Operating Mode	Normal

7.2. DAC1

mode: OUT1 Configuration

mode: OUT2 Configuration

7.2.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	Enable
Trigger	**Timer 6 Trigger Out event ***
Wave generation mode	Disabled

DAC Out2 Settings:

Output Buffer	Enable
Trigger	**Timer 6 Trigger Out event ***
Wave generation mode	Disabled

7.3. DAC2

mode: OUT1 Configuration

7.3.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	Enable
Trigger	**Timer 6 Trigger Out event ***

7.4. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	1 WS (2 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

7.5. RTC

mode: Activate Clock Source

mode: Activate Calendar

Alarm A: Internal Alarm A

Alarm B: Internal Alarm B

7.5.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255

Calendar Time:

Data Format	**Binary data format ***
Hours	0
Minutes	0
Seconds	0
Day Light Saving: value of hour adjustment	Daylightsaving None
Store Operation	Storeoperation Reset

Calendar Date:

Week Day	Monday
Month	January
Date	1
Year	0

Alarm A:

Hours	0
Minutes	0
Seconds	0
Sub Seconds	0
Alarm Mask Date Week day	Disable
Alarm Mask Hours	Disable
Alarm Mask Minutes	Disable
Alarm Mask Seconds	Disable
Alarm Sub Second Mask	All Alarm SS fields are masked.
Alarm Date Week Day Sel	Date
Alarm Date	1

Alarm B:

Hours	0
Minutes	0
Seconds	0
Sub Seconds	0
Alarm Mask Date Week day	Disable
Alarm Mask Hours	Disable
Alarm Mask Minutes	Disable
Alarm Mask Seconds	Disable
Alarm Sub Second Mask	All Alarm SS fields are masked.
Alarm Date Week Day Sel	**Weekday ***
Alarm Week Day	Monday

7.6. SDADC1

IN0: IN0-Single-Ended zero reference

IN1: IN1-Single-Ended zero reference
IN2: IN2-Single-Ended zero reference
IN3: IN3-Single-Ended zero reference
IN4: IN4-Single-Ended zero reference
IN5: IN5-Single-Ended zero reference
IN6: IN6-Single-Ended zero reference
IN7: IN7-Single-Ended zero reference
IN8: IN8-Single-Ended zero reference
mode: Conversion Configuration 0
mode: Conversion Configuration 1
mode: Conversion Configuration 2

7.6.1. Parameter Settings:

General Settings:

Low Power Mode	None
Fast Conversion Mode	Disable
Slow Clock Mode	Disable
Reference Voltage	Forced externally using VREF pin

Conversion Configuration 0:

Input Mode	**Single-ended zero-volt reference mode ***
Gain	equal to 1
Common Mode	SDADC VSSA
Offset	0

Conversion Configuration 1:

Input Mode	**Single-ended zero-volt reference mode ***
Gain	equal to 1
Common Mode	SDADC VSSA
Offset	0

Conversion Configuration 2:

Input Mode	**Single-ended zero-volt reference mode ***
Gain	equal to 1
Common Mode	SDADC VSSA
Offset	0

SDADC Regular Conversions Settings:

Enable Regular Conversion	Disable

SDADC Injected Conversions Settings:

Enable Injected Conversion	**Enable ***
Number of Channels To be converted	**9 ***

Trigger type	**External trigger ***
External Trigger Edge	Rising edge
External Trigger source	Timer 13 Capture Compare 1
Injected Delay	Disable
Injected Multimode type	Disable
Continuous Mode	**Enabled ***
Channel Configuration	1
Channel	Channel 0
Configuration Index	Configuration 0
Channel Configuration	**2 ***
Channel	Channel 1
Configuration Index	Configuration 0
Channel Configuration	**3 ***
Channel	Channel 2
Configuration Index	Configuration 0
Channel Configuration	**4 ***
Channel	Channel 3
Configuration Index	**Configuration 1 ***
Channel Configuration	**5 ***
Channel	Channel 4
Configuration Index	**Configuration 1 ***
Channel Configuration	**6 ***
Channel	Channel 5
Configuration Index	**Configuration 1 ***
Channel Configuration	**7 ***
Channel	Channel 6
Configuration Index	**Configuration 2 ***
Channel Configuration	**8 ***
Channel	Channel 7
Configuration Index	**Configuration 2 ***
Channel Configuration	**9 ***
Channel	Channel 8
Configuration Index	**Configuration 2 ***

7.7. SDADC2

IN0: IN0-Single-Ended zero reference

IN1: IN1-Single-Ended zero reference

IN2: IN2-Single-Ended zero reference
mode: Conversion Configuration 0
mode: Conversion Configuration 1
mode: Conversion Configuration 2

7.7.1. Parameter Settings:

General Settings:

Low Power Mode	None
Fast Conversion Mode	Disable
Slow Clock Mode	Disable
Reference Voltage	Forced externally using VREF pin

Conversion Configuration 0:

Input Mode	**Single-ended zero-volt reference mode ***
Gain	equal to 1
Common Mode	SDADC VSSA
Offset	0

Conversion Configuration 1:

Input Mode	**Single-ended zero-volt reference mode ***
Gain	equal to 1
Common Mode	SDADC VSSA
Offset	0

Conversion Configuration 2:

Input Mode	**Single-ended zero-volt reference mode ***
Gain	equal to 1
Common Mode	SDADC VSSA
Offset	0

SDADC Regular Conversions Settings:

Enable Regular Conversion	Disable

SDADC Injected Conversions Settings:

Enable Injected Conversion	**Enable ***
Number of Channels To be converted	**3 ***
Trigger type	**External trigger ***
External Trigger Edge	Rising edge
External Trigger source	**Timer 12 Capture Compare 1 ***
Injected Delay	Disable
Continuous Mode	**Enabled ***
Channel Configuration	1
Channel	Channel 0
Configuration Index	Configuration 0

Channel Configuration	**2 ***
Channel	Channel 1
Configuration Index	**Configuration 1 ***
Channel Configuration	**3 ***
Channel	Channel 2
Configuration Index	**Configuration 2 ***

7.8. SDADC3

IN0: IN0-Differential

IN2: IN2-Differential

IN4: IN4-Differential

IN6: IN6-Differential

IN8: IN8-Differential

mode: Conversion Configuration 0

mode: Conversion Configuration 1

mode: Conversion Configuration 2

7.8.1. Parameter Settings:

General Settings:

Low Power Mode	None
Fast Conversion Mode	Disable
Slow Clock Mode	Disable
Reference Voltage	Forced externally using VREF pin

Conversion Configuration 0:

Input Mode	Differential mode
Gain	equal to 1
Common Mode	SDADC VSSA
Offset	0

Conversion Configuration 1:

Input Mode	Differential mode
Gain	equal to 1
Common Mode	SDADC VSSA
Offset	0

Conversion Configuration 2:

Input Mode	Differential mode
Gain	equal to 1
Common Mode	SDADC VSSA
Offset	0

SDADC Regular Conversions Settings:

Enable Regular Conversion	Disable

SDADC Injected Conversions Settings:

Enable Injected Conversion	**Enable ***
Number of Channels To be converted	**5 ***
Trigger type	**External trigger ***
External Trigger Edge	Rising edge
External Trigger source	**Timer 12 Capture Compare 2 ***
Injected Delay	Disable
Continuous Mode	**Enabled ***
Channel Configuration	1
Channel	Channel 0
Configuration Index	Configuration 0
Channel Configuration	**2 ***
Channel	Channel 2
Configuration Index	Configuration 0
Channel Configuration	**3 ***
Channel	Channel 4
Configuration Index	**Configuration 1 ***
Channel Configuration	**4 ***
Channel	Channel 6
Configuration Index	**Configuration 1 ***
Channel Configuration	**5 ***
Channel	Channel 8
Configuration Index	**Configuration 2 ***

7.9. SPI1

Mode: Full-Duplex Master

7.9.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**4 ***
Baud Rate	**12.0 MBits/s ***

Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

7.10. SPI2

Mode: Full-Duplex Master

7.10.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**256 ***
Baud Rate	**93.75 KBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

7.11. SYS

Debug: Trace Asynchronous Sw

Timebase Source: SysTick

7.12. TIM2

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

7.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**0xffff ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.13. TIM4

Combined Channels: Encoder Mode

7.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

7.14. TIM5

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

7.14.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**0xffff ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.15. TIM6

mode: Activated

7.15.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**99 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**0xbb80 ***
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	**Update Event ***

7.16. TIM12

mode: Clock Source

Channel1: Output Compare No Output

Channel2: Output Compare No Output

7.16.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**0xbb80 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Output Compare No Output Channel 1:

Mode	**Toggle on match ***
Pulse (16 bits value)	0
Output compare preload	Disable
CH Polarity	High

Output Compare No Output Channel 2:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
Output compare preload	Disable
CH Polarity	High

7.17. TIM13

mode: Activated

Channel1: Output Compare No Output

7.17.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**0xbb80 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Output Compare No Output Channel 1:

Mode	**Toggle on match ***
Pulse (16 bits value)	0
Output compare preload	Disable
CH Polarity	High

7.18. TIM16

mode: Activated

Channel1: Input Capture direct mode

7.18.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**4799 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0xffff
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

7.19. TIM17

mode: Activated

Channel1: Input Capture direct mode

7.19.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**4799 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0xffff
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Input Capture Channel 1:

Polarity Selection	Rising Edge

IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

7.20. TIM19

Combined Channels: Encoder Mode

7.20.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

7.21. USART1

Mode: Asynchronous

7.21.1. Parameter Settings:

Basic Parameters:

Baud Rate	38400
Word Length	8 Bits (including Parity)
Parity	None

Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.22. USB

mode: Device (FS)

7.22.1. Parameter Settings:

Basic Parameters:

Speed	Full Speed 12MBit/s
Physical interface	Internal Phy

Power Parameters:

Low Power	Disabled
Battery Charging	Disabled

7.23. FATFS

mode: User-defined

7.23.1. Set Defines:

Version:

FATFS version	R0.11

Function Parameters:

FS_READONLY (Read-only mode)	Disabled
FS_MINIMIZE (Minimization level)	Disabled
USE_STRFUNC (String functions)	Enabled with LF -> CRLF conversion
USE_FIND (Find functions)	Disabled

USE_MKFS (Make filesystem function)	Enabled
USE_FASTSEEK (Fast seek function)	Enabled
USE_LABEL (Volume label functions)	Disabled
USE_FORWARD (Forward function)	Disabled

Locale and Namespace Parameters:

CODE_PAGE (Code page on target)	Multilingual Latin 1 (OEM)
USE_LFN (Use Long Filename)	Disabled
MAX_LFN (Max Long Filename)	255
LFN_UNICODE (Enable Unicode)	ANSI/OEM
STRF_ENCODE (Character encoding)	UTF-8
FS_RPATH (Relative Path)	Disabled

Physical Drive Parameters:

VOLUMES (Logical drives)	1
MAX_SS (Maximum Sector Size)	512
MIN_SS (Minimum Sector Size)	512
MULTI_PARTITION (Volume partitions feature)	Disabled
USE_TRIM (Erase feature)	Disabled
FS_NOFSINFO (Force full FAT scan)	0

System Parameters:

FS_TINY (Tiny mode)	Disabled
FS_NORTC (Timestamp feature)	Dynamic timestamp
WORD_ACCESS (Platform dependent access option)	Byte access
FS_REENTRANT (Re-Entrancy)	Disabled
FS_TIMEOUT (Timeout ticks)	1000
FS_LOCK (Number of files opened simultaneously)	2

7.24. USB_DEVICE

Class For FS IP: Communication Device Class (Virtual Port Com)

7.24.1. Parameter Settings:

Basic Parameters:

USBD_MAX_NUM_INTERFACES (Maximum number of supported interfaces)	1
USBD_MAX_NUM_CONFIGURATION (Maximum number of supported configuration)	1
USBD_MAX_STR_DESC_SIZ (Maximum size for the string descriptors)	512
USBD_SELF_POWERED (Enabled self power)	**Disabled ***
USBD_DEBUG_LEVEL (USBD Debug Level)	0: No debug message

Class Parameters:

USB CDC Rx Buffer Size	1000
USB CDC Tx Buffer Size	1000

7.24.2. Device Descriptor:

Device Descriptor:

VID (Vendor IDentifier)	1155
LANGID_STRING (Language Identifier)	English(United States)
MANUFACTURER_STRING (Manufacturer Identifier)	STMicroelectronics

Device Descriptor FS:

PID (Product IDentifier)	22336
PRODUCT_STRING (Product Identifier)	STM32 Virtual ComPort
CONFIGURATION_STRING (Configuration Identifier)	CDC Config
INTERFACE_STRING (Interface Identifier)	CDC Interface

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
CAN	PD0	CAN_RX	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PD1	CAN_TX	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
DAC1	PA4	DAC1_OUT1	Analog mode	No pull-up and no pull-down	n/a	AO0
	PA5	DAC1_OUT2	Analog mode	No pull-up and no pull-down	n/a	AO1
DAC2	PA6	DAC2_OUT1	Analog mode	No pull-up and no pull-down	n/a	AO2
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PF0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PF1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SDADC1	PB0	SDADC1_AIN6P	Analog mode	No pull-up and no pull-down	n/a	AI0
	PB1	SDADC1_AIN5P	Analog mode	No pull-up and no pull-down	n/a	AI1
	PB2	SDADC1_AIN4P	Analog mode	No pull-up and no pull-down	n/a	AI2
	PE7	SDADC1_AIN3P	Analog mode	No pull-up and no pull-down	n/a	AI3
	PE8	SDADC1_AIN8P	Analog mode	No pull-up and no pull-down	n/a	AI4
	PE9	SDADC1_AIN7P	Analog mode	No pull-up and no pull-down	n/a	AI5
	PE10	SDADC1_AIN2P	Analog mode	No pull-up and no pull-down	n/a	AI6
	PE11	SDADC1_AIN1P	Analog mode	No pull-up and no pull-down	n/a	AI7
	PE12	SDADC1_AIN0P	Analog mode	No pull-up and no pull-down	n/a	AI8
SDADC2	PE13	SDADC2_AIN2P	Analog mode	No pull-up and no pull-down	n/a	AI9
	PE14	SDADC2_AIN1P	Analog mode	No pull-up and no pull-down	n/a	AI10
	PE15	SDADC2_AIN0P	Analog mode	No pull-up and no pull-down	n/a	AI11
SDADC3	PB14	SDADC3_AIN8P	Analog mode	No pull-up and no pull-down	n/a	DAI0P
	PB15	SDADC3_AIN8M	Analog mode	No pull-up and no pull-down	n/a	DAI0M
	PD8	SDADC3_AIN6P	Analog mode	No pull-up and no pull-down	n/a	DAI1P
	PD9	SDADC3_AIN6M	Analog mode	No pull-up and no pull-down	n/a	DAI1M
	PD10	SDADC3_AIN4P	Analog mode	No pull-up and no pull-down	n/a	DAI2P
	PD11	SDADC3_AIN4M	Analog mode	No pull-up and no pull-down	n/a	DAI2M
	PD12	SDADC3_AIN2P	Analog mode	No pull-up and no pull-down	n/a	DAI3P
	PD13	SDADC3_AIN2M	Analog mode	No pull-up and no pull-down	n/a	DAI3M
	PD14	SDADC3_AIN0P	Analog mode	No pull-up and no pull-down	n/a	DAI4P
	PD15	SDADC3_AIN0M	Analog mode	No pull-up and no pull-down	n/a	DAI4M
SPI1	PC7	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC8	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PC9	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
SPI2	PA8	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PA9	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PA10	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
	PB3	SYS_JTDO-TRACESWO	n/a	n/a	n/a	
TIM2	PA0	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM4
	PA1	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM5
	PA2	TIM2_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM6
	PA3	TIM2_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM7
TIM4	PB6	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	E0-
	PB7	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	E0+
TIM5	PC0	TIM5_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM0
	PC1	TIM5_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM1
	PC2	TIM5_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM2
	PC3	TIM5_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM3
TIM16	PB8	TIM16_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	IC1
TIM17	PB9	TIM17_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	IC0
TIM19	PC10	TIM19_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	E1-
	PC11	TIM19_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	E1+
USART1	PE0	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PE1	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
USB	PA11	USB_DM	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PA12	USB_DP	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
GPIO	PE2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DI0
	PE3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DI1
	PE4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DI2
	PE5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DI3
	PE6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DI4
	PC13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DI5
	PF9	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DI6
	PF10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DI7
	PF2	GPIO_Output	Output Push Pull	**Pull-up ***	Low	CS4
	PF4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CS3

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PA7	GPIO_Output	Output Push Pull	**Pull-up ***	Low	CS0
	PC4	GPIO_Output	Output Push Pull	**Pull-up ***	Low	CS1
	PC5	GPIO_Output	Output Push Pull	**Pull-up ***	Low	CS2
	PB10	GPIO_Output	Output Push Pull	**Pull-up ***	Low	CS5
	PC6	GPIO_Output	Output Push Pull	**Pull-up ***	Low	TS_CS
	PF6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD_RST
	PA15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD_DC
	PC12	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	STOP_LOGGING_CONTROL
	PD2	GPIO_Output	Output Push Pull	**Pull-up ***	Low	LCD_CS
	PD3	GPIO_Input	Input mode	**Pull-up ***	n/a	TS_IRQ
	PD4	GPIO_Output	Output Push Pull	**Pull-up ***	Low	SD_CS
	PD5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED0
	PD6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED1
	PD7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED2
	PB4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED3
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED4

8.2. DMA configuration

DMA request	Stream	Direction	Priority
TIM17_CH1/UP	DMA1_Channel1	Peripheral To Memory	**Medium ***
TIM16_CH1/UP	DMA1_Channel3	Peripheral To Memory	Low
SDADC3	DMA2_Channel5	Peripheral To Memory	Low
SDADC2	DMA2_Channel4	Peripheral To Memory	Low
SDADC1	DMA2_Channel3	Peripheral To Memory	Low

TIM17_CH1/UP: DMA1_Channel1 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

TIM16_CH1/UP: DMA1_Channel3 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

SDADC3: DMA2_Channel5 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

SDADC2: DMA2_Channel4 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***

Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

SDADC1: DMA2_Channel3 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel1 global interrupt	true	0	0
DMA1 channel3 global interrupt	true	0	0
CAN RX0 interrupt	true	0	0
DMA2 channel3 global interrupt	true	0	0
DMA2 channel4 global interrupt	true	0	0
DMA2 channel5 global interrupt	true	0	0
USB low priority global interrupt	true	0	0
PVD interrupt through EXTI line16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
CAN TX interrupt	unused		
CAN RX1 interrupt	unused		
CAN SCE interrupt	unused		
TIM16 global interrupt	unused		
TIM17 global interrupt	unused		
TIM18 global interrupt and DAC2 underrun error interrupt	unused		
TIM2 global interrupt	unused		
TIM4 global interrupt	unused		
SPI1 global interrupt	unused		
SPI2 global interrupt	unused		
USART1 global interrupt / USART1 wake-up interrupt through EXTI line 25	unused		
RTC alarms A and B interrupt through EXTI line 17	unused		
TIM12 global interrupt	unused		
TIM13 global interrupt	unused		
TIM5 global interrupt	unused		
TIM6 global interrupt and DAC1 underrun error interrupts	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
SDADC1 global interrupt	unused		
SDADC2 global interrupt	unused		
SDADC3 global interrupt	unused		
USB high priority global interrupt	unused		
TIM19 global interrupt	unused		
Floating point unit interrupt	unused		

8.3.2. NVIC Code generation

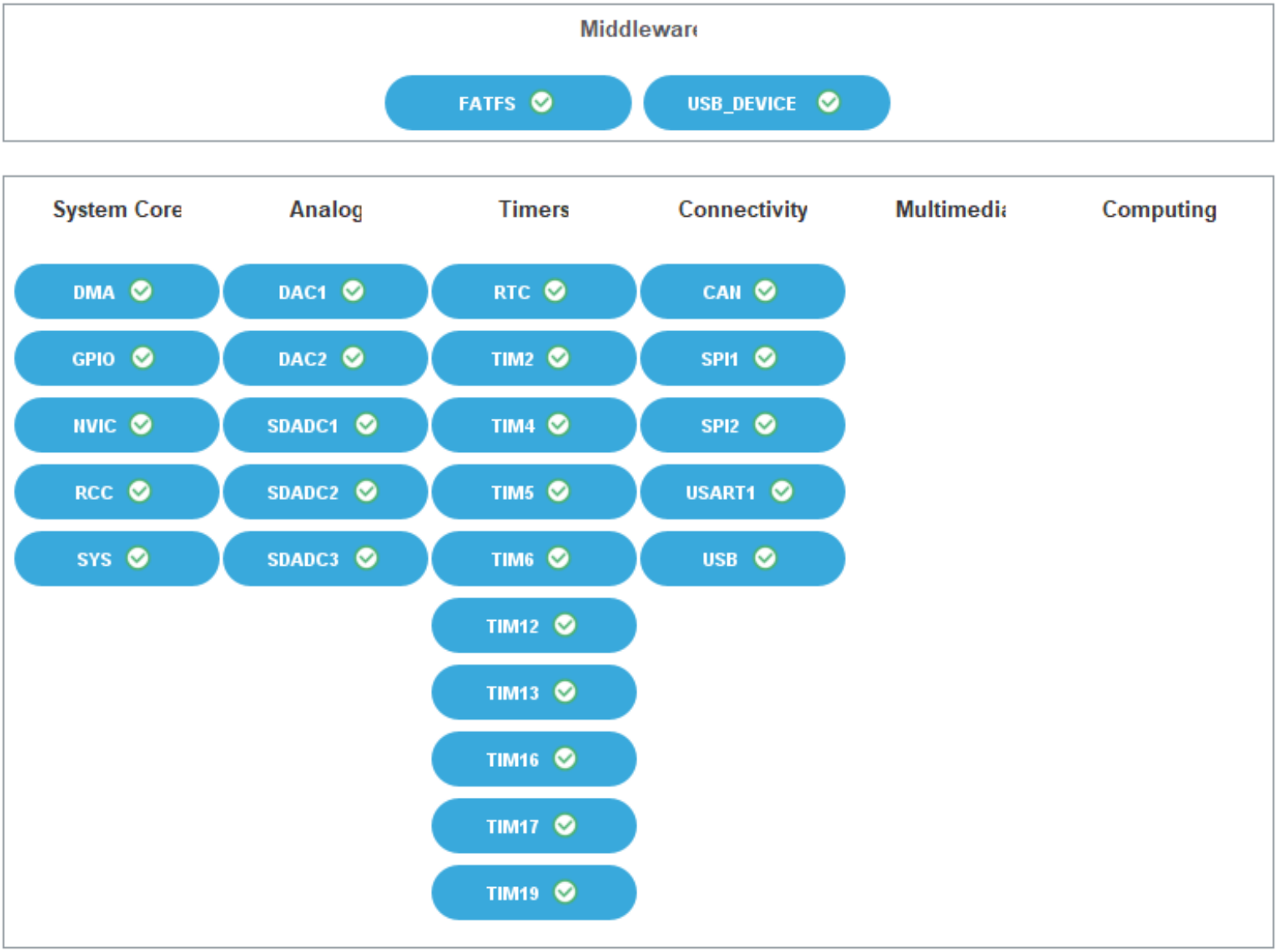
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 channel1 global interrupt	false	true	true
DMA1 channel3 global interrupt	false	true	true
CAN RX0 interrupt	false	true	true
DMA2 channel3 global interrupt	false	true	true
DMA2 channel4 global interrupt	false	true	true
DMA2 channel5 global interrupt	false	true	true
USB low priority global interrupt	false	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current



10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00046749.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00041563.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00047037.pdf
Application note	http://www.st.com/resource/en/application_note/CD00160362.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00249778.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00025071.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00047998.pdf
Application note	http://www.st.com/resource/en/application_note/DM00053084.pdf
Application note	http://www.st.com/resource/en/application_note/DM00070391.pdf
Application note	http://www.st.com/resource/en/application_note/DM00070480.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00074240.pdf
Application note	http://www.st.com/resource/en/application_note/DM00080497.pdf
Application note	http://www.st.com/resource/en/application_note/DM00085385.pdf
Application note	http://www.st.com/resource/en/application_note/DM00087593.pdf
Application note	http://www.st.com/resource/en/application_note/DM00121474.pdf
Application note	http://www.st.com/resource/en/application_note/DM00124123.pdf

Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00157785.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf
Application note	http://www.st.com/resource/en/application_note/DM00210617.pdf
Application note	http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note	http://www.st.com/resource/en/application_note/DM00236305.pdf
Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note	http://www.st.com/resource/en/application_note/DM00296349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00315319.pdf
Application note	http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354244.pdf
Application note	http://www.st.com/resource/en/application_note/DM00355687.pdf
Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note	http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note	http://www.st.com/resource/en/application_note/DM00445657.pdf
Application note	http://www.st.com/resource/en/application_note/DM00493651.pdf
Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00607955.pdf
Application note	http://www.st.com/resource/en/application_note/DM00725181.pdf