
STM32
CubeMX

1. Description

1.1. Project

Project Name	ETH OPAMP DCMI FSMC CAN ENCODER CS1000
Board Name	custom
Generated with:	STM32CubeMX 6.1.1
Date	02/07/2021

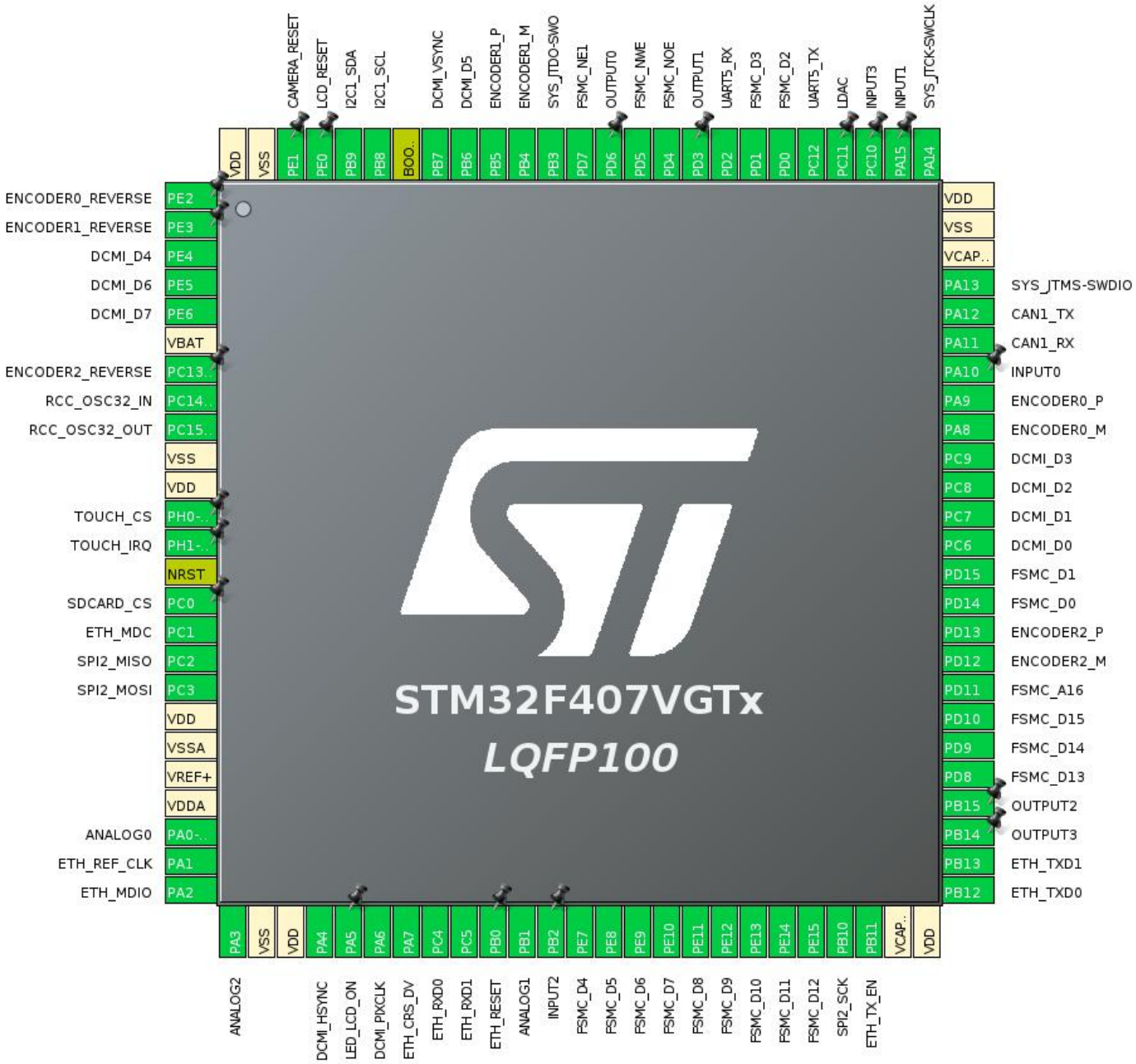
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F407/417
MCU name	STM32F407VGTx
MCU Package	LQFP100
MCU Pin number	100

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration



3. Pins Configuration

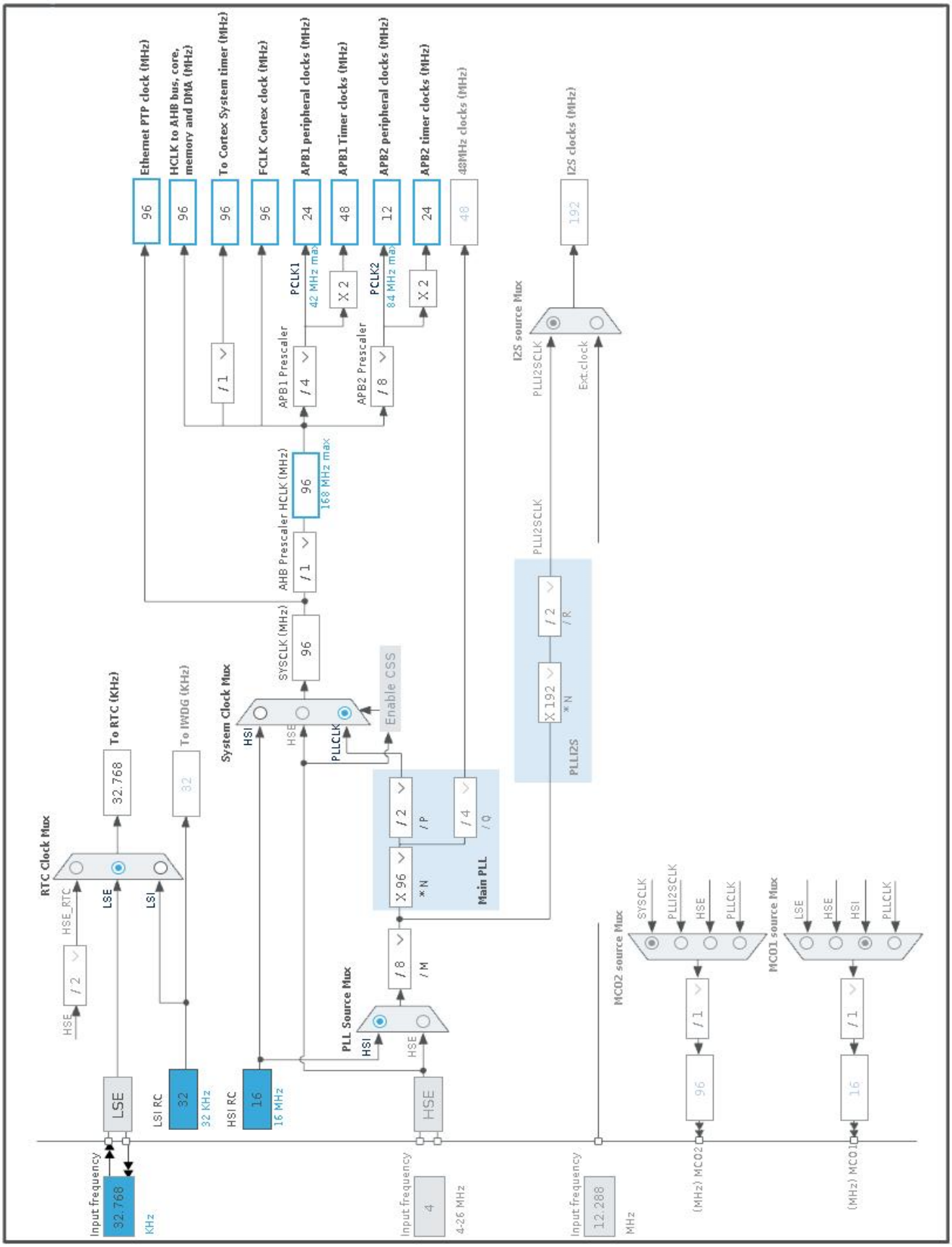
Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Output	ENCODER0_REVERSE
2	PE3 *	I/O	GPIO_Output	ENCODER1_REVERSE
3	PE4	I/O	DCMI_D4	
4	PE5	I/O	DCMI_D6	
5	PE6	I/O	DCMI_D7	
6	VBAT	Power		
7	PC13-ANTI_TAMP *	I/O	GPIO_Output	ENCODER2_REVERSE
8	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN *	I/O	GPIO_Output	TOUCH_CS
13	PH1-OSC_OUT *	I/O	GPIO_Input	TOUCH_IRQ
14	NRST	Reset		
15	PC0 *	I/O	GPIO_Output	SDCARD_CS
16	PC1	I/O	ETH_MDC	
17	PC2	I/O	SPI2_MISO	
18	PC3	I/O	SPI2_MOSI	
19	VDD	Power		
20	VSSA	Power		
21	VREF+	Power		
22	VDDA	Power		
23	PA0-WKUP	I/O	ADC1_IN0	ANALOG0
24	PA1	I/O	ETH_REF_CLK	
25	PA2	I/O	ETH_MDIO	
26	PA3	I/O	ADC1_IN3	ANALOG2
27	VSS	Power		
28	VDD	Power		
29	PA4	I/O	DCMI_HSYNC	
30	PA5 *	I/O	GPIO_Output	LED_LCD_ON
31	PA6	I/O	DCMI_PIXCLK	
32	PA7	I/O	ETH_CRS_DV	
33	PC4	I/O	ETH_RXD0	
34	PC5	I/O	ETH_RXD1	
35	PB0 *	I/O	GPIO_Output	ETH_RESET
36	PB1	I/O	ADC1_IN9	ANALOG1

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
37	PB2 *	I/O	GPIO_Input	INPUT2
38	PE7	I/O	FSMC_D4	
39	PE8	I/O	FSMC_D5	
40	PE9	I/O	FSMC_D6	
41	PE10	I/O	FSMC_D7	
42	PE11	I/O	FSMC_D8	
43	PE12	I/O	FSMC_D9	
44	PE13	I/O	FSMC_D10	
45	PE14	I/O	FSMC_D11	
46	PE15	I/O	FSMC_D12	
47	PB10	I/O	SPI2_SCK	
48	PB11	I/O	ETH_TX_EN	
49	VCAP_1	Power		
50	VDD	Power		
51	PB12	I/O	ETH_TXD0	
52	PB13	I/O	ETH_TXD1	
53	PB14 *	I/O	GPIO_Output	OUTPUT3
54	PB15 *	I/O	GPIO_Output	OUTPUT2
55	PD8	I/O	FSMC_D13	
56	PD9	I/O	FSMC_D14	
57	PD10	I/O	FSMC_D15	
58	PD11	I/O	FSMC_A16	
59	PD12	I/O	TIM4_CH1	ENCODER2_M
60	PD13	I/O	TIM4_CH2	ENCODER2_P
61	PD14	I/O	FSMC_D0	
62	PD15	I/O	FSMC_D1	
63	PC6	I/O	DCMI_D0	
64	PC7	I/O	DCMI_D1	
65	PC8	I/O	DCMI_D2	
66	PC9	I/O	DCMI_D3	
67	PA8	I/O	TIM1_CH1	ENCODER0_M
68	PA9	I/O	TIM1_CH2	ENCODER0_P
69	PA10 *	I/O	GPIO_Input	INPUT0
70	PA11	I/O	CAN1_RX	
71	PA12	I/O	CAN1_TX	
72	PA13	I/O	SYS_JTMS-SWDIO	
73	VCAP_2	Power		
74	VSS	Power		
75	VDD	Power		

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
76	PA14	I/O	SYS_JTCK-SWCLK	
77	PA15 *	I/O	GPIO_Input	INPUT1
78	PC10 *	I/O	GPIO_Input	INPUT3
79	PC11 *	I/O	GPIO_Output	LDAC
80	PC12	I/O	UART5_TX	
81	PD0	I/O	FSMC_D2	
82	PD1	I/O	FSMC_D3	
83	PD2	I/O	UART5_RX	
84	PD3 *	I/O	GPIO_Output	OUTPUT1
85	PD4	I/O	FSMC_NOE	
86	PD5	I/O	FSMC_NWE	
87	PD6 *	I/O	GPIO_Output	OUTPUT0
88	PD7	I/O	FSMC_NE1	
89	PB3	I/O	SYS_JTDO-SWO	
90	PB4	I/O	TIM3_CH1	ENCODER1_M
91	PB5	I/O	TIM3_CH2	ENCODER1_P
92	PB6	I/O	DCMI_D5	
93	PB7	I/O	DCMI_VSYNC	
94	BOOT0	Boot		
95	PB8	I/O	I2C1_SCL	
96	PB9	I/O	I2C1_SDA	
97	PE0 *	I/O	GPIO_Output	LCD_RESET
98	PE1 *	I/O	GPIO_Output	CAMERA_RESET
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	ETH OPAMP DCMI FSMC CAN ENCODER CS1000
Project Folder	/home/dell/Dokument/STM32-Workspace/ETH OPAMP DCMI FSMC CAN
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.25.2
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_FSMC_Init	FSMC
4	MX_DCMI_Init	DCMI
5	MX_I2C1_Init	I2C1
6	MX_SPI2_Init	SPI2
7	MX_TIM1_Init	TIM1
8	MX_TIM3_Init	TIM3
9	MX_ADC1_Init	ADC1
10	MX_CAN1_Init	CAN1
11	MX_RTC_Init	RTC

Rank	Function Name	Peripheral Instance Name
12	MX_LWIP_Init	LWIP
13	MX_TIM4_Init	TIM4
14	MX_FATFS_Init	FATFS
15	MX_UART5_Init	UART5

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F407/417
MCU	STM32F407VGTx
Datasheet	DS8626_Rev8

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

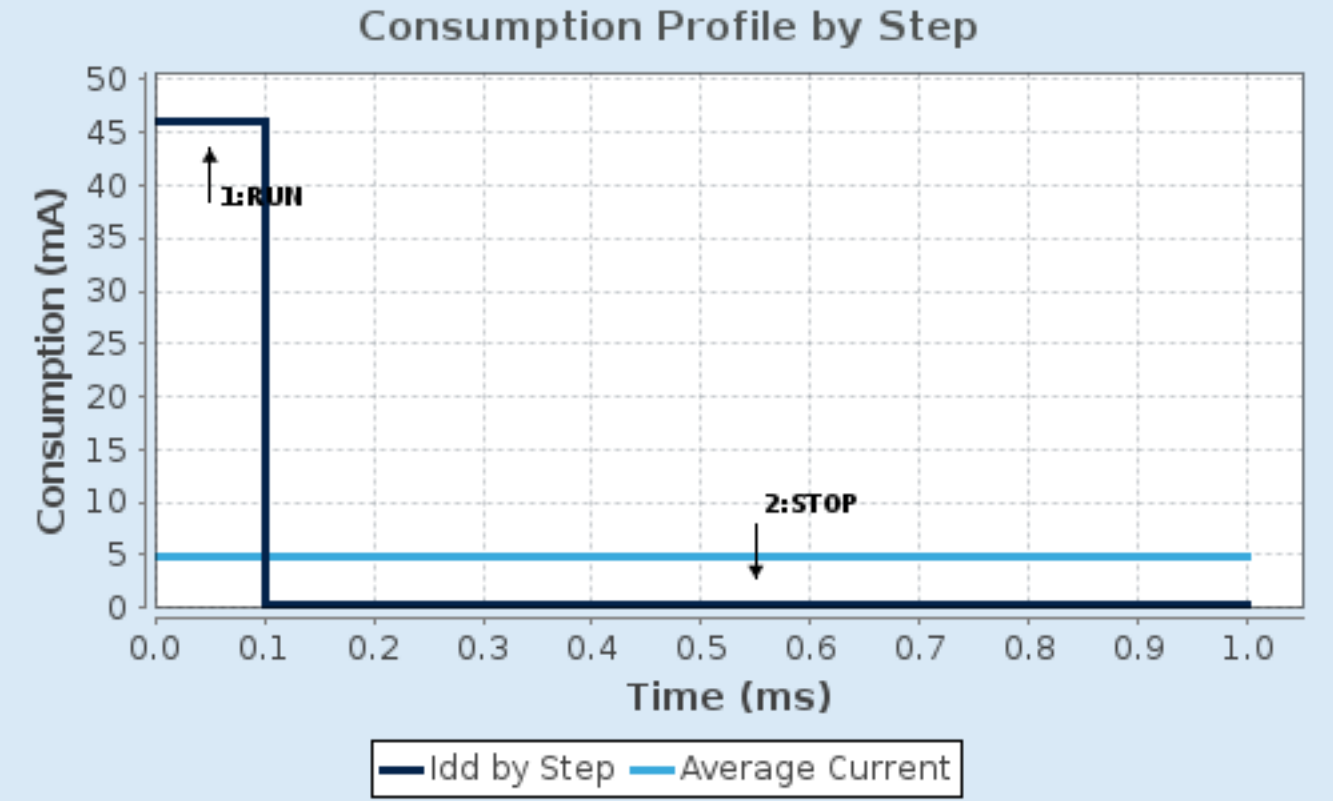
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	168 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	46 mA	280 µA
Duration	0.1 ms	0.9 ms
DMIPS	210.0	0.0
Ta Max	98.47	104.96
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	4.85 mA
Battery Life	29 days, 4 hours	Average DMIPS	210.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
50
45
40
35
30
25
20
15
10
5
0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. ADC1

mode: IN0

mode: IN3

mode: IN9

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 2
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 0
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.2. CAN1

mode: Activated

7.2.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum)	16
Time Quantum	**666.6666666666666 ***

Time Quanta in Bit Segment 1	1 Time
Time Quanta in Bit Segment 2	1 Time
Time for one Bit	**1999.99 ***
Baud Rate	**500000 ***
ReSynchronization Jump Width	1 Time

Basic Parameters:

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	Disable
Automatic Wake-Up Mode	Disable
Automatic Retransmission	Disable
Receive Fifo Locked Mode	Disable
Transmit Fifo Priority	Disable

Advanced Parameters:

Operating Mode	Normal

7.3. DCMI

DCMI: Slave 8 bits External Synchro

7.3.1. Parameter Settings:

Mode Config:

Pixel clock polarity	Active on Falling edge
Vertical synchronization polarity	Active Low
Horizontal synchronization polarity	Active Low
Frequency of frame capture	All frames are captured
JPEG mode	Disabled

7.4. ETH

Mode: RMII

7.4.1. Parameter Settings:

Advanced : Ethernet Media Configuration:

Auto Negotiation	Enabled
Speed	100 MBits/s
Duplex Mode	Full Duplex

General : Ethernet Configuration:

Ethernet MAC Address	00:80:E1:00:00:00
PHY Address	**5 ***

Ethernet Basic Configuration:

Rx Mode	Interrupt Mode
TX IP Header Checksum Computation	By hardware

7.4.2. Advanced Parameters:

External PHY Configuration:

PHY	**DP83848_PHY_ADDRESS ***
PHY Address Value	5
PHY Reset delay these values are based on a 1 ms Systick interrupt	**0x000000FF ***
PHY Configuration delay	**0x00000FFF ***
PHY Read TimeOut	**0x0000FFFF ***
PHY Write TimeOut	**0x0000FFFF ***

Common : External PHY Configuration:

Transceiver Basic Control Register	**0x00 ***
Transceiver Basic Status Register	**0x01 ***
PHY Reset	**0x8000 ***
Select loop-back mode	**0x4000 ***
Set the full-duplex mode at 100 Mb/s	**0x2100 ***
Set the half-duplex mode at 100 Mb/s	**0x2000 ***
Set the full-duplex mode at 10 Mb/s	**0x0100 ***
Set the half-duplex mode at 10 Mb/s	**0x0000 ***
Enable auto-negotiation function	**0x1000 ***
Restart auto-negotiation function	**0x0200 ***
Select the power down mode	**0x0800 ***
Isolate PHY from MII	**0x0400 ***
Auto-Negotiation process completed	**0x0020 ***
Valid link established	**0x0004 ***
Jabber condition detected	**0x0002 ***

Extended : External PHY Configuration:

PHY special control/status register Offset	**0x1F ***
PHY Speed mask	**0x0004 ***
PHY Duplex mask	**0x0010 ***
PHY Interrupt Source Flag register Offset	**0x001D ***
PHY Link down inturrupt	**0x000B ***

7.5. FSMC

NOR Flash/PSRAM/SRAM/ROM/LCD 1

Chip Select: set

Memory type: LCD Interface

LCD Register Select: A16

Data: 16 bits

7.5.1. NOR/PSRAM 1:

NOR/PSRAM control:

Memory type	LCD Interface
Bank	Bank 1 NOR/PSRAM 1
Write operation	Enabled
Extended mode	Disabled

NOR/PSRAM timing:

Address setup time in HCLK clock cycles	15
Data setup time in HCLK clock cycles	255
Bus turn around time in HCLK clock cycles	15

7.6. I2C1

I2C: I2C

7.6.1. Parameter Settings:

Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

7.7. RCC

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.7.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	3 WS (4 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

7.8. RTC

mode: Activate Clock Source

7.8.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255

7.9. SPI2

Mode: Full-Duplex Master

7.9.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**12.0 MBits/s ***
Clock Polarity (CPOL)	Low

Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

7.10. SYS

Debug: Trace Asynchronous Sw

Timebase Source: TIM2

7.11. TIM1

Combined Channels: Encoder Mode

7.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	Encoder Mode TI1
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

7.12. TIM3

Combined Channels: Encoder Mode

7.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	Encoder Mode TI1
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

7.13. TIM4

Combined Channels: Encoder Mode

7.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	Encoder Mode TI1
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

7.14. UART5

Mode: Asynchronous

7.14.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.15. FATFS

mode: User-defined

7.15.1. Set Defines:

Version:

FATFS version	R0.12c

Function Parameters:

FS_READONLY (Read-only mode)	Disabled
FS_MINIMIZE (Minimization level)	Disabled
USE_STRFUNC (String functions)	Enabled with LF -> CRLF conversion
USE_FIND (Find functions)	Disabled
USE_MKFS (Make filesystem function)	Enabled

USE_FASTSEEK (Fast seek function)	Enabled
USE_EXPAND (Use f_expand function)	Disabled
USE_CHMOD (Change attributes function)	Disabled
USE_LABEL (Volume label functions)	Disabled
USE_FORWARD (Forward function)	Disabled

Locale and Namespace Parameters:

CODE_PAGE (Code page on target)	Latin 1
USE_LFN (Use Long Filename)	Disabled
MAX_LFN (Max Long Filename)	255
LFN_UNICODE (Enable Unicode)	ANSI/OEM
STRF_ENCODE (Character encoding)	UTF-8
FS_RPATH (Relative Path)	Disabled

Physical Drive Parameters:

VOLUMES (Logical drives)	1
MAX_SS (Maximum Sector Size)	512
MIN_SS (Minimum Sector Size)	512
MULTI_PARTITION (Volume partitions feature)	Disabled
USE_TRIM (Erase feature)	Disabled
FS_NOFSINFO (Force full FAT scan)	0

System Parameters:

FS_TINY (Tiny mode)	Disabled
FS_EXFAT (Support of exFAT file system)	Disabled
FS_NORTC (Timestamp feature)	Dynamic timestamp
FS_REENTRANT (Re-Entrancy)	Enabled
FS_TIMEOUT (Timeout ticks)	1000
USE_MUTEX	Disabled
SYNC_t (O/S sync object)	osSemaphoreId_t
FS_LOCK (Number of files opened simultaneously)	2

7.16. FREERTOS

Interface: CMSIS_V2

7.16.1. Config parameters:

API:

FreeRTOS API	CMSIS v2

Versions:

FreeRTOS version	10.2.1
CMSIS-RTOS version	2.00

MPU/FPU:

ENABLE_MPU	Disabled

ENABLE_FPU	Disabled

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	56
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Enabled
USE_COUNTING_SEMAPHORES	Enabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Disabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled

Memory management settings:

Memory Allocation	Dynamic / Static
TOTAL_HEAP_SIZE	15360
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Enabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Enabled
TIMER_TASK_PRIORITY	2
TIMER_QUEUE_LENGTH	10
TIMER_TASK_STACK_DEPTH	256

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

Added with 10.2.1 support:

MESSAGE_BUFFER_LENGTH_TYPE	size_t
USE_POSIX_ERRNO	Disabled

7.16.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Enabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Enabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Enabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Enabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Enabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled
uxTaskGetStackHighWaterMark2	Disabled

7.16.3. Advanced settings:

Newlib settings (see parameter description first):

USE_NEWLIB_REENTRANT	Disabled

Project settings (see parameter description first):

Use FW pack heap file	Enabled

7.17. LWIP

mode: Enabled

Advanced parameters are not listed except if modified by user.

7.17.1. General Settings:

LwIP Version:	
LwIP Version (Version of LwIP supported by CubeMX ** CubeMX specific **)	2.1.2
IPv4 - DHCP Options:	
LWIP_DHCP (DHCP Module)	Enabled
RTOS Dependency:	
WITH_RTOS (Use FREERTOS ** CubeMX specific **)	Enabled
CMSIS_VERSION (CMSIS API Version used)	CMSIS v2
Protocols Options:	
LWIP_ICMP (ICMP Module Activation)	Enabled
LWIP_IGMP (IGMP Module)	Disabled
LWIP_DNS (DNS Module)	Disabled
LWIP_UDP (UDP Module)	Enabled
MEMP_NUM_UDP_PCB (Number of UDP Connections)	4
LWIP_TCP (TCP Module)	Enabled
MEMP_NUM_TCP_PCB (Number of TCP Connections)	5

7.17.2. Key Options:

Infrastructure - OS Awarness Option:	
NO_SYS (OS Awarness)	OS Used
Infrastructure - Timers Options:	
LWIP_TIMERS (Use Support For sys_timeout)	Enabled
Infrastructure - Core Locking and MPU Options:	
SYS_LIGHTWEIGHT_PROT (Memory Functions Protection)	Enabled
Infrastructure - Heap and Memory Pools Options:	
MEM_SIZE (Heap Memory Size)	1600
Infrastructure - Internal Memory Pool Sizes:	
MEMP_NUM_PBUF (Number of Memory Pool struct Pbufs)	16
MEMP_NUM_RAW_PCB (Number of Raw Protocol Control Blocks)	4
MEMP_NUM_TCP_PCB_LISTEN (Number of Listening TCP Connections)	8
MEMP_NUM_TCP_SEG (Number of TCP Segments simultaneously queued)	16
MEMP_NUM_LOCALHOSTLIST (Number of Host Entries in the Local Host List)	1
Pbuf Options:	
PBUF_POOL_SIZE (Number of Buffers in the Pbuf Pool)	16

PBUF_POOL_BUFSIZE (Size of each pbuf in the pbuf pool)	592

IPv4 - ARP Options:

LWIP_ARP (ARP Functionality)	Enabled

Callback - TCP Options:

TCP_TTL (Number of Time-To-Live Used by TCP Packets)	255
TCP_WND (TCP Receive Window Maximum Size)	2144
TCP_QUEUE_OOSEQ (Allow Out-Of-Order Incoming Packets)	Enabled
LWIP_TCP_SACK_OUT (Allow Sending Selective Acknowledgements)	Disabled
TCP_MSS (Maximum Segment Size)	536
TCP_SND_BUF (TCP Sender Buffer Space)	1072
TCP_SND_QUEUELEN (Number of Packet Buffers Allowed for TCP Sender)	9

Network Interfaces Options:

LWIP_NETIF_STATUS_CALLBACK (Callback Function on Interface Status Changes)	Disabled
LWIP_NETIF_EXT_STATUS_CALLBACK (Extended Callback Function for several netif)	Disabled
LWIP_NETIF_LINK_CALLBACK (Callback Function on Interface Link Changes)	Enabled

NETIF - Loopback Interface Options:

LWIP_NETIF_LOOPBACK (NETIF Loopback)	Disabled

Infrastructure - Threading Options:

TCPIP_THREAD_NAME (TCPIP Thread Name)	"tcpip_thread"
TCPIP_THREAD_STACKSIZE (TCPIP Thread Stack Size)	1024
TCPIP_THREAD_PRIO (TCPIP Thread Priority Level)	24
TCPIP_MBOX_SIZE (TCPIP Mailbox Size)	6
DEFAULT_THREAD_NAME (Default LwIP Thread Name)	"lwIP"
DEFAULT_THREAD_STACKSIZE (Default LwIP Thread Stack Size)	1024
DEFAULT_THREAD_PRIO (Default LwIP Thread Priority Level)	3
DEFAULT_RAW_RECVMBOX_SIZE (Default Mailbox Size on a NETCONN Raw)	0
DEFAULT_TCP_RECVMBOX_SIZE (Default Mailbox Size on a NETCONN TCP)	6
DEFAULT_ACCEPTMBOX_SIZE (Default Mailbox Size for Incoming Connections)	6

Thread Safe APIs - Netconn Options:

LWIP_NETCONN (NETCONN API)	Enabled

Thread Safe APIs - Socket Options:

LWIP_SOCKET (Socket API)	Enabled
LWIP_COMPAT_SOCKETS (BSD-style Socket Functions Names)	1
LWIP_SOCKET_OFFSET (Socket Offset Number)	0
LWIP_SOCKET_SELECT (Select for Socket)	Enabled
LWIP_SOCKET_POLL (Poll for Socket)	Enabled

7.17.3. PPP:

PPP Options:

PPP_SUPPORT (PPP Module)	Disabled

7.17.4. IPv6:

IPv6 Options:

LWIP_IPV6 (IPv6 Protocol)	Disabled

7.17.5. HTTPD:

HTTPD Options:

LWIP_HTTPD (LwIP HTTPD Support ** CubeMX specific **)	Disabled

7.17.6. SNMP:

SNMP Options:

LWIP_SNMP (LwIP SNMP Agent)	Disabled

7.17.7. SNTP/SMTP:

SNTP Options:

LWIP_SNTP (LWIP SNTP Support ** CubeMX specific **)	Disabled

SMTP Options:

LWIP_SMTP (LWIP SMTP Support ** CubeMX specific **)	Disabled

7.17.8. MDNS/TFTP:

MDNS Options:

LWIP_MDNS (Multicast DNS Support ** CubeMX specific **)	Disabled

TFTP Options:

LWIP_TFTP (TFTP Support ** CubeMX specific **)	Disabled

7.17.9. Perf/Checks:

Sanity Checks:

LWIP_DISABLE_TCP_SANITY_CHECKS (TCP Sanity Checks)	Disabled
LWIP_DISABLE_MEMP_SANITY_CHECKS (MEMP Sanity Checks)	Disabled

Performance Options:

LWIP_PERF (Performace Testing for LwIP)	Disabled

7.17.10. Statistics:

Debug - Statistics Options:

LWIP_STATS (Statictics Collection)	Disabled

7.17.11. Checksum:

Infrastructure - Checksum Options:

CHECKSUM_BY_HARDWARE (Hardware Checksum ** CubeMX specific **)	Enabled
LWIP_CHECKSUM_CTRL_PER_NETIF (Generate/Check Checksum per Netif)	Disabled
CHECKSUM_GEN_IP (Generate Software Checksum for Outgoing IP Packets)	Disabled
CHECKSUM_GEN_UDP (Generate Software Checksum for Outgoing UDP Packets)	Disabled
CHECKSUM_GEN_TCP (Generate Software Checksum for Outgoing TCP Packets)	Disabled
CHECKSUM_GEN_ICMP (Generate Software Checksum for Outgoing ICMP Packets)	Disabled
CHECKSUM_GEN_ICMP6 (Generate Software Checksum for Outgoing ICMP6 Packets)	Disabled
CHECKSUM_CHECK_IP (Generate Software Checksum for Incoming IP Packets)	Disabled
CHECKSUM_CHECK_UDP (Generate Software Checksum for Incoming UDP Packets)	Disabled
CHECKSUM_CHECK_TCP (Generate Software Checksum for Incoming TCP Packets)	Disabled
CHECKSUM_CHECK_ICMP (Generate Software Checksum for Incoming ICMP Packets)	Disabled
CHECKSUM_CHECK_ICMP6 (Generate Software Checksum for Incoming ICMP6 Packets)	Disabled

7.17.12. Debug:

LwIP Main Debugging Options:

LWIP_DBG_MIN_LEVEL (Minimum Level)	All

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0-WKUP	ADC1_IN0	Analog mode	No pull-up and no pull-down	n/a	ANALOG0
	PA3	ADC1_IN3	Analog mode	No pull-up and no pull-down	n/a	ANALOG2
	PB1	ADC1_IN9	Analog mode	No pull-up and no pull-down	n/a	ANALOG1
CAN1	PA11	CAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA12	CAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
DCMI	PE4	DCMI_D4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE5	DCMI_D6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE6	DCMI_D7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA4	DCMI_HSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA6	DCMI_PIXCLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC6	DCMI_D0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC7	DCMI_D1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC8	DCMI_D2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC9	DCMI_D3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB6	DCMI_D5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB7	DCMI_VSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
ETH	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB12	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PB13	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
FSMC	PE7	FSMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE8	FSMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE9	FSMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE10	FSMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE11	FSMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE12	FSMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE13	FSMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE14	FSMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE15	FSMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD8	FSMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD9	FSMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD10	FSMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD11	FSMC_A16	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD14	FSMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD15	FSMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD0	FSMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD1	FSMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD4	FSMC_NOE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD5	FSMC_NWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD7	FSMC_NE1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
I2C1	PB8	I2C1_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	
	PB9	I2C1_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
SPI2	PC2	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC3	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB10	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-	n/a	n/a	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
		SWCLK				
	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	ENCODER0_M
	PA9	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	ENCODER0_P
TIM3	PB4	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	ENCODER1_M
	PB5	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	ENCODER1_P
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	ENCODER2_M
	PD13	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	ENCODER2_P
UART5	PC12	UART5_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
	PD2	UART5_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
GPIO	PE2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ENCODER0_REVERSE
	PE3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ENCODER1_REVERSE
	PC13-ANTI_TAMP	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ENCODER2_REVERSE
	PH0-OSC_IN	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TOUCH_CS
	PH1-OSC_OUT	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	TOUCH_IRQ
	PC0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SDCARD_CS
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_LCD_ON
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ETH_RESET
	PB2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	INPUT2
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OUTPUT3
	PB15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OUTPUT2
	PA10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	INPUT0
	PA15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	INPUT1
	PC10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	INPUT3
	PC11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LDAC
	PD3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OUTPUT1
	PD6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OUTPUT0
	PE0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD_RESET
	PE1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CAMERA_RESET

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
TIM2 global interrupt	true	0	0
Ethernet global interrupt	true	5	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
CAN1 TX interrupts	unused		
CAN1 RX0 interrupts	unused		
CAN1 RX1 interrupt	unused		
CAN1 SCE interrupt	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
SPI2 global interrupt	unused		
UART5 global interrupt	unused		
Ethernet wake-up interrupt through EXTI line 19	unused		
DCMI global interrupt	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init	Generate IRQ	Call HAL handler

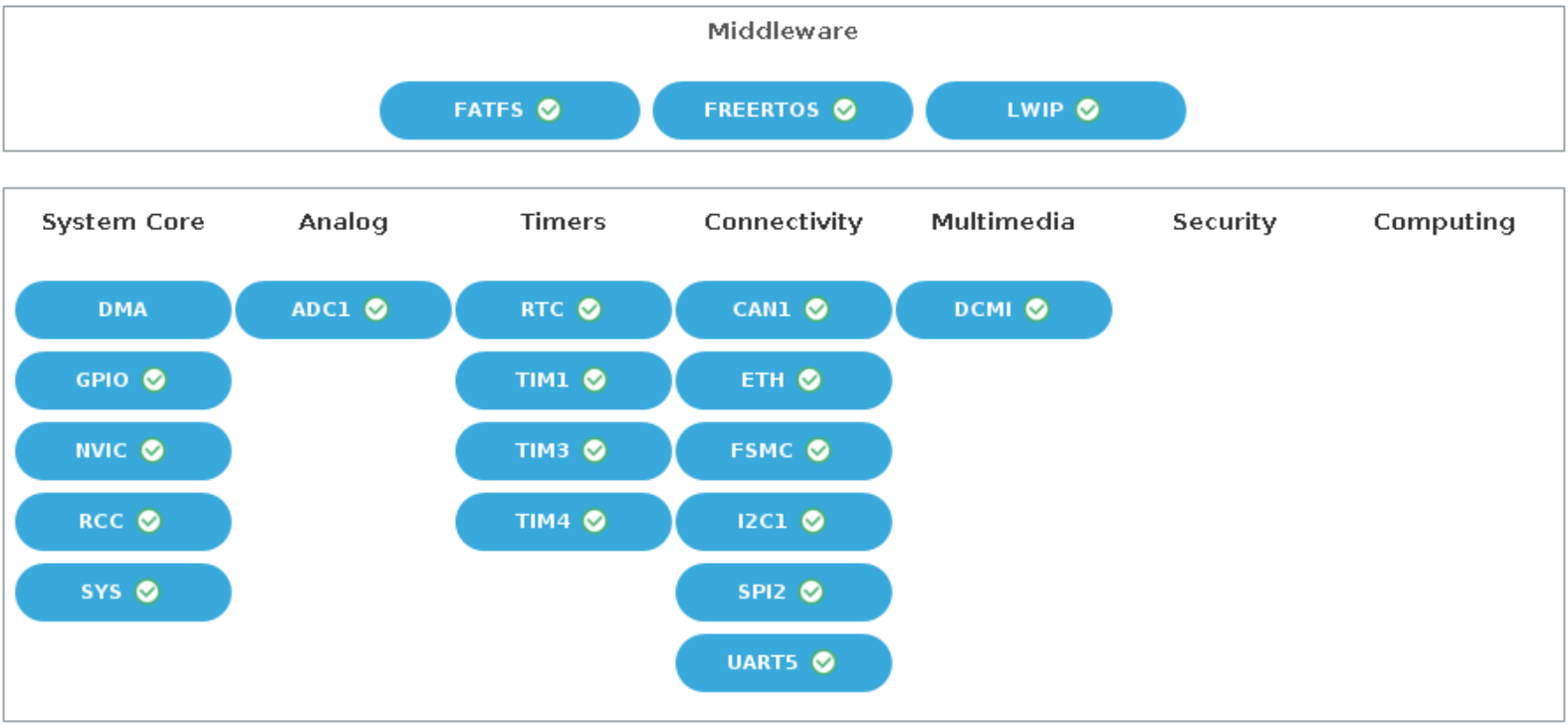
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	false	true
TIM2 global interrupt	false	true	true
Ethernet global interrupt	false	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current



10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00037051.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00031020.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00037591.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00249778.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264321.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00024853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00025071.pdf
Application note	http://www.st.com/resource/en/application_note/DM00040802.pdf
Application note	http://www.st.com/resource/en/application_note/DM00040808.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00046011.pdf
Application note	http://www.st.com/resource/en/application_note/DM00050879.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00080497.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00115714.pdf
Application note	http://www.st.com/resource/en/application_note/DM00123028.pdf

Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00154959.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf
Application note	http://www.st.com/resource/en/application_note/DM00213525.pdf
Application note	http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note	http://www.st.com/resource/en/application_note/DM00236305.pdf
Application note	http://www.st.com/resource/en/application_note/DM00263732.pdf
Application note	http://www.st.com/resource/en/application_note/DM00281138.pdf
Application note	http://www.st.com/resource/en/application_note/DM00296349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354244.pdf
Application note	http://www.st.com/resource/en/application_note/DM00373474.pdf
Application note	http://www.st.com/resource/en/application_note/DM00315319.pdf
Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note	http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note	http://www.st.com/resource/en/application_note/DM00431633.pdf
Application note	http://www.st.com/resource/en/application_note/DM00493651.pdf
Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00725181.pdf