# AN5031
# Application note

## Getting started with STM32MP151, STM32MP153 and STM32MP157 line hardware development

## Introduction

This application note describes how to use the STM32MP151, STM32MP153 and STM32MP157 lines, and details the minimum hardware resources required to develop an application based on those MPUs devices.

This application note is intended for system designers who require an overview of the hardware implementation of the development board, with a focus on features such as:

- Power supply
- Package selection
- Clock management
- Reset control
- Boot mode settings
- Debug management.

Reference design schematics are also contained in this document with descriptions of the main components, interfaces and modes.

# Contents


**1 General information . . . . . 8**

**2 Reference documents . . . . . 8**

**3 Glossary . . . . . 9**

**4 Power supplies . . . . . 11**

4.1 Introduction . . . . . 12

4.1.1 Independent ADC and DAC converter supply and reference voltage . . 12

4.1.2 Battery backup . . . . . 13

4.1.3 Voltage regulators . . . . . 13

4.2 Power supply schemes . . . . . 14

4.3 Reset and power supply supervisor . . . . . 18

4.3.1 Power on reset (POR) / power down reset (PDR) . . . . . 18

4.3.2 Programmable voltage detector (PVD) . . . . . 18

4.3.3 Application and system resets . . . . . 19

**5 Packages . . . . . 21**

5.1 Package selection . . . . . 21

5.2 Alternate function mapping to pins . . . . . 23

5.3 Package compatibility between versions . . . . . 24

**6 Clocks . . . . . 29**

6.1 HSE OSC clock . . . . . 29

6.1.1 External source (HSE bypass) . . . . . 30

6.1.2 External crystal/ceramic resonator (HSE crystal) . . . . . 30

6.2 LSE OSC clock . . . . . 31

6.2.1 External source (LSE bypass) . . . . . 31

6.2.2 External crystal/ceramic resonator (LSE crystal) . . . . . 31

6.3 Clock security system (CSS) . . . . . 32

6.3.1 CSS on HSE . . . . . 32

6.3.2 CSS on LSE . . . . . 32

**7 Boot configuration . . . . . 33**

7.1 Boot mode selection . . . 33
7.2 Boot pin connection . . . 34
7.3 Embedded boot loader mode . . . 36

**8 Debug management . . . 37**
8.1 Introduction . . . 37
8.2 SWJ debug port (serial wire and JTAG) . . . 37
8.3 Pinout and debug port pins . . . 37
8.3.1 Internal pull-up and pull-down resistors on JTAG pins . . . 37
8.3.2 Debug port connection with standard JTAG connector . . . 38
8.3.3 Debug port and UART connection with STDC14 connector . . . 39
8.3.4 Parallel trace and HDP . . . 40
8.3.5 Debug triggers and LEDs . . . 42

**9 Recommendations . . . 43**
9.1 Printed circuit board . . . 43
9.2 Component position . . . 43
9.3 Ground and power supply ($V_{SSx}$, $V_{DDx}$) . . . 43
9.4 I/O speed settings . . . 43
9.5 PCB stack and technology . . . 47
9.6 Decoupling . . . 51
9.7 ESD/EMI protections . . . 51
9.8 Sensitive signals . . . 52
9.9 Unused I/Os and features . . . 52

**10 Reference design examples . . . 53**
10.1 Description . . . 53
10.1.1 Clock . . . 53
10.1.2 Reset . . . 54
10.1.3 Boot mode . . . 54
10.1.4 SWD / JTAG interface . . . 54
10.1.5 Power supply . . . 55
10.1.6 DDR3/DDR3L SDRAM . . . 58
10.1.7 LpDDR2/LpDDR3 SDRAM . . . 59
10.1.8 SD card . . . 60
10.1.9 eMMC™ Flash . . . 62

10.1.10 SLC NAND-Flash . . . . . 64
10.1.11 Serial NOR-Flash/NAND-Flash . . . . . 65
10.1.12 USB . . . . . 67
10.1.13 Ethernet . . . . . 70
10.1.14 Display serial interface (DSI) . . . . . 76

**11 Revision history . . . . . 79**

# List of tables

Table 1. Reference documents . . . 8
Table 2. Glossary . . . 9
Table 3. Recommended settings for ANASWVDD and EN_BOOSTER . . . 13
Table 4. Amount of decoupling recommendation by package . . . 16
Table 5. Supply usage for unused features . . . 17
Table 6. Package summary . . . 21
Table 7. Major feature changes related to packages . . . 22
Table 8. Device compatibility summary . . . 24
Table 9. STM32MP151xxx and STM32MP153xxx for 16x16 LFBGA354 compatibility . . . 25
Table 10. STM32MP151xxx and STM32MP153xxx for 10x10 TFBGA257 compatibility . . . 26
Table 11. STM32MP151xxx and STM32MP153xxx for 12x12 TFBGA361 compatibility . . . 27
Table 12. STM32MP151xxx and STM32MP153xxx for 18x18 LFBGA448 compatibility . . . 28
Table 13. Boot modes . . . 33
Table 14. OSPEEDR setting example for VDD = 3.3 V typical . . . 44
Table 15. OSPEEDR setting example for VDD = 1.8 V typical . . . 45
Table 16. HSE BOM for oscillator or crystal . . . 53
Table 17. UART possible boot pins . . . 54
Table 18. USB package length matching values . . . 69
Table 19. USB high-speed PCB routing recommendations . . . 70
Table 20. DSI package length matching values . . . 77
Table 21. DSI PCB routing recommendations . . . 78
Table 22. Document revision history . . . 79

# List of figures

Figure 1. Power supply scheme . . . 11
Figure 2. Power-on reset/power-down reset waveform . . . 18
Figure 3. PVD thresholds . . . 19
Figure 4. Simplified reset pin circuit . . . 20
Figure 5. STM32CubeMX example screen-shot . . . 23
Figure 6. 16x16 LFBGA354 compatibility . . . 25
Figure 7. 10x10 TFBGA257 compatibility . . . 26
Figure 8. 12x12 TFBGA361 compatibility . . . 27
Figure 9. 18x18 LFBGA448 compatibility . . . 28
Figure 10. HSE external clock . . . 29
Figure 11. HSE crystal/ceramic resonators . . . 29
Figure 12. LSE external clock . . . 31
Figure 13. LSE crystal/ceramic resonators . . . 31
Figure 14. Boot mode selection example . . . 34
Figure 15. BOOT pins typical connection schematics . . . 35
Figure 16. Simplified boot flow . . . 36
Figure 17. Host-to-board connection . . . 37
Figure 18. JTAG/SWD MIPI10 connector implementation example . . . 38
Figure 19. JTAG/SWD/UART VCP STDC14 connector implementation example . . . 39
Figure 20. Parallel trace port with JTAG/SWD on Mictor-38 implementation example . . . 41
Figure 21. Example of LED connections . . . 42
Figure 22. I/O speed summary with various loads and voltages . . . 44
Figure 23. 6 layer PCB stack example . . . 47
Figure 24. 4 layer PCB stack example . . . 48
Figure 25. PCB rule example for 0.8 mm pitch package . . . 49
Figure 26. PCB rule example for 0.5 mm pitch package . . . 50
Figure 27. PCB rule example for inner balls with 0.65mm power improved pitch . . . 50
Figure 28. Example of decoupling layout . . . 51
Figure 29. HSE recommended schematics for both oscillator/crystal options . . . 53
Figure 30. Discrete supplies example 3.3 V I/Os with DDR3L . . . 55
Figure 31. PMIC example 3.3 V I/Os with DDR3L . . . 56
Figure 32. PMIC example 1.8 V I/Os with LPDDR2/LPDDR3 . . . 57
Figure 33. DDR3L 16/32 bits connection example . . . 58
Figure 34. LPDDR2/LPDDR3 32-bits connection example . . . 59
Figure 35. SD-Card with external level shifter connection example . . . 61
Figure 36. SD-Card with 3.3 V I/Os connection example . . . 62
Figure 37. eMMC™ connection example . . . 63
Figure 38. SLC NAND-Flash connection example . . . 64
Figure 39. Serial Flash connection example . . . 65
Figure 40. Dual-Serial Flash connection example . . . 66
Figure 41. USB 2 ports host high-speed + OTG full-speed connection example . . . 67
Figure 42. USB host high-speed + OTG high-speed connection example . . . 68
Figure 43. USB high-speed PCB track example for 0.8 mm ball pitch package . . . 69
Figure 44. 10/100M Ethernet PHY connection example . . . 71
Figure 45. 10/100M Ethernet PHY connection with REFCLK from RCC example . . . 72
Figure 46. Gigabit Ethernet PHY connection example with VDD = 3.3 V (RTL8211E) . . . 73
Figure 47. Gigabit Ethernet PHY connection example with VDD = 3.3 V (RTL8211F) . . . 74
Figure 48. Gigabit Ethernet PHY connection example with VDD = 1.8 V (RTL8211F) . . . 74

Figure 49. Gigabit Ethernet 2-port switch example with VDD = 3.3 V (RTL8363NB-VG) . . . . . 75
Figure 50. Display connection example with DSI. . . . . 76
Figure 51. DSI interface PCB track example for 0.8 mm ball pitch package . . . . . 77

# 1 General information

This document applies to Arm®[a]-based devices.

arm

# 2 Reference documents

The following documents are available on *www.st.com.*

**Table 1. Reference documents**

| Reference | Title |
|---|---|
| AN2867 | Oscillator design guide for ST microcontrollers |
| AN1709 | EMC design guide for ST microcontrollers |
| AN5275 | USB DFU/USART protocols used in STM32MP1 Series bootloaders |
| AN5168 | DDR configuration on STM32MP1 Series MPUs |
| AN5089 | STM32MP1 Series and STPMIC1 hardware / software integration |
| AN5122 | STM32MP1 Series DDR memory routing guidelines |
| AN5256 | STM32MP151, STM32MP153 and STM32MP157 discrete power supply hardware integration |
| UM2535 | Evaluation boards with STM32MP157 MPUs |
| UM2534 | Discovery kits with STM32MP157 MPUs |
| RM0441 | STM32MP151 advanced Arm®-based 32-bit MPUs |
| RM0442 | STM32MP153 advanced Arm®-based 32-bit MPUs |
| RM0436 | STM32MP157 advanced Arm®-based 32-bit MPUs |
| DS12500 | STM32MP151A/D datasheet |
| DS12501 | STM32MP151C/F datasheet |
| DS12502 | STM32MP153A/D datasheet |
| DS12503 | STM32MP153C/F datasheet |
| DS12504 | STM32MP157A/D datasheet |
| DS12505 | STM32MP157C/F datasheet |

a. Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

# 3 Glossary

**Table 2. Glossary**

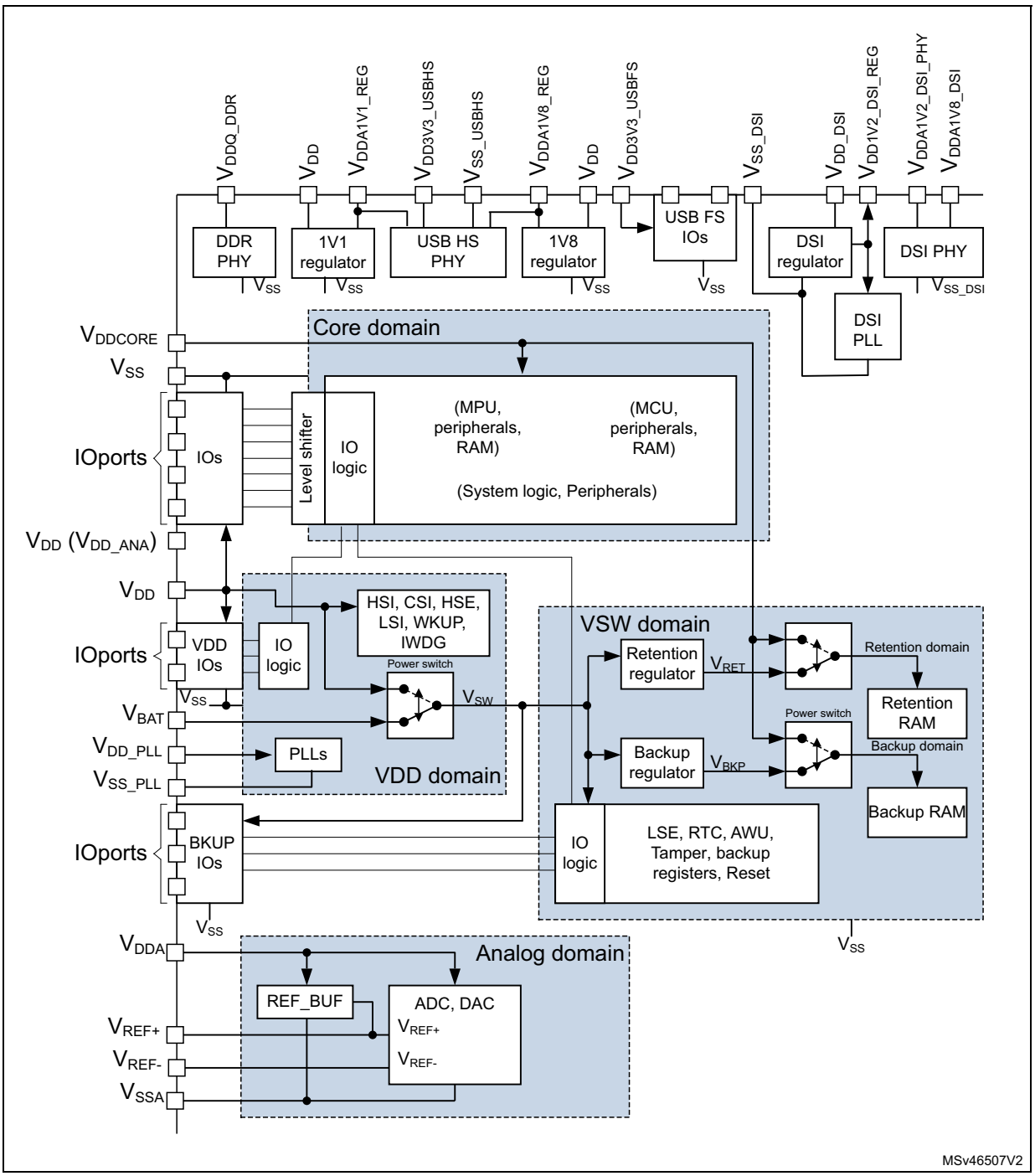
| Term | Meaning |
|---|---|
| ADC | Analog to digital converter |
| AHB | Advanced high-performance bus |
| CSI | Low power internal oscillator |
| CTI | Cross-trigger interface |
| DAC | Digital to analog converter |
| DAP | Debug access port |
| DDRCTRL | Double data rate SDRAM controller. Supports LPDDR2 and DDR3/DDR3L protocols |
| DDRPHYC | DDR physical interface control |
| DSI | Display serial interface master |
| ETH | Ethernet controller |
| EXTI | Extended interrupt and event controller |
| FMC | Flexible memory controller |
| GPIO | General purpose input output |
| HDP | Hardware debug port |
| HSE | High-speed external quartz oscillator |
| HSI | High-speed internal oscillator |
| I2C | Inter IC bus |
| IWDG | Independent watchdog |
| JTAG | Joint test action group. A debug interface |
| LSE | Low-speed external quartz oscillator |
| LSI | Low-speed internal oscillator |
| MDIOS | Management data input/output slave. Interface used to control Ethernet physical Interface |
| OTG | USB on the Go. An USB standard for interface able to become host or device |
| OTP | One time program memory |
| PMIC | Power management integrated circuit. External circuit which provides various platform power supplies with large controllability through signals and serial interface |
| PWR | Power control |
| QUADSPI | Quad data lanes serial peripheral interface |
| RCC | Reset and clock control |
| ROM | Read-only memory |
| RTC | Real time clock |

**Table 2. Glossary (continued)**

| Term | Meaning |
|---|---|
| SDMMC | Secure digital and multiMedia card interface. Supports SD, MMC, eMMC and SDIO protocols |
| SMPS | Switched mode power supply |
| SPI | Serial peripheral interface |
| STM | System trace macrocell |
| SW | Software |
| SWD | Serial wire debug |
| SWO | Single wire output. A trace port |
| SYSCFG | System configuration |
| TAMP | Tamper detection IP |
| TEMP | Temperature sensor |
| UART | Universal asynchronous receiver/transmitter |
| USART | Universal synchronous/asynchronous receiver/transmitter |
| USB | Universal serial bus |
| USBH | USB host controller |
| VREFBUF | ADC/DAC voltage reference buffer |

# 4 Power supplies

**Figure 1. Power supply scheme**



## 4.1 Introduction

*Note: See details and guaranteed operating points in product datasheets.*

- The main I/Os voltage supply ($V_{DD}$) range is 1.71 V to 3.6 V.
- The core logic operating voltage supply ($V_{DDCORE}$) range is 1.18 V to 1.25 V.
- The USB supplies ($V_{DD3V3\_USBHS}$ and $V_{DD3V3\_USBFS}$) range is 3.07 V to 3.6 V.
- Embedded regulators are used to supply some internal blocks.
  - 1.2 V LDO for DSI available on $V_{DD1V2\_DSI\_REG}$ which is used to supply DSI PLL and $V_{DD1V2\_DSI\_PHY}$ pin. Range is 1.15 V to 1.26 V.
  - 1.8 V LDO for DSI and USB available on $V_{DDA1V8\_REG}$ which is used to supply USB internally and $V_{DDA1V8\_DSI}$.
    When BYPASS_REG1V8 = $V_{DD}$, $V_{DDA1V8\_REG}$ must be supplied externally. In that case, range is 1.65 V to 1.95 V.
  - 1.1 V LDO for USB available on $V_{DD1V1\_REG}$ for external decoupling

  Note: Embedded regulators must not be used to supply external components.
- The real-time clock (RTC) and backup registers are powered from the $V_{BAT}$ voltage when the main $V_{DD}$ supply is powered off. This internal supply with automatic switch between $V_{BAT}$ and $V_{DD}$ is named $V_{SW}$ domain and is also used to supply PI8, PC13, PC14, PC15 pads.

  $V_{BAT}$ voltage range is 1.20 V to 3.6 V.

  When $V_{DD}$ is above $V_{BAT}$, a small charging current is enabled on $V_{BAT}$ for an external backup voltage device (for example a supercapacitor).

### 4.1.1 Independent ADC and DAC converter supply and reference voltage

To improve the conversion accuracy and dynamic range, the ADC, DAC and reference have an independent power supply that can be filtered separately, and shielded from noise on the PCB.

The analog operating voltage supply ($V_{DDA}$) range is 1.71 V to 3.6 V (DAC is only used when $V_{DDA}$ is above or equal 1.8 V).

- The ADC/DAC/VREFBUF voltage supply input is available on a separate $V_{DDA}$ pin.
- An isolated supply ground connection is provided on the $V_{SSA}$ pin.
  In all cases, the $V_{SSA}$ pin must be externally connected to same supply ground than $V_{SS}$.

#### External VREF

The user can connect a separate external reference voltage ADC/DAC input on $V_{REF+}$. The voltage on $V_{REF+}$ may range from 1.62 V to $V_{DDA}$.

*Note: In order to work, DAC requires $V_{REF+}$ above 1.8 V.*

#### Internal VREF

The user can enable in the VREFBUF block an internal reference voltage on $V_{REF+}$.
The voltage selection on $V_{REF+}$ is between 1.5 V, 1.8 V, 2.048 V and 2.5 V.

With internal VREF available on $V_{REF+}$ pin, it can be used externally (for example for analog comparator reference) if loading is kept within datasheet values.

*Note: In order to work, the DAC requires $V_{REF+}$ above 1.8 V.*

*Note: The VREFBUF requires $V_{DDA}$ equal to or higher than $V_{REF+}$ + 0.3 V.*

**Caution:** When available (depending on package), $V_{REF-}$ must be externally tied to $V_{SSA}$.

### Booster for ADC analog input switches

The ADC inputs are multiplexed with analog switches which have reduced performances when $V_{DDA}$ supply is below 2.7 V. In order to get maximum ADC analog performances, it is alternatively possible to supply analog switches with either $V_{DD}$ (if above 2.7 V) or an embedded 3.3 V booster from $V_{DDA}$.

The control is done in the SYSCFG_PMCR register.

**Table 3. Recommended settings for ANASWVDD and EN_BOOSTER**

| $V_{DDA}$ (V) | $V_{DD}$ (V) | --> | SYSCFG_PMCR. ANASWVDD | SYSCFG_PMCR. EN_BOOSTER | Switches supply | ADC analog performances |
|---|---|---|---|---|---|---|
| >2.7 | 1.71 to 3.6 | - | 0 | 0 | $V_{DDA}$ (>2.7 V) | Maximum |
| <2.7 | >2.7 | - | 1 | 0 | $V_{DD}$ (>2.7 V) | |
| | <2.7 | - | 0 | 1(1) | Booster (~3.3 V) | |
| | | | | 0(2) | $V_{DDA}$ (<2.7 V) | Reduced |

1. Booster voltage takes up to 50 µs to stabilize.
2. If reduced ADC analog performance is acceptable, the booster disabled can save up to 250 µA.

## 4.1.2 Battery backup

To retain the content of the backup registers, BKPSRAM and RETRAM, when $V_{DD}$ is turned off, the $V_{BAT}$ pin can be connected to an optional standby voltage supplied by a battery or another source.

The $V_{BAT}$ pin also powers the RTC unit, allowing the RTC to operate even when the main digital supply ($V_{DD}$) is turned off. The switch to the $V_{BAT}$ supply is controlled by the power down reset (PDR) circuitry embedded in the reset block.

If no external battery is used in the application, it is required to connect $V_{BAT}$ externally to $V_{DD}$.

## 4.1.3 Voltage regulators

The 1.8 V LDO (for USB and DSI) is always enabled after power on reset if BYPASS_REG1V8 = $V_{SS}$. It is not affected by (LP/LPLV-)Stop, however disabled on Standby entry.

The 1.1 V LDO (for USB) is always enabled after power on reset. It is not affected by (LP/LPLV-)Stop, however disabled on Standby entry.

The 1.2 V LDO (for DSI) is disabled after system reset and must be enabled by software before DSI is used. It is not affected by (LP/LPLV-)Stop, however disabled on Standby entry.

*Note: The embedded regulators must not be used to supply external components unless specifically mentioned.*

## 4.2 Power supply schemes

The circuit is powered by multiple power supplies:

- The $V_{DD}$ is the main supply for I/Os and internal part kept powered during the Standby mode. The useful voltage range is 1.71 V to 3.6 V (for example: 1.8 V, 2.5 V, 3.0 V or 3.3 V typical)
  - Those supplies must be connected to external decoupling capacitors (see *Table 4*).
  - $V_{DD\_DSI}$, $V_{DD\_PLL}$ and $V_{DD\_ANA}$ must be connected to $V_{DD}$
- The $V_{DDCORE}$ is the main digital voltage and shutdowns externally during the Standby mode. The voltage range during Run mode is 1.18 V to 1.25/1.38 V (1.2/1.34 V typical).
  - This supply must be connected to external decoupling capacitors (see *Table 4*)
  - $V_{DDCORE}$ is reduced further in specific Stop mode (LPLV_Stop). This involves either PWR_ON signal (for example with STPMIC1, external power management IC) or PWR_LP signal (with discrete SMPS components)
- The $V_{BAT}$ pin can be connected to the external battery (1.2 V < $V_{BAT}$ < 3.6 V).
  - If RETRAM is used, minimum $V_{BAT}$ is 1.4 V
  - If the application does not support backup battery, it is recommended to connect this pin to $V_{DD}$.
  - If the application supports backup battery, it is recommended to add a 100 nF ceramic decoupling capacitor between $V_{BAT}$ and $V_{SS}$.
  - If the application uses a supercapacitor on $V_{BAT}$, no additional decoupling is required.
- The $V_{DDA}$ pin is the analog (ADC/DAC/VREFBUF) supply and must be connected to external decoupling capacitors (see *Table 4*).
- The $V_{REF+}$ pin can be connected to the $V_{DDA}$ external power supply. If a separate, internal or external, reference voltage is applied on $V_{REF+}$, a decoupling capacitor must be connected between this pin and $V_{REF-}$ (see *Table 4*). Refer to *Section 4.1.1*.

  Additional precautions allow to filter analog noise:
  - $V_{DDA}$ can be connected to $V_{DD}$ through an inductor based filter.
- $V_{DDQ\_DDR}$ is the DDR I/O supply and must be connected to external decoupling capacitors (see *Table 4*).
  - Voltage range is 1.425 V to 1.575 V for interfacing DDR3 memories (1.5 V typical)
  - Voltage range is 1.283 V to 1.45 V for interfacing DDR3L memories (1.35 V typical)
  - Voltage range is 1.14 V to 1.3 V for interfacing LPDDR2 or LPDDR3 memories (1.2 V typical)
- $V_{DDA1V2\_DSI\_REG}$ pin is the output of internal regulator and must be connected to external decoupling capacitors (see *Table 4*).
  - $V_{DDA1V2\_DSI\_REG}$ is connected internally to DSI PLL.
- $V_{DDA1V2\_DSI\_PHY}$ is the analog DSI PHY supply. Voltage range is 1.15 V to 1.26 V. (1.2 V typical)

  $V_{DDA1V2\_DSI\_PHY}$ must be connected to $V_{DDA1V2\_DSI\_REG}$.

- $V_{DD3V3\_USBHS}$ and $V_{DD3V3\_USBFS}$ are respectively the USB high-speed and full-speed PHY supply. Voltage range is 3.07 V to 3.6 V. Must be connected together to external decoupling capacitors (see *Table 4*).

  $V_{DD3V3\_USBFS}$ is used to supply OTG_VBUS and OTG_ID (PA10) pins. Therefore, $V_{DD3V3\_USBFS}$ must be supplied as well when USB high-speed dual-role-port or USB high-speed device is used. If not used, it must be connected to $V_{DD}$.
- The $V_{DDA1V8\_REG}$ pin is the output of internal regulator and must be connected to external decoupling capacitors (see *Table 4*).
  - $V_{DDA1V8\_REG}$, is connected internally to USB PHY and USB PLL.
  - Internal $V_{DDA1V8\_REG}$ regulator is enabled by default and is controlled by the software. It is always shutdown during Standby.

  For the 1.8 V voltage regulator configuration, there is specific BYPASS_REG1V8 pin that must be connected either to $V_{SS}$ or $V_{DD}$ to activate or deactivate the voltage regulator. It is mandatory to bypass the 1.8 V regulator when $V_{DD}$ is below 2.25 V:
  - BYPASS_REG1V8 = $V_{DD}$. In that case, $V_{DDA1V8\_REG}$ pin must be connected to $V_{DD}$ (if below 1.98V) or a dedicated 1.65 V - 1.98 V supply (1.8 V typical).
  - BYPASS_REG1V8 = $V_{SS}$. In that case, $V_{DD}$ must be above 2.25 V to allow correct behavior of 1.8 V voltage regulator.
  - Refer to *Section 4.1.3* and section *Embedded regulators characteristics* of the related device datasheet for details.
- $V_{DDA1V8\_DSI}$ is the analog DSI supply. the voltage range is 1.65 V to 1.98 V. (1.8 V typical.)
  It must be connected to $V_{DDA1V8\_REG}$ and to the external decoupling capacitors (see *Table 4*).
- $V_{DDA1V1\_REG}$ pin is the output of internal regulator and must be connected to external decoupling capacitors (see *Table 4*). The voltage range is 1.045 V to 1.155 V (1.1 V typical)
  - $V_{DDA1V1\_REG}$ is connected internally to USB PHY.
  - Internal $V_{DDA1V1\_REG}$ regulator is enabled by default and is controlled by the software. It is always shutdown during Standby.

**Caution:** $V_{DD3V3\_USBHS}$ must not be present unless $V_{DDA1V8\_REG}$ is present, otherwise permanent STM32MP15x lines damage can occur. It must be ensured by PMIC ranking order or with external component in case of discrete component power-supply implementation.

**Caution:** All supply grounds ($V_{SS}$, $V_{SS\_ANA}$, $V_{SS\_PLL}$, $V_{SS\_USBHS}$, $V_{SS\_DSI}$, $V_{SSA}$ and $V_{REF-}$) must connect together with power planes.

**Table 4. Amount of decoupling recommendation by package(1)**

| Supplies pins | Decoupling point(2) | Value | LFBGA354 | TFBGA257 | TFBGA361 | LFBGA448 | Comments |
|---|---|---|---|---|---|---|---|
| $V_{BAT}$ | $V_{SS}$ | 100 nF | 1 | 1 | 1 | 1 | Can be skipped if $V_{BAT}$ is connected to $V_{DD}$ or if a supercapacitor is used instead of a battery |
| $V_{DDCORE}$ | $V_{SS}$ | 1 µF(3) | 15 | 15 | 15 | 15 | Not including capacitors on PMIC/SMPS |
| $V_{DDQ\_DDR}$ | $V_{SS}$ | 1 nF | 2 | 2 | 2 | 2 | Not including capacitors on PMIC/SMPS and additional capacitors on DDR memory |
| | | 3.3 nF | 0 | 3 | 0 | 0 | |
| | | 1 µF(3) | 4 | 2 | 7 | 7 | |
| $V_{DD\_ANA}$ | $V_{SS\_ANA}$ | 1 µF(3) | 1 | -(4) | 1 | 1 | - |
| $V_{DD\_PLL}$, $V_{DD\_PLL2}$ | $V_{SS\_PLL}$, $V_{SS\_PLL2}$ | 1 µF(3) | 2 | -(4) | -(4) | 2 | Not including capacitors on PMIC/SMPS. |
| $V_{DD}$, $V_{DD\_DSI}$ | $V_{SS}$ | 1 µF(3) | 4 | 4 | 4 | 4 | |
| $V_{DD1V2\_DSI\_REG}$, $V_{DD1V2\_DSI\_PHY}$ | $V_{SS\_DSI}$ | 2.2 µF(3) | 1 | - | 1 | 1 | - |
| | $V_{SS}$ | | - | 1(5) | - | - | |
| $V_{DDA1V8\_REG}$ | $V_{SS\_USBHS}$ | 2.2 µF(3) | 1 | - | 1 | 1 | - |
| | $V_{SS}$ | | - | 1(5) | - | - | |
| $V_{DDA1V8\_DSI}$ | $V_{SS\_DSI}$ | 1 µF(3) | 1 | - | 1 | 1 | $V_{DDA1V8\_DSI}$ must be connected to $V_{DDA1V8\_REG}$ |
| | $V_{SS}$ | | - | 1(5) | - | - | |
| $V_{DDA1V1\_REG}$ | $V_{SS\_USBHS}$ | 2.2 µF(3) | 1 | - | 1 | 1 | - |
| | $V_{SS}$ | | - | 1(5) | - | - | |
| $V_{DD3V3\_USBHS}$, $V_{DD3V3\_USBFS}$ | $V_{SS\_USBHS}$ | 1 µF(3) | 1 | - | 1 | 1 | - |
| $V_{DD3V3\_USB}$ | $V_{SS}$ | | - | 1(5) | - | - | |
| $V_{DDA}$ | $V_{SSA}$ | 100 nF + 1 µF(3) | 1+1 | 1+1 | 1+1 | 1+1 | $V_{SSA}$ must be connected to $V_{SS}$ plane |
| $V_{REF+}$ | $V_{REF-}$ and $V_{SSA}$ | 100 nF + 1 µF(3) | 1+1 | - | - | 1+1 | $V_{REF-}$ must be connected to $V_{SSA}$ then $V_{SS}$ plane |
| | $V_{SSA}$ | | - | 1+1 (6) | 1+1 (6) | - | $V_{SSA}$ must be connected to $V_{SS}$ plane |

1. This table gives guidelines, the real count and values of capacitors can be adapted depending of various parameters such as, capacitor size, capacitor dielectric, PCB technology, and using results of product power integrity simulations.
2. All $V_{SS\_x}$ and $V_{SSA}$ must be connected to a common $V_{SS}$ plane.
3. Multi Layer Ceramic Capacitor type (MLCC).
4. Supply internally merged with $V_{DD}$.
5. Supply return path internally merged with $V_{SS}$.
6. $V_{REF-}$ internally merged with $V_{SSA}$.

**Table 5. Supply usage for unused features**

| Supply | Usual connection | Alternate option[1] | Pins or functions[2] | Related block |
|---|---|---|---|---|
| VDD3V3_USBHS | Dedicated 3.3 V supply | VSS (or open) | USB_DP1/DM1 pins | USBH |
| | | | USB_DP2/DM2 pins | OTG or USBH |
| VDD3V3_USBFS | Dedicated 3.3 V supply or VDD 3.3 V | VSS (or open or VDD) | PA11/PA12 pins as OTG_FS | OTG |
| | | | PA10 pins as USB_ID | OTG |
| | | | OTG_VBUS pin | OTG |
| VDD3V3_USB[3] | Dedicated 3.3 V supply | VSS (or open) | USB_DP1/DM1 pins | USBH |
| | | | USB_DP2/DM2 pins | OTG or USBH |
| | | | PA11/PA12 pins as OTG_FS | OTG |
| | | | PA10 pins as USB_ID | OTG |
| | | | OTG_VBUS pin | OTG |
| VDDA1V1_REG | Decoupling capacitor | Open | USB_DP1/DM1 pins | USBH |
| | | | USB_DP2/DM2 pins | OTG or USBH |
| VDDA1V8_REG | Decoupling capacitor or dedicated 1.8 V supply or VDD 1.8 V | Open | USB_DP1/DM1 pins | USBH |
| | | | USB_DP2/DM2 pins | OTG or USBH |
| VDDA1V8_DSI | VDDA1V8_REG | VSS (or open) | DSI_xxx pins | DSI |
| VDDA1V2_DSI_REG | Decoupling capacitor | Open | DSI_xxx pins | DSI |
| VDDA1V2_DSI_PHY | VDDA1V2_DSI_REG | VSS (or open) | DSI_xxx pins | DSI |
| VDDA | Dedicated supply or filtered VDD | VSS (or open or VDD) | ADC internal channels | ADC2 |
| | | | ADCx_INxx pins | ADC1/ADC2 |
| | | | VREFBUF usage | VREFBUF |
| | | | VREF+ pin | ADC/DAC |
| | | | DAC_OUTx usage pins | DAC |

1. Possible connection only when all related pins/functions are not used.
2. Possible connection only when all related pins/functions are not used.
3. On some package this pin is a merge of VDD3V3_USBHS and VDD3V3_USBFS.

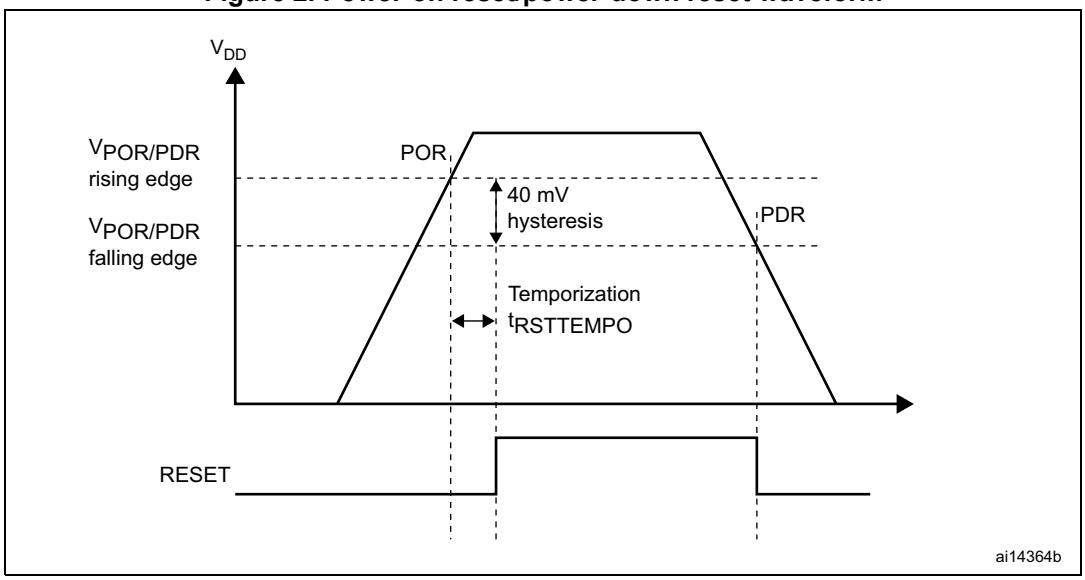
## 4.3 Reset and power supply supervisor

### 4.3.1 Power on reset (POR) / power down reset (PDR)

The device has an integrated POR/PDR circuitry that allows proper operation starting from 1.71 V.

The device remains in the reset mode as long as $V_{DD}$ is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit. For more details concerning the power on/power down reset threshold, refer to the electrical characteristics in the product datasheets.

**Figure 2. Power-on reset/power-down reset waveform**




1. $t_{RSTTEMPO}$ is approximately 2.6 ms. $V_{POR/PDR}$ rising edge is 1.67 V (typical) and $V_{POR/PDR}$ falling edge is 1.63 V (typical). Refer to STM32MP15x datasheets for actual values.

The internal power-on reset (POR) / power-down reset (PDR) circuitry can be disabled through the PDR_ON pin. In that case, an external power supply supervisor must monitor $V_{DD}$ and must maintain the device in reset mode as long as $V_{DD}$ is below a specified threshold.

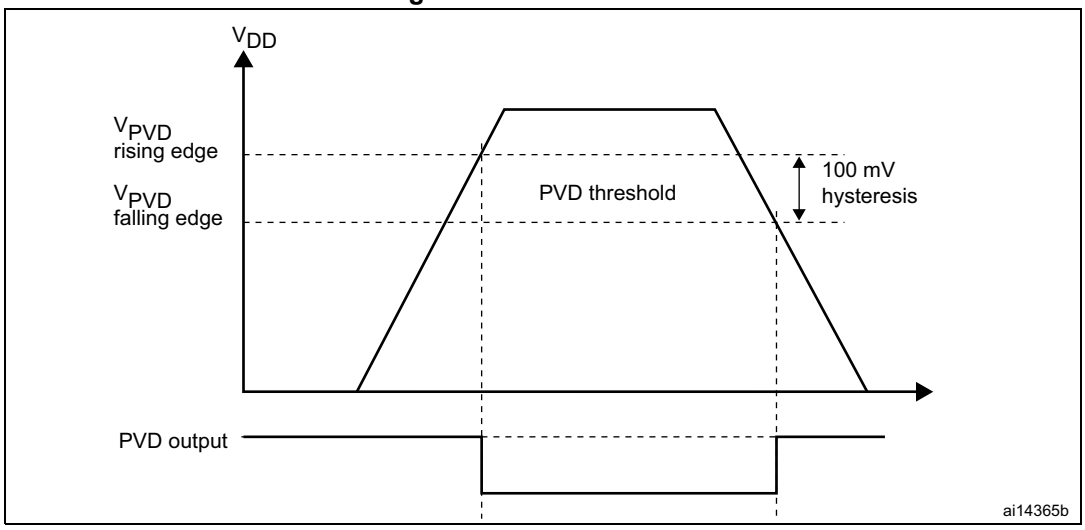
### 4.3.2 Programmable voltage detector (PVD)

The user can use the PVD to monitor the $V_{DD}$ power supply by comparing it to a threshold selected by the PLS[2:0] bits in the power control register (PWR_CR).

The PVD is enabled by setting the PVDE bit.

A PVDO flag is available, in the power control/status register (PWR_CSR), to indicate whether $V_{DD}$ is higher or lower than the PVD threshold. This event is internally connected to EXTI Line16 and generates an interrupt if enabled through the EXTI registers. The PVD output interrupt is generated when $V_{DD}$ drops below the PVD threshold and/or when $V_{DD}$ rises above the PVD threshold depending on the EXTI Line16 rising/falling edge configuration. As an example the service routine performs emergency shutdown tasks.

**Figure 3. PVD thresholds**




### 4.3.3 Application and system resets

An application reset (app_rst) is generated from one of the following sources:

- A reset from NRST pad,
- A reset from por_rst signal (generally called power-on reset),
- A reset from bor_rst signal (generally called brownout),
- A reset from the Independent Watchdogs 1 (iwdg1_rst),
- A reset from the Independent Watchdogs 2 (iwdg2_rst),
- A software reset from the Cortex-M4 (MCU), via the AIRCR register (MCSYSRST) if the option byte OPT_MCU_SYSRST_EN allows it,
- A software reset from the RCC, when the Cortex-A7 (MPU) sets the bit MPSYSRST to '1' in the RCC,
- A failure on HSE, when the clock security system feature is activated (hcss_rst).

A System reset (nreset) is generated from one of the following sources:

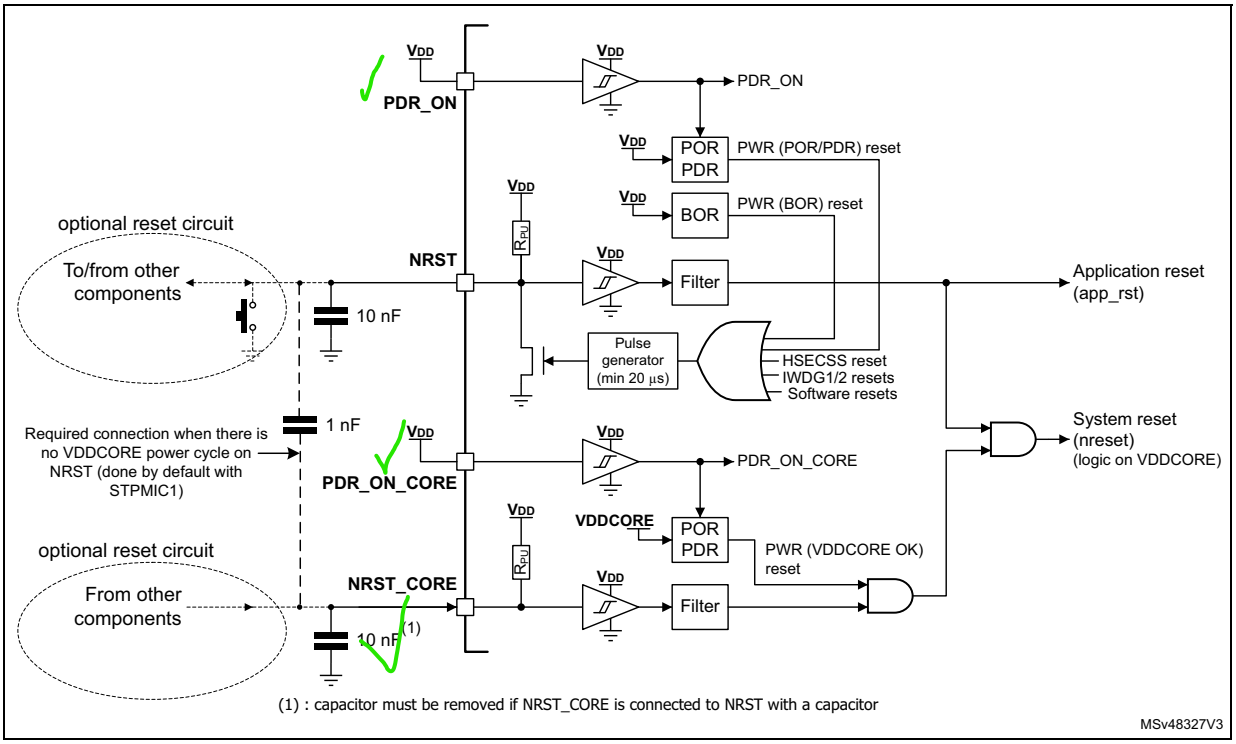
- A reset from app_rst signal (application reset),
- A reset from vcore_rst signal.

*Note: When the system is in Standby, the $V_{DDCORE}$ is switched off, while $V_{DD}$ is still present. When the system exits from Standby, the vcore_rst signal is activated, generating a nreset reset.*

*Note: It is required to connect NRST to NRST_CORE, using a capacitor of 1/10th the capacitor put on NRST, when there is no VDDCORE power cycle on NRST activation (done by default with STPMIC1). Refer to product errata sheet for details.*

Refer to RCC section in the reference manual for more details on reset coverage.

**Figure 4. Simplified reset pin circuit**



# 5 Packages

## 5.1 Package selection

The package must be selected by taking into account the constraints that are strongly dependent upon the application.

The list below summarizes the more frequent constraints:

- Amount of interfaces required.
  Interfaces not available on some packages.
  Interfaces combinations not possible on some packages.
  Refer to the product datasheets for more details
- PCB technology constraints.
  Small pitch and high-ball density require more PCB layers and higher PCB class requiring stackup with micro-via (laser via) technology
- Package height
- PCB available area
- Thermal constraints (larger packages have better thermal dissipation capabilities)

**Table 6. Package summary**

| Size (mm)[1] | 16 x 16 | 10 x 10 | 12 x 12 | 18 x 18 |
|---|---|---|---|---|
| **Minimum Pitch (mm)** | **0.8** | **0.5** | **0.5** | **0.8** |
| **Height (mm)** | **1.4** | **1.2** | **1.2** | **1.4** |
| **Sales numbers** | **LFBGA354** | **TFBGA257** | **TFBGA361** | **LFBGA448** |
| STM32MP151xxx | X | X | X | X |
| STM32MP153xxx | X | X | X | X |
| STM32MP157xxx | X | X | X | X |

1. Typical body size.

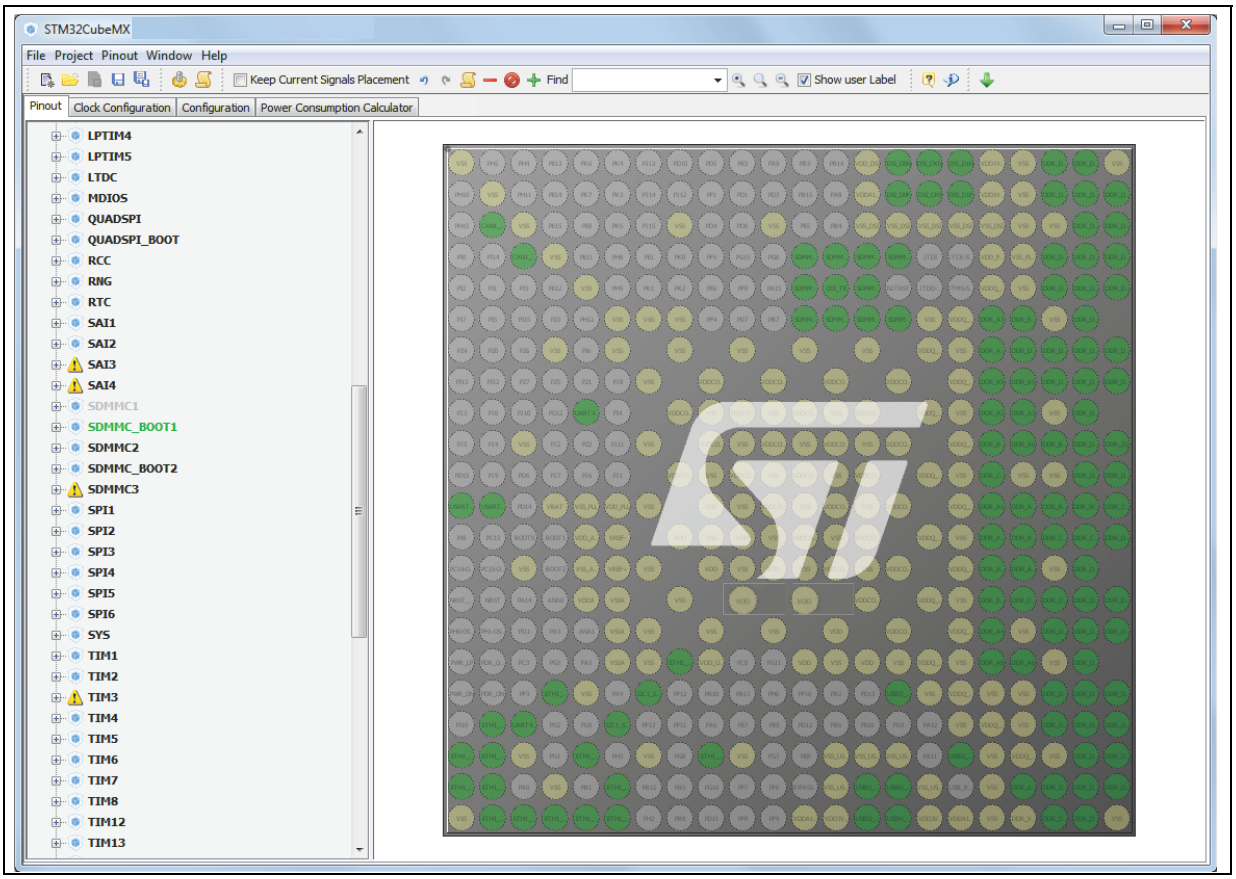
**Table 7. Major feature changes related to packages**

| Packages | | | TFBGA257 | LFBGA354 | TFBGA361 | LFBGA448 |
|---|---|---|---|---|---|---|
| Package | | Body Size (mm) | 10x10 | 16x16 | 12x12 | 18x18 |
| | | Pitch (mm) | 0.5 (center 0.65) | 0.8 | 0.5 (center 0.65) | 0.8 |
| | | Thickness (mm) | <1.2 | <1.4 | <1.2 | <1.4 |
| | | Ball count | 257 | 354 | 361 | 448 |
| SDRAM | LPDDR2/3 | 16-bits 533 MHz | Up to 1 GByte, single rank | | | |
| | | 32-bits 533 MHz | - | | Up to 1GByte, single rank | |
| | DDR3/3L | 16-bits 533 MHz | Up to 1 GByte, single rank | | | |
| | | 32-bits 533 MHz | - | | Up to 1GByte, single rank | |
| FMC | Parallel Address/Data 8/16 bits | | - | | 4 × CS, up to 4 × 64 MBytes | |
| | Parallel AD-Mux 8/16 bits | | 4 × CS, up to 4 × 64 MBytes | | | |
| | NAND 8/16 bits | | Yes, 2 × CS, SLC, BCH4/8 | | | |
| Gigabit Ethernet | | | - | | MII, RMII, GMII, RGMII with PTP and EEE | |
| 10/100M Ethernet | | | MII, RMII with PTP and EEE | | | |
| GPIOs with interrupt (total count) | | | 98 | | 148 | 176 |
| - | Securable GPIOs | | - | | 8 | |
| | Wakeup pins | | 4 | | 6 | |
| | Tamper pins (active tamper) | | 2 (1) | | 3 (1) | |
| Up to 16 bit synchronized ADC | | | 2 (up to 0.25/4.4/5/5.7/6.7 Msps on 16/14/12/10/8 bits each) | | | |
| - | Low noise 16 bit (differential) | | - | | 2 (1) | |
| | 16 bit (differential) | | 17 (7) | | 20 (9) | |
| | ADC channels in total | | 17 | | 22 | |

## 5.2 Alternate function mapping to pins

In order to easily explore peripheral alternate functions mapping to pins, it is recommended to use the STM32CubeMX tool available on *www.st.com*.

**Figure 5. STM32CubeMX example screen-shot**



## 5.3 Package compatibility between versions

The STM32MP151xxx, STM32MP153xxx devices slightly differ from the STM32MP157xxx devices. Nevertheless, it is possible to build a compatible PCB at the expense of few additional connections.

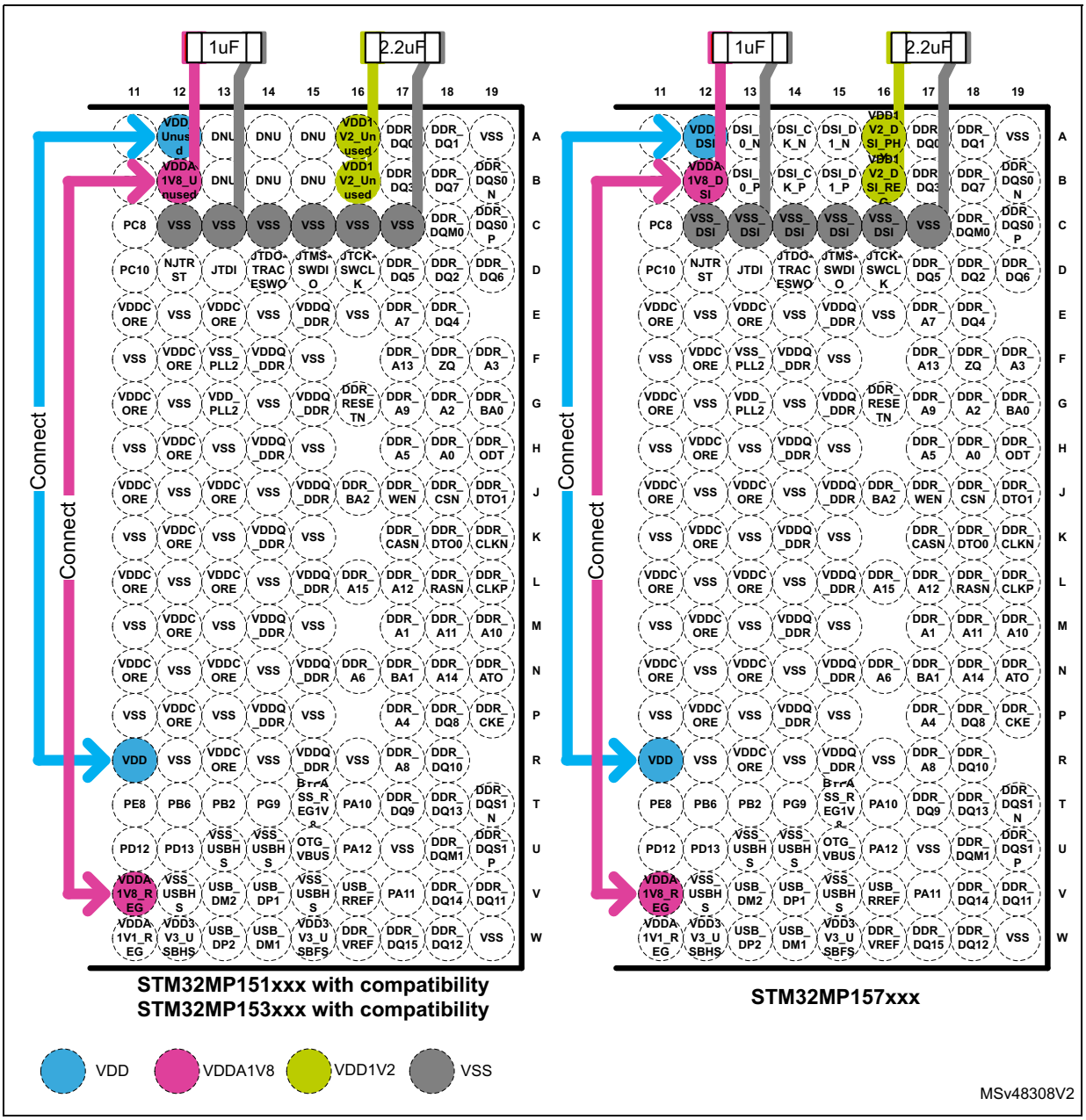
**Table 8. Device compatibility summary**

| PCB made for | Device used | | |
|---|---|---|---|
| | **STM32MP151xxx** | **STM32MP153xxx** | **STM32MP157xxx** |
| STM32MP151xxx | **Compatible** | Compatible | Compatibility possible (See *Table 9* to *Table 12* and *Figure 6* to *Figure 9*) |
| STM32MP153xxx | Compatible | **Compatible** | |
| STM32MP157xxx | Compatible | Compatible | **Compatible** |

**Table 9. STM32MP151xxx and STM32MP153xxx for 16x16 LFBGA354 compatibility**

| Ball connection to add | STM32MP151xxx | STM32MP153xxx | STM32MP157xxx |
|---|---|---|---|
| B12 to V11 (VDD1V8_REG) | VDDA1V8_Unused | | VDDA1V8_DSI |
| A16 to B16 + 1 µF to VSS | VDD1V2_Unused | | VDD1V2_DSI_PHY / VDD1V2_DSI_REG |
| A12 to VDD | VDD_Unused | | VDD_DSI |

**Figure 6. 16x16 LFBGA354 compatibility**

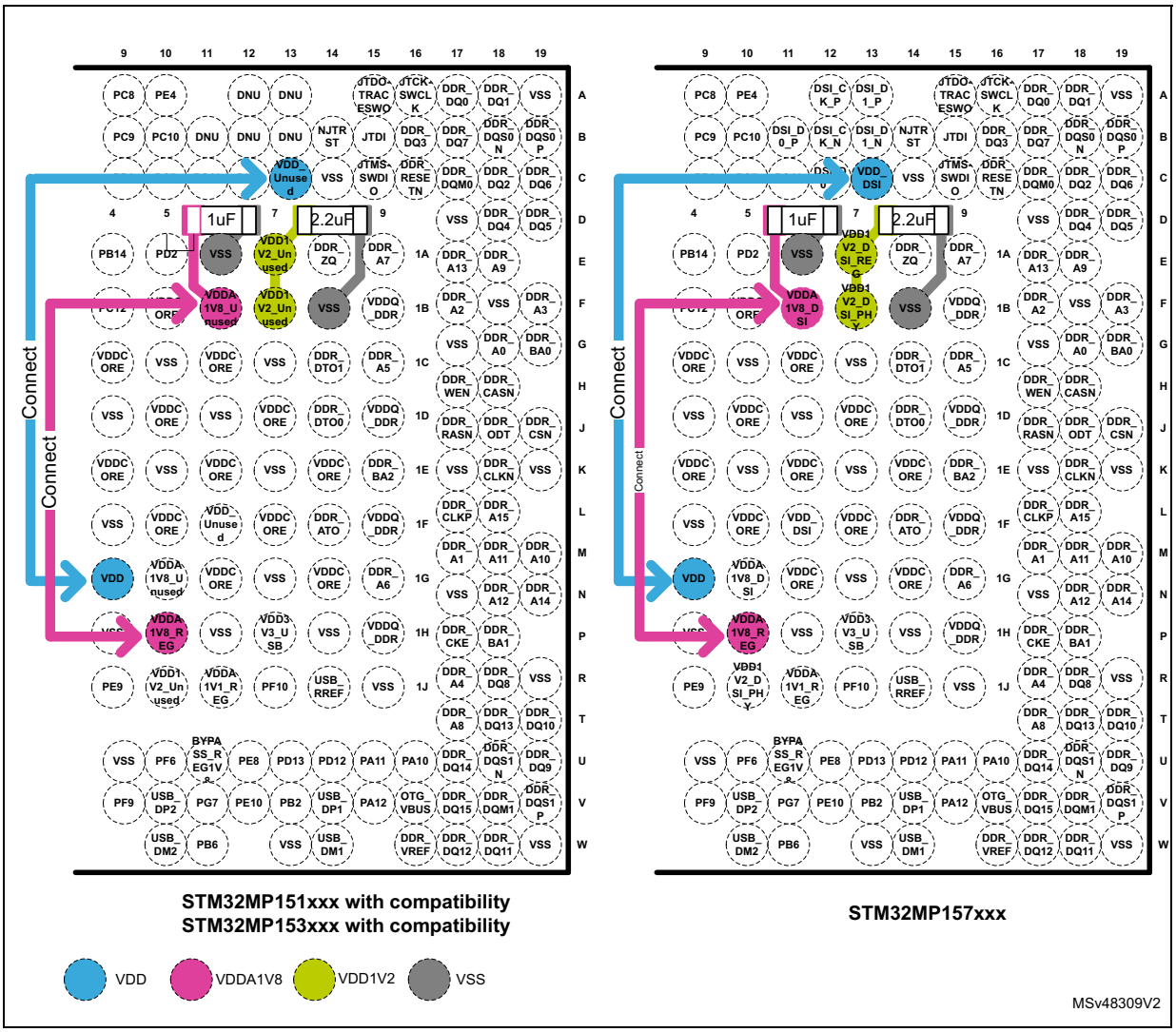



*Note: This drawing is to help understanding and does not show realistic board traces and components size/placement.*

**Table 10. STM32MP151xxx and STM32MP153xxx for 10x10 TFBGA257 compatibility**

| Ball connection to add | STM32MP151xxx | STM32MP153xxx | STM32MP157xxx |
|---|---|---|---|
| 1B6 to 1H5 (VDD1V8_REG) | VDDA1V8_Unused | | VDDA1V8_DSI |
| 1B7 to 1A7 + 1 µF to VSS | VDD1V2_Unused | | VDD1V2_DSI_PHY / VDD1V2_DSI_REG |
| C13 to VDD | VDD_Unused | | VDD_DSI |

**Figure 7. 10x10 TFBGA257 compatibility**

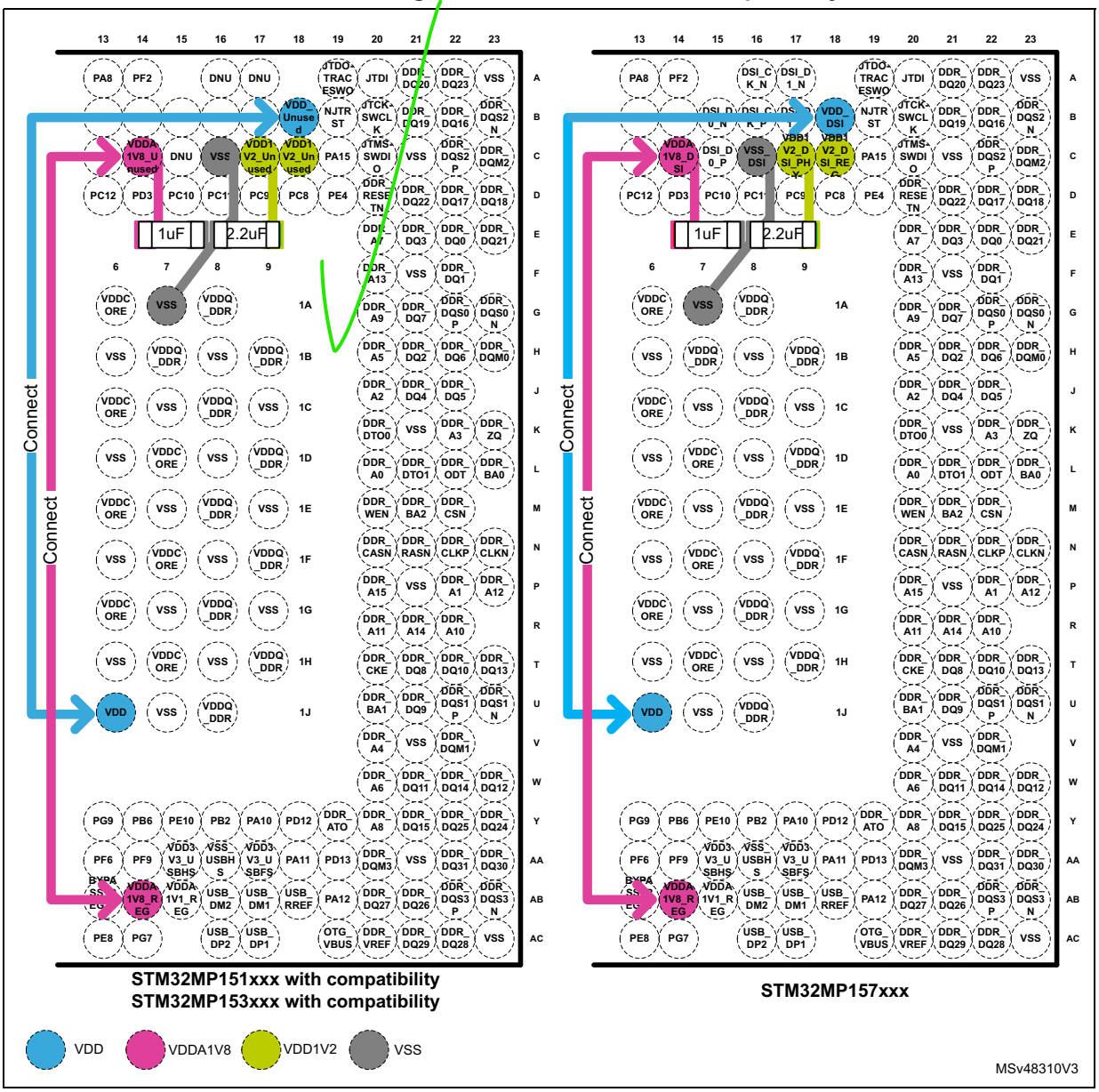



*Note: This drawing is to help understanding and does not show realistic board traces and components size/placement.*

**Table 11. STM32MP151xxx and STM32MP153xxx for 12x12 TFBGA361 compatibility**

| Ball connection to add | STM32MP151xxx | STM32MP153xxx | STM32MP157xxx |
|---|---|---|---|
| C14 to AB14 (VDD1V8_REG) | VDDA1V8_Unused | | VDDA1V8_DSI |
| C17 to C18 + 1 µF to VSS | VDD1V2_Unused | | VDD1V2_DSI_PHY / VDD1V2_DSI_REG |
| B18 to VDD | VDD_Unused | | VDD_DSI |

**Figure 8. 12x12 TFBGA361 compatibility**

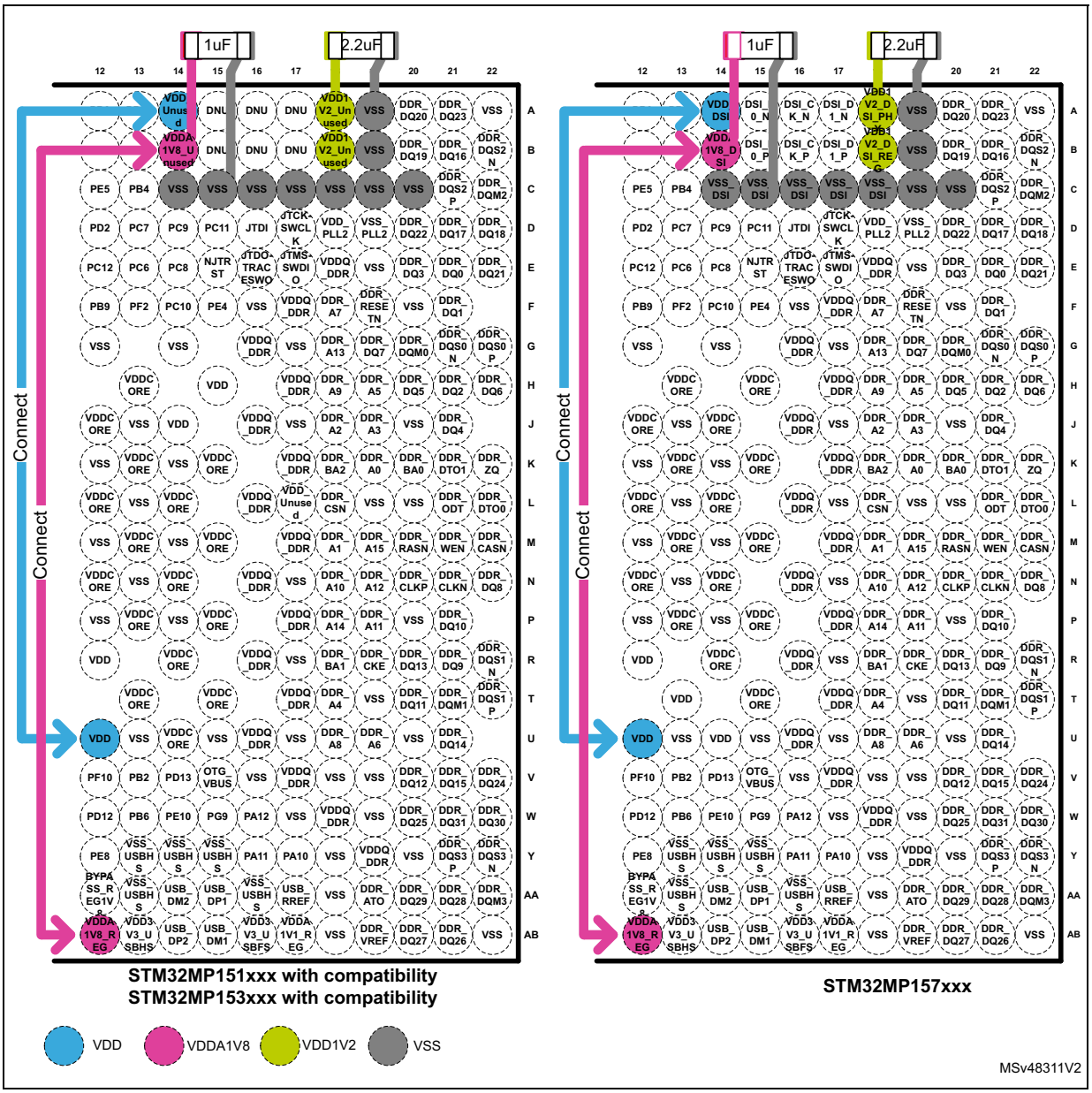



*Note: This drawing is to help understanding and does not show realistic board traces and components size/placement.*

**Table 12. STM32MP151xxx and STM32MP153xxx for 18x18 LFBGA448 compatibility**

| Ball connection to add | STM32MP151xxx | STM32MP153xxx | STM32MP157xxx |
|---|---|---|---|
| B14 to AB12 (VDD1V8_REG) | VDDA1V8_Unused | | VDDA1V8_DSI |
| A18 to B18 + 1 µF to VSS | VDD1V2_Unused | | VDD1V2_DSI_PHY / VDD1V2_DSI_REG |
| A14 to VDD | VDD_Unused | | VDD_DSI |

**Figure 9. 18x18 LFBGA448 compatibility**




*Note: This drawing is to help understanding and does not show realistic board traces and components size/placement.*

# 6 Clocks

Different clock sources are used to drive the sub-systems clocks:

- HSI oscillator clock (high-speed internal clock signal)
- CSI oscillator clock (low power internal clock signal)
- HSE oscillator clock (high-speed external clock signal)
- PLL1/2/3/4 clocks
- PLL_DSI to generate the DSI clock (up to 1 GHz)[(a)]
- PLL_USB to generate the USB clock (480 MHz)

The devices have two secondary clock sources:

- 32 kHz low-speed internal RC (LSI RC) that drives the independent watchdog and, optionally, the RTC used for auto-wakeup from the Stop/Standby modes.
- 32.768 kHz low-speed external crystal (LSE crystal) that optionally drives the real-time clock (RTCCLK)

Each clock source can be switched on or off independently when it is not used, to optimize the power consumption.

Refer to the RM0436, RM0441, RM0442 reference manuals for the description of the clock tree.

## 6.1 HSE OSC clock

The high-speed external clock signal (HSE) are generated from two possible clock sources:

- HSE user external clock (see *Figure 10*)
- HSE external crystal/ceramic resonator (see *Figure 11*)

**Figure 10. HSE external clock**

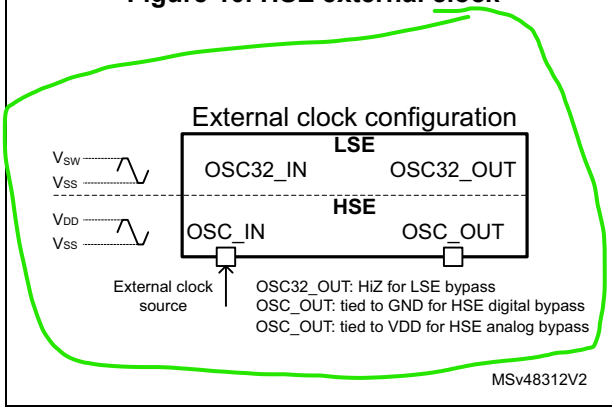
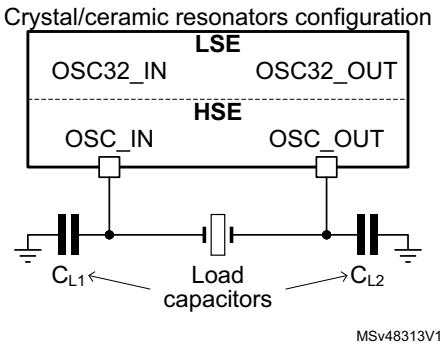



**Figure 11. HSE crystal/ceramic resonators**




1. Refer *Oscillator design guide for ST microcontrollers* application note (AN2867).
2. Load capacitance $C_L$ has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where: $C_{stray}$ is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 4 pF. Refer to *Section 9: Recommendations on page 43* to minimize its value.

a. Availability depends on the STM32MP15x lines devices.

Although low-level boot is done using internal clocks, ST supplies software packages as well as major external interfaces such as,DDR, USB that require a crystal or an external oscillator to be connected on HSE pins.

### 6.1.1 External source (HSE bypass)

In this mode, an external clock source must be provided. The frequency is from 8 MHz to up 50 MHz (refer to STM32MP15x datasheets for actual maximum value).

The external digital ($V_{IL}/V_{IH}$) or analog (amplitude of 200 mV pk-pk minimum) clock signal with a duty cycle of about 50%, has to drive the OSC_IN pin.

*Note: In order to allow USB boot, the BootROM automatically selects the HSE mode by checking the OSC_OUT connection during startup phase (that is on NRST rising edge):*

- OSC_OUT is tied to GND (max 1 Kohm): HSE digital bypass
- OSC_OUT is tied to VDD (max 1 Kohm): HSE analog bypass
- OSC_OUT high-impedance or connected to a crystal/ceramic resonator: HSE crystal/ceramic resonator mode.

When Bypass is used, the external clock generator is enabled by PWR_ON to save power (that is disabled in Standby). In that case, the OSC_IN clock input must be stable within 10 ms after the PWR_ON rising edge occurs.

### 6.1.2 External crystal/ceramic resonator (HSE crystal)

The external oscillator frequency ranges from 8 to 48 MHz.

The external oscillator has the advantage of producing a very accurate rate on the main clock. The associated hardware configuration is shown in *Figure 11*. Using a 24 MHz crystal frequency is a good choice to get accurate USB high-speed clocks.

The crystal/ceramic resonator and the load capacitors must be connected as close as possible to the oscillator pins to minimize the output distortion and startup stabilization time. The load capacitance values must be adjusted according to the selected crystal/ceramic resonator.

For $C_{L1}$ and $C_{L2}$ it is recommended to use NP0/C0G capacitors in the 5 pF-to-25 pF range (typical), selected to meet the load requirements of the crystal/ceramic resonator. $C_{L1}$ and $C_{L2,}$ have usually the same value. The crystal manufacturer typically specifies a load capacitance that is the series combination of $C_{L1}$ and $C_{L2}$. The PCB and pin capacitances must be included when sizing $C_{L1}$ and $C_{L2}$ (10 pF can be used as a rough estimate of the combined pin and board capacitance).

Refer to *oscillator design guide for ST microcontrollers* application note (AN2867) and electrical characteristics sections in the product datasheet for more details.

## 6.2 LSE OSC clock

The low-speed external clock signal (LSE) is generated from two possible clock sources:

- LSE user external clock (see *Figure 12*)
- LSE external crystal/ceramic resonator (see *Figure 13*)

**Figure 12. LSE external clock**

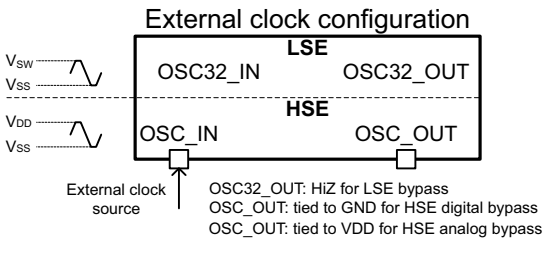
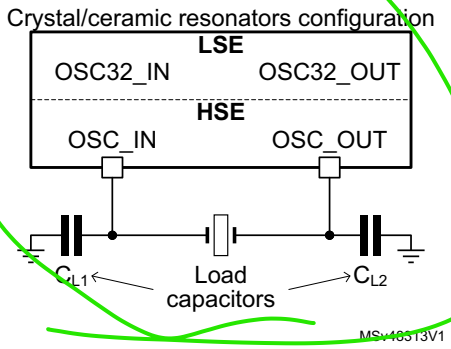



**Figure 13. LSE crystal/ceramic resonators**




1. ***Figure 13: LSE crystal/ceramic resonators*:**
   It is strongly recommended to use a resonator with a load capacitance $C_L \leq 12.5$ pF.
2. ***Figure 12: LSE external clock* and *Figure 13: LSE crystal/ceramic resonators*:**
   OSC32_IN and OSC32_OUT pins are used also as GPIO, however it is recommended not to use them as both RTC and GPIO pins in the same application.

If LSE is not used, OSC32_IN must be tied to VSS.

### 6.2.1 External source (LSE bypass)

In this mode, an external clock source must be provided. Its frequency is up to 1 MHz. The external digital (VIL/VIH) or analog (amplitude of 200 mV pk-pk minimum) clock signal with a duty cycle of about 50% has to drive the OSC32_IN pin while the OSC32_OUT pin must be left high impedance (see *Figure 12*). The configuration of the bypass mode as well as the selection between the digital and analog is done within RCC registers

### 6.2.2 External crystal/ceramic resonator (LSE crystal)

The LSE crystal is a 32.768 kHz low-speed external crystal or ceramic resonator. It has the advantage of providing a low-power, while highly accurate clock source to the real-time clock peripheral (RTC) for clock/calendar or other timing functions.

The resonator and the load capacitors must be connected as close as possible to the oscillator pins to minimize output distortion and startup stabilization time. The load capacitance values $C_{L1}$ and $C_{L2}$ must be adjusted according to the selected oscillator.

Refer to *Oscillator design guide for ST microcontrollers* dedicated application note (AN2867) and electrical characteristics sections in the product datasheet for more details.

## 6.3 Clock security system (CSS)

Refer to the product reference manual for more details (See *Table 1: Reference documents*).

### 6.3.1 CSS on HSE

The clock security system is activated by the software. In this case, the clock detector is enabled after the HSE oscillator startup delay, and disabled when this oscillator is stopped.

- If a failure is detected on the HSE oscillator clock, a system reset is generated and signaled to the TAMP block for security protection.

### 6.3.2 CSS on LSE

The clock security system is activated by the software. In this case, the clock detector is enabled after the LSE oscillator startup delay, and disabled when this oscillator is stopped.

- If a failure is detected on the LSE oscillator clock, the RTC/TAMP clock source is stopped as well as signaled to the TAMP block for security protection.

# 7 Boot configuration

## 7.1 Boot mode selection

In the STM32MP15x lines devices, different boot modes can be selected by means of the BOOT[2:0] pins. the reserved configuration is highlighted in gray in the table.

**Table 13. Boot modes**

| BOOT2 | BOOT1 | BOOT0 | Initial boot mode | Comments |
|---|---|---|---|---|
| 0 | 0 | 0 | UART and USB(1) | Wait incoming connection on:<br>– USART2/3/6 and UART4/5/7/8 on default pins<br>– USB High-Speed device on OTG_HS_DP/DM pins(2) |
| 0 | 0 | 1 | Serial NOR-Flash(3) | Serial NOR-Flash on QUADSPI(5) |
| 0 | 1 | 0 | eMMC™(3) | eMMC™ on SDMMC2 (default)(5)(6) |
| 0 | 1 | 1 | NAND-Flash(3) | SLC NAND-Flash on FMC |
| 1 | 0 | 0 | Engineering boot (No Flash boot) | Used to get debug access without boot from Flash(4) |
| 1 | 0 | 1 | SD-Card(3) | SD-Card on SDMMC1 (default)(5)(6) |
| 1 | 1 | 0 | UART and USB(1)(3) | Wait incoming connection on:<br>– USART2/3/6 and UART4/5/7/8 on default pins<br>– USB High-speed device on OTG_HS_DP/DM pins(2) |
| 1 | 1 | 1 | Serial NAND-Flash(3) | Serial NAND-Flash on QUADSPI(5) |

1. Could be disabled by OTP settings. Note that an HSE clock/crystal is always required even for UART boot, unless USB and HSE frequency auto-detection are disabled in OTP.
2. USB requires an HSE clock/crystal (see *Section 7.3: Embedded boot loader mode*).
3. Boot source can be changed by OTP settings (such as Initial boot on SD-Card, then eMMC with OTP settings).
4. Cortex-A7 Core0 in infinite loop toggling PA13, Cortex-M4 in infinite loop on RETRAM.
5. Default pins can be altered by OTP.
6. Alternatively, another SDMMC interface than this default can be selected by OTP.

The values on the BOOT pins are sampled by BootROM after a reset. It is up to the user to set the BOOT[2:0] pins before reset exit to select the required boot mode.

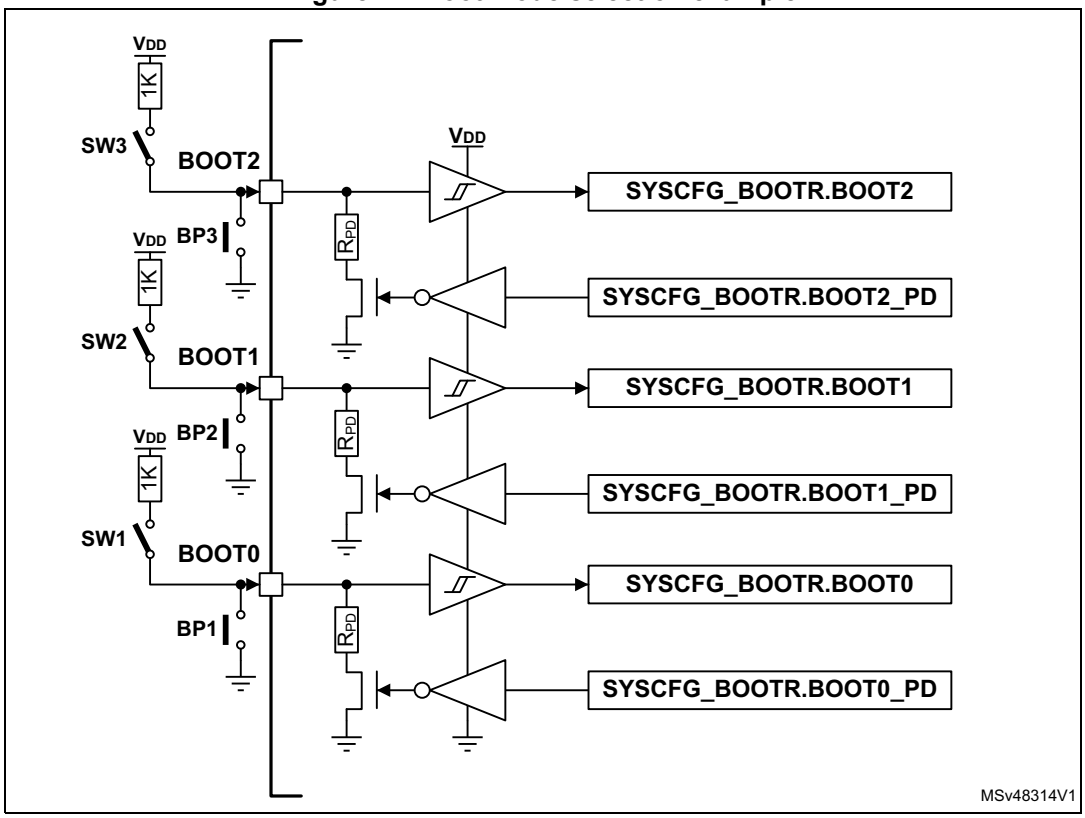
The BOOT pins can also be resampled later by software (for example by reading SYSCFG.BOOTR_BOOT[2:0] field) or by the BootROM when exiting the Standby mode. Consequently, they must be kept in the required boot mode configuration all the time.

During Stop modes, when the BOOT[2:0] pins are connected to $V_{DD}$, as the three embedded pull-down are enabled by default, some current is flowing through the pull-down. In order to save some tens of µA of power, the software can disable the pull-down on pins which are connected to $V_{DD}$ by simply setting field SYSCFG_BOOTR.BOOT[2:0]_PD equal to value read in SYSCFG_BOOTR.BOOT[2:0] field. This must be done again after each Standby exit as the SYSCFG_BOOTR register is reset. Note that during Standby, the BOOT[2:0] pins are set in tri-state and no current is flowing in BOOT[2:0] pins even if connected to $V_{DD}$.

## 7.2 Boot pin connection

*Figure 14* shows an example of the external connection required to select the boot memory of the STM32MP15x lines devices.

**Figure 14. Boot mode selection example**




Despite all the recovery cases in the software, there is a risk that with wrong or corrupted Flash content (such as, user mistake, bad Flash content programmed, power lost), the system does not start (also known as bricked).

Note that on empty Flash, the boot code automatically switches to UART/USB connection.

It is possible having to force the use of UART/USB connection to allow the board Flash re-programming for example, after sale services or firmware update.

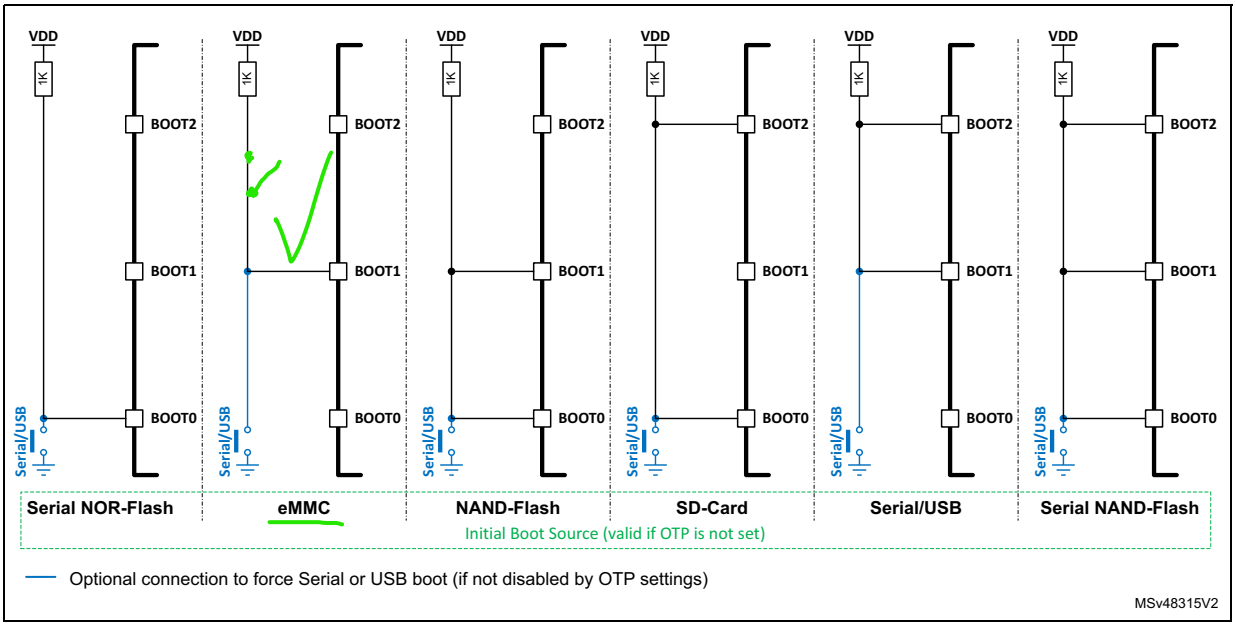
There are also cases of where initial boot is done on a different Flash than regular boot (for example the initial boot from SD-Card, which copies binary data in another Flash like Serial NOR, Serial NAND, eMMC or SLC NAND). This is possible as the initial boot code can set relevant OTP bits to force future boot from the programmed Flash (see *Figure 16*). This allows a simplified and flexible mass production without intervention on BOOT pins.

The typical connections examples for final board are described in *Figure 15*.

The switches are done by various ways such as, pushbutton, solder bridges, connector contacts, test points while assumed *open* by default during normal product boot to avoid current flow in external resistors.

Note that OTP configuration forces or forbids any of the boot sources to comply with product security requirements.

**Figure 15. BOOT pins typical connection schematics**



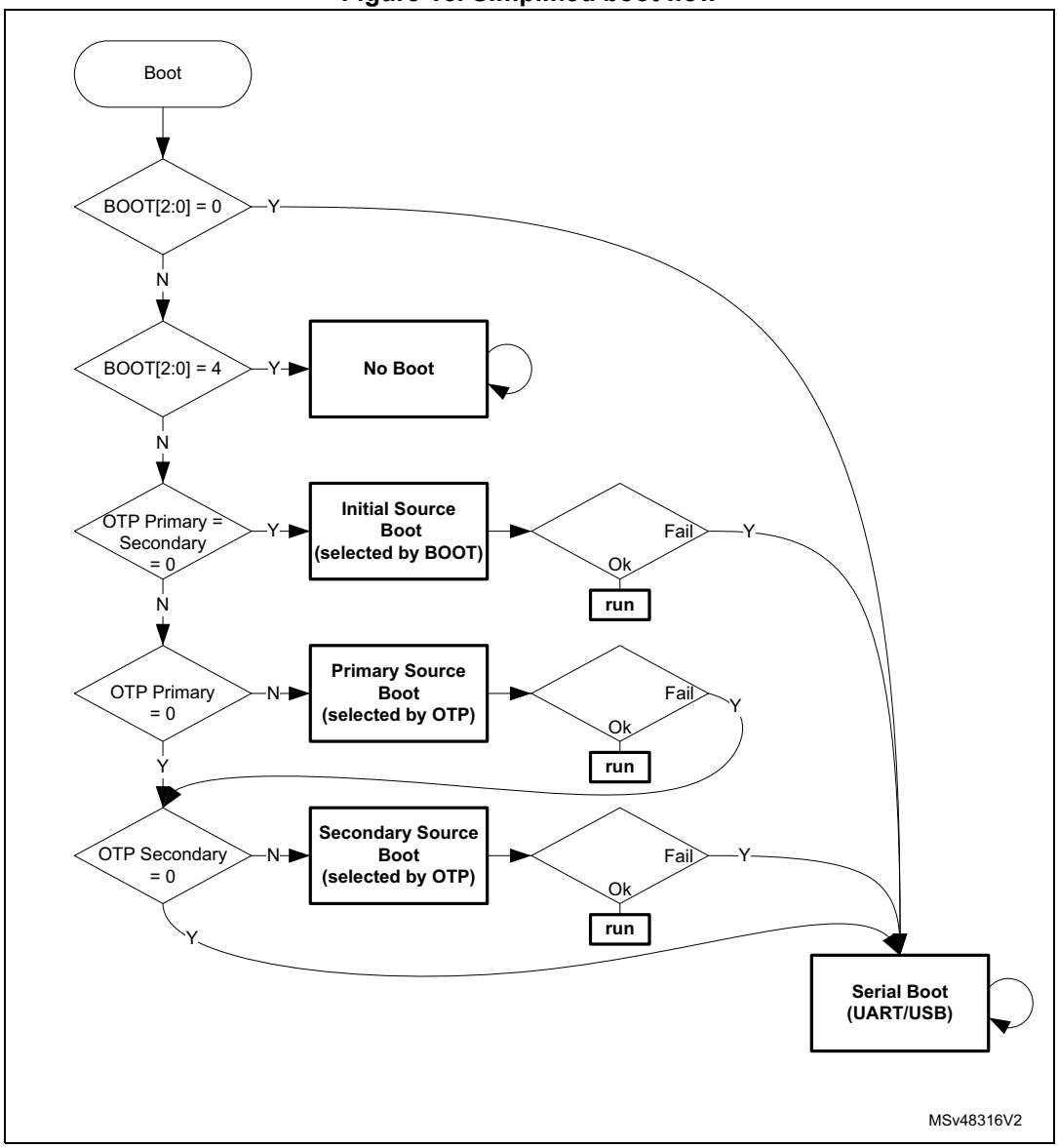
## 7.3 Embedded boot loader mode

This embedded boot loader is located in the BootROM memory.

For additional information, refer to *USB DFU/USART protocols used in STM32MP1 Series bootloaders* (AN5275) (*Table 1*).

During boot, the QUADSPI, FMC, SDMMC and USART peripherals operates with the internal 64 MHz oscillator (HSI).
The USB OTG HS device, however functions only if an external clock (HSE) is present with a default frequency of either 8, 10, 12, 14, 16, 20, 24, 28, 32, 36, 40 or 48 MHz (automatic detection). Alternatively, a fixed 24, 25 or 26 MHz frequency is used with OTP settings).

**Figure 16. Simplified boot flow**



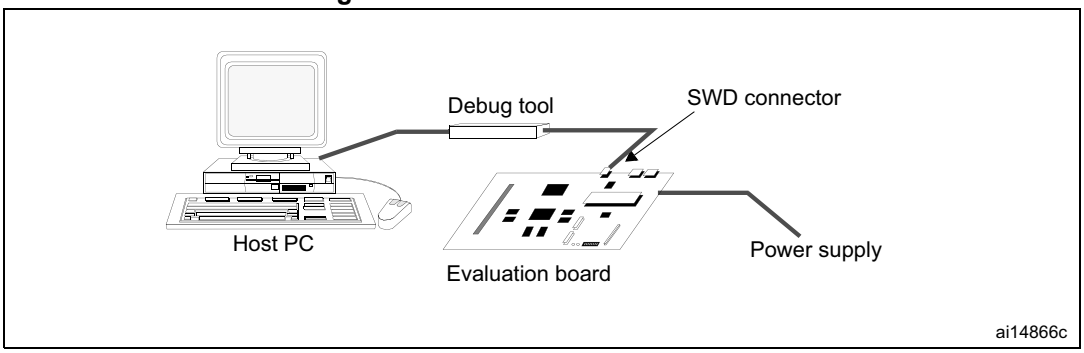
# 8 Debug management

## 8.1 Introduction

The Host/target interface is the hardware equipment that connects the host to the application board. This interface is made of three components: a hardware debug tool, a JTAG or SWD connector and a cable connecting the host to the debug tool.

*Figure 17* shows the connection of the host to the evaluation board.

**Figure 17. Host-to-board connection**




## 8.2 SWJ debug port (serial wire and JTAG)

The STM32MP15x lines core integrates the Serial Wire / JTAG debug port (SWJ-DP). It is an Arm® standard CoreSight™ debug port that combines a JTAG-DP (5-pin) interface and a SW-DP (2-pin) interface.

- The JTAG debug port (JTAG-DP) provides a 5-pin standard JTAG interface to the AHP-AP port
- The serial wire debug port (SW-DP) provides a 2-pin (clock + data) interface to the AHB-AP port

The two pins of the SW-DP are multiplexed with two of the five JTAG pins of the JTAG-DP.

## 8.3 Pinout and debug port pins

### 8.3.1 Internal pull-up and pull-down resistors on JTAG pins

To avoid any uncontrolled I/O levels, the STM32MP15x lines embed internal pull-up and pull-down resistors on JTAG pins:

- NJTRST: Internal pull-up
- JTDI: Internal pull-up
- JTDO-TRACESWO: Internal pull-up
- JTMS-SWDIO: Internal pull-up
- JTCK-SWCLK: Internal pull-down

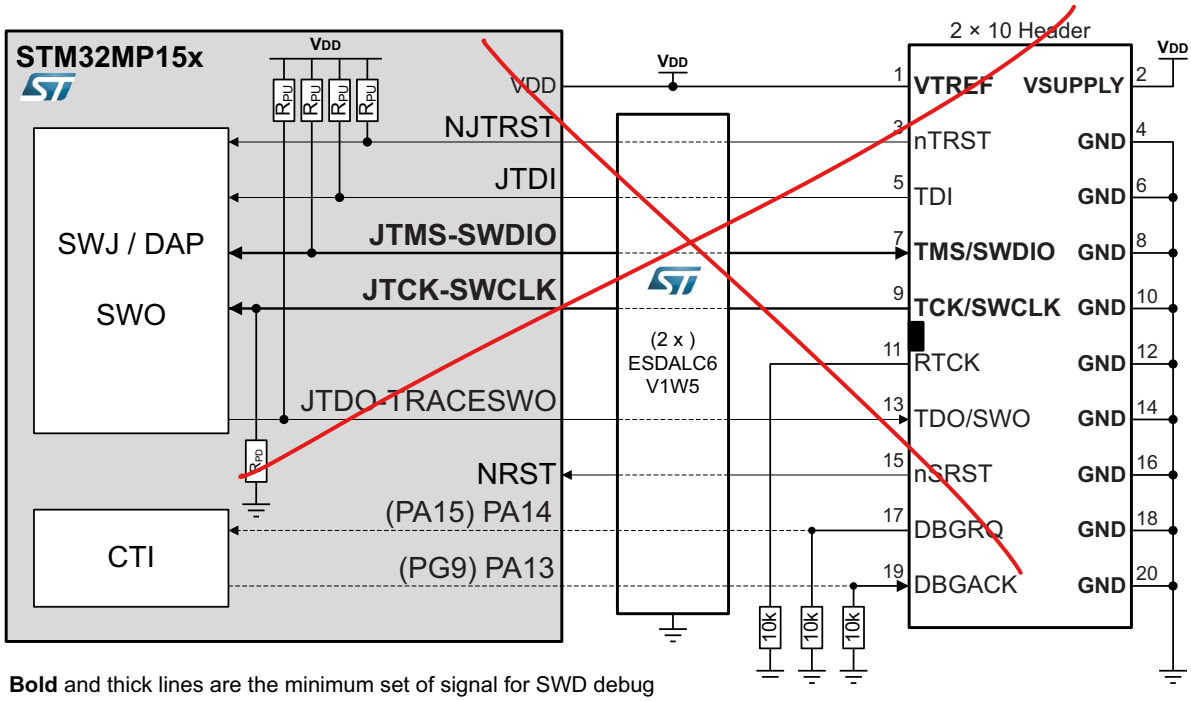
*Note: The JTAG IEEE standard recommends to add pull-up resistors on TDI, TMS and nTRST, there is no special recommendation for TCK. However, for the* STM32MP15x lines*, an integrated pull-down resistor is used for JTCK.*

*Embedded pull-up and pull-down resistors removes the need to add external resistors.*

### 8.3.2 Debug port connection with standard JTAG connector

*Figure 18* shows the connection between the STM32MP15x lines and a standard JTAG/SWD connector.

**Figure 18. JTAG/SWD MIPI10 connector implementation example**



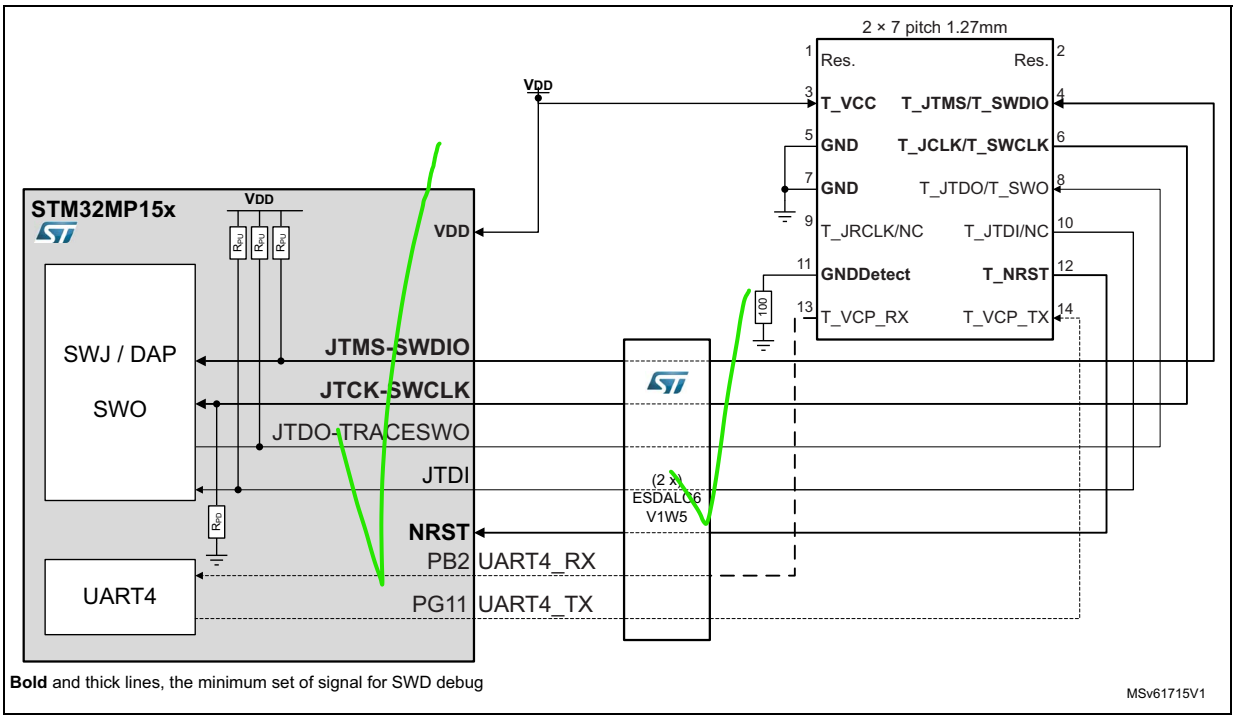

*Note: The single wire trace on TRACESWO pin is only available for Cortex-M4 core. To trace all cores activity, a parallel trace port must be used (see Section 8.3.4: Parallel trace and HDP).*

### 8.3.3 Debug port and UART connection with STDC14 connector

*Figure 19* shows the connection between the STM32MP15x lines and a STDC14 connector including UART virtual com port connection.

Reference example for STDC14 header is FTSH-107-01-L-DV-K-A

**Figure 19. JTAG/SWD/UART VCP STDC14 connector implementation example**




*Note: The single wire trace on TRACESWO pin is only available for Cortex-M4 Core. To trace all cores activity, a parallel trace port must be used (see Section 8.3.4: Parallel trace and HDP).*

*Note: STDC14 connector is respecting (from pin 3 to pin 12) the Arm10 pinout (Arm Cortex debug connector).*

### 8.3.4 Parallel trace and HDP

#### Parallel trace

TRACED[15:0] and TRACECLK signals are available as alternate functions on I/Os pins. The user can select number of trace data N = 1, 2, 4, 8 or 16 pins. Less trace data mean lower available trace bandwidth, therefore less information is traced (such as, the number of trace sources, code and/or data tracing) without trace overrun (there is a 8 Kbytes buffer in STM32MP15x lines). For each product, a trade-off between available features and trace bus might lead to have reduced feature while using trace during product development.

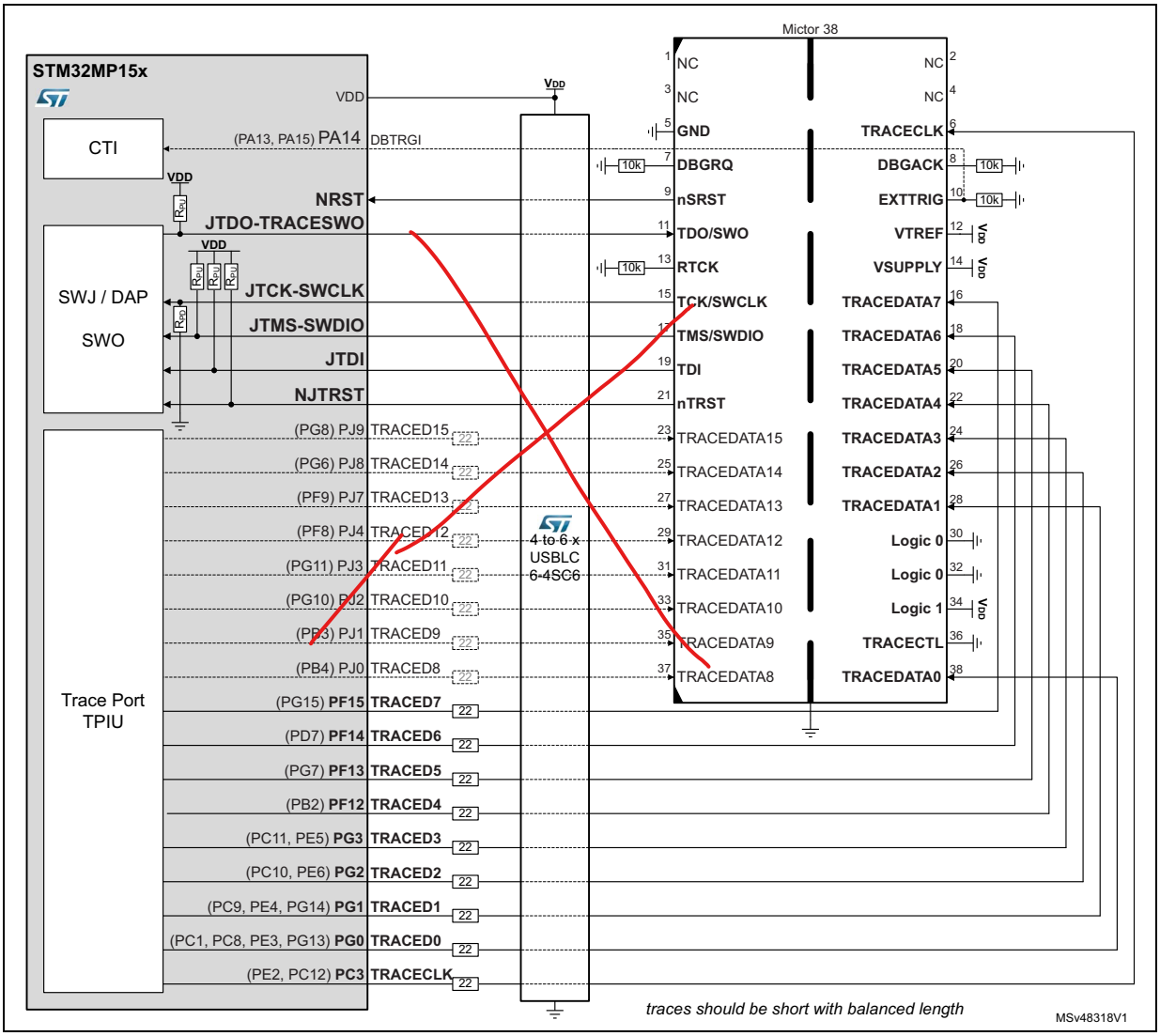
The trace is compliant to Arm® CoreSight™ trace and requires a dedicated tracing tool to be interpreted and correlated with debugging done through SWD or JTAG.

For more information on the Trace Port Interface CoreSight™ component, refer to product reference manual and the Arm® CoreSight™ SoC-400 technical reference manual.

Note that for efficient tracing bandwidth, TRACECLK must run as fast as possible while maintaining good signal integrity on all parallel trace signals. This is dependent on board and connector choices, GPIO strength settings (GPIO_OSPEEDR registers) and $V_{DD}$ voltage.
When using $V_{DD}$ = 1.8 V, a setting in the OTP bit and the register SYSCFG_IOCTRLSETR (HSLVEN_TRACE bit) is required to ensure the best speed on pads used on trace signals.

**Warning: HSLVEN_xxx must not be set when $V_{DD}$ is above 2.7 V otherwise permanent IC damage might occur.**

**Figure 20. Parallel trace port with JTAG/SWD on Mictor-38 implementation example**




## Hardware debug port

Some internal signal are available for deep debugging. Internal knowledge and an oscilloscope or logic analyzer are needed. For more information, refer to product reference manual and datasheet.

### 8.3.5 Debug triggers and LEDs

The CoreSight™ Cross-Trigger Interface (CTI) are available on pins as DBTRGI and DBTRGO.

DBTRGI is generated by external user signal and programmed inside CoreSight™ components to start/stop traces or enter specific core(s) in debug mode (break).

DBTRGO is generated by CTI to see externally that a trigger condition is reached by one of the CoreSight™ component (such as, core break, trace started).

DBTRGO can be available on PA13, PA14 or PG9.

DBTRGI can be available on PA13, PA14 or PA15.

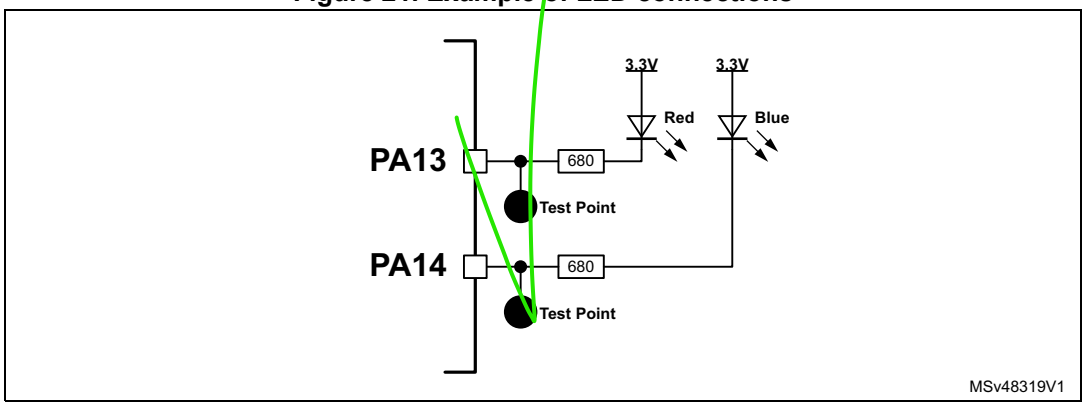
PA13 specific behavior (see boot documentation for details):

- During boot phase, in case of boot failure, the PA13 pin is set to low open-drain (that is the error LED lights bright).
- During UART/USB boot, the PA13 pin toggles open-drain at a rate of about 5 Hz until a connection is started (that is error LED blinks fast).
- With BOOT[2:0] = 0b100 (no boot, used for specific debug), PA13 toggles open-drain at a rate of about 5 kHz (that is error LED lights weak).
- In all other cases, the PA13 is kept in its reset value, that is high-z until software setting.

It is a good idea to put a red LED on PA13 as shown in *Figure 21*.

LEDs are useful for quick visual signaling of system activity. So, it is a good choice to use PA13 and PA14. This does not avoid usage of DBTRGI and DBTRGO on PA13 or PA14 for debug (assuming the software stops controlling LEDs during this specific debug).

**Figure 21. Example of LED connections**



# 9 Recommendations

## 9.1 Printed circuit board

For technical reasons, it is mandatory to use a multilayer printed circuit board (PCB) with a separate layer dedicated to ground ($V_{SS}$) and another layer dedicated for power supplies like the $V_{DD}$ and $V_{DDCORE}$. This provides good decoupling and a good shielding effect.

## 9.2 Component position

A preliminary layout of the PCB must separate the different circuits according to their EMI contribution to reduce cross-coupling on the PCB, that is noisy, high-current circuits, low-voltage circuits, and digital components.

## 9.3 Ground and power supply ($V_{SSx}$, $V_{DDx}$)

Due to large power and high frequencies involved in STM32MP15x lines, it is mandatory to use at least 4 layers PCB with dedicated power planes for $V_{SSx}$ and $V_{DDx}$.

## 9.4 I/O speed settings

It is important to set the right output drive on I/Os to have sufficient rise and fall time, as well as to avoid additional ringing and noise.

When there is no specific requirements for I/O speed, it is mandatory to set OSPEEDR to 0.

As a first approximation, the following drawing and tables permits to quickly choose the right setting to apply according to signal frequency and capacitive load. This setting needs to be tailored in case of signal integrity issue.

In most cases, I/O compensation needs to be enabled in SYSCFG. Refer to product datasheet for more details.

*Note: In case of asynchronous or single edge clocked data lanes (such as SDR), the maximum data frequency toggle is effectively half the data rate. For example an SPI running at 10 Mbits/s has a maximum frequency of 5 MHz on data signal (for example output serial data 01010101...), while10 MHz on the clock signal. On dual edge clocked data lanes (such as DDR), the clock and data have same maximum toggling frequency.*

*Note: The HSLVEN_xxx bits are not taken into account if the OTP bit PRODUCT_BELOW_2V5 =0 (default state).*

*Note: Setting HSLVEN_xxx=1 and product_below_2V5=1 while VDD > 2.7V can damage the IC.*

**Figure 22. I/O speed summary with various loads and voltages**

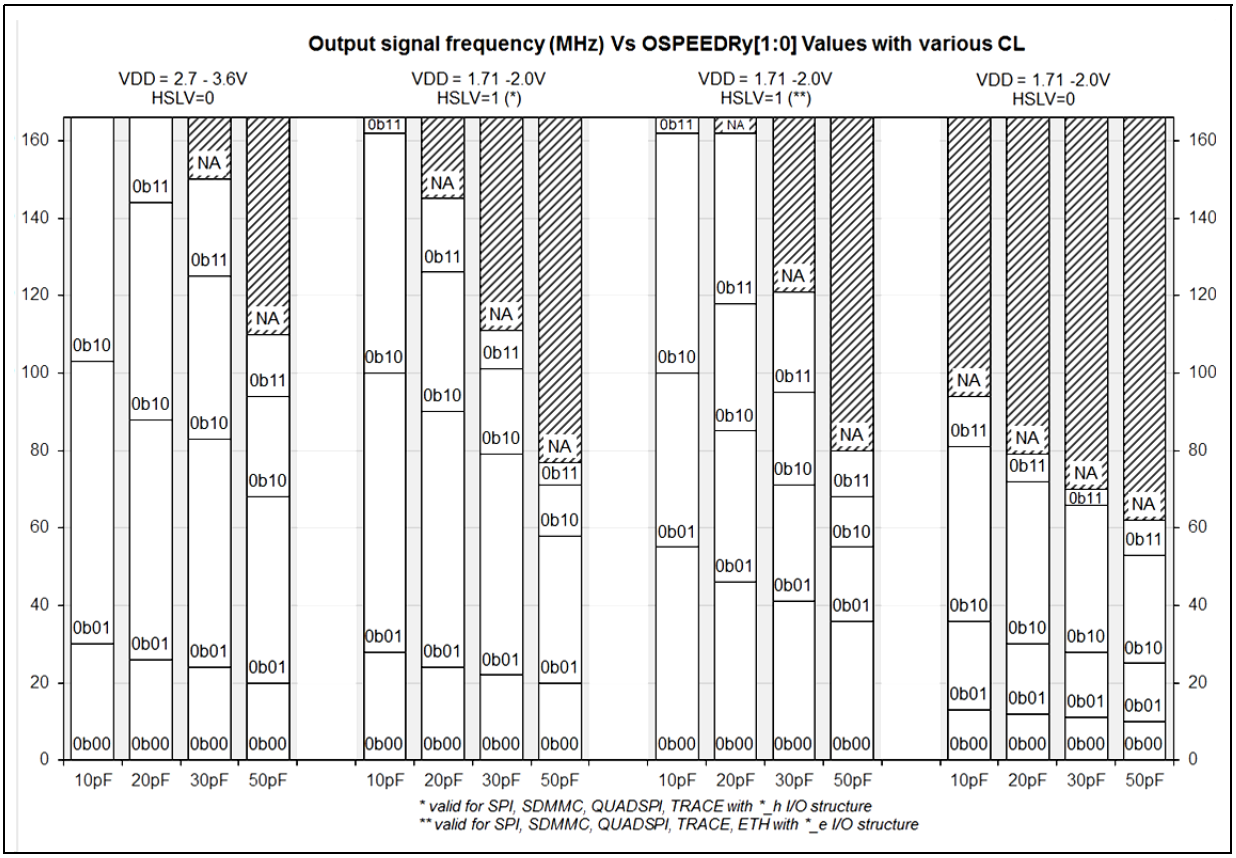



**Table 14. OSPEEDR setting example for VDD = 3.3 V typical**

| Peripheral | Signals | Toggling rate (MHz) | OSPEEDR CL=30 pF | | OSPEEDR CL=10 pF | |
|---|---|---|---|---|---|---|
| FMC async | Data/Controls | 50 | 1 | Medium speed | 1 | Medium speed |
| FMC sync | CLK | 100 | 2 | High speed | 1 | Medium speed |
| | Data/Controls | 50 | 1 | Medium speed | 1 | Medium speed |
| QUADSPI (SDR) | CLK | 133 | 2 | High speed(1) | 2 | High speed |
| | Data/Controls | 66.5 | 1 | Medium speed | 1 | Medium speed |
| QUADSPI (DDR) | All | 66.5 | 1 | Medium speed | 1 | Medium speed |
| LTDC (HDMI)(2) | CLK | 74.25 | 1 | Medium speed | 1 | Medium speed |
| | Data/Controls | 37.125 | 1 | Medium speed | 1 | Medium speed |
| LTDC(2) | CLK | 90 | 2 | High speed | 1 | Medium speed |
| | Data/Controls | 45 | 1 | Medium speed | 1 | Medium speed |
| LTDC | CLK | 48 | 1 | Medium speed | 1 | Medium speed |
| | Data/Controls | 24 | 0 | Low speed | 0 | Low speed |
| TIM/LPTIM | All | 5 | 0 | Low speed | 0 | Low speed |

**Table 14. OSPEEDR setting example for VDD = 3.3 V typical (continued)**

| Peripheral | Signals | Toggling rate (MHz) | OSPEEDR CL=30 pF | | OSPEEDR CL=10 pF | |
|---|---|---|---|---|---|---|
| I2C | All | 1 | 0 | Low speed | 0 | Low speed |
| USART | All | 5 | 0 | Low speed | 0 | Low speed |
| SPI | CLK | 50 | 1 | Medium speed | 1 | Medium speed |
| | Data/Controls | 25 | 1 | Medium speed | 0 | Low speed |
| SAI | MCLK | 15 | 0 | Low speed | 0 | Low speed |
| | CLK | 1 | 0 | Low speed | 0 | Low speed |
| | Data/Controls | 0.5 | 0 | Low speed | 0 | Low speed |
| MDIOS | All | 5 | 0 | Low speed | 0 | Low speed |
| SDMMC (SDR) | CLK | 133 | 2 | High speed(1) | 2 | High speed |
| | Data/Controls | 66.5 | 1 | Medium speed | 1 | Medium speed |
| SDMMC (DDR) | All | 52 | 1 | Medium speed | 1 | Medium speed |
| FDCAN | All | 5 | 0 | Low speed | 0 | Low speed |
| ETH (MII) | CLK | 50 | 1 | Medium speed | 1 | Medium speed |
| | Data/Controls | 25 | 1 | Medium speed | 0 | Low speed |
| ETH (RMII) | All | 50 | 1 | Medium speed | 1 | Medium speed |
| ETH (GMII) | CLK | 125 | 2 | High speed | 2 | High speed |
| | Data/Controls | 62.5 | 1 | Medium speed | 1 | Medium speed |
| ETH (RGMII) | All | 125 | 2 | High speed | 2 | High speed |
| ETH (MDIO) | MDIO | 2.5 | 0 | Low speed | 0 | Low speed |
| TRACE | All | 133 | 3 | Very high speed | 2 | High speed |
| | | 100 | 2 | High speed | 1 | Medium speed |

1. Value for CL=20 pF.
2. Requires external oscillator for HSE.

**Table 15. OSPEEDR setting example for VDD = 1.8 V typical.(1)**

| Peripheral | Signals | Toggling rate (MHz) | OSPEEDR CL=30 pF | | OSPEEDR CL=10 pF | |
|---|---|---|---|---|---|---|
| FMC async | Data/Controls | 50 | 2 | High speed | 2 | High speed |
| FMC sync | CLK | 69 | 3 | Very high speed | 3 | Very high speed |
| | Data/Controls | 34.5 | 2 | High speed | 1 | Medium speed |
| QUADSPI (SDR)(2) | CLK | 133 | 3 | Very high speed(3) | 2 | High speed |
| | Data/Controls | 66.5 | 1 | Medium speed | 1 | Medium speed |
| QUADSPI (DDR)(2) | All | 66.5 | 1 | Medium speed | 1 | Medium speed |
| LTDC (HDMI) | CLK | 74.25 | 3 | Very high speed(3) | 3 | Very high speed |
| | Data/Controls | 37.125 | 2 | High speed | 2 | High speed |

**Table 15. OSPEEDR setting example for VDD = 1.8 V typical.(1) (continued)**

| Peripheral | Signals | Toggling rate (MHz) | OSPEEDR CL=30 pF | | OSPEEDR CL=10 pF | |
|---|---|---|---|---|---|---|
| LTDC | CLK | 69 | 3 | Very high speed | 3 | Very high speed |
| | Data/Controls | 34.5 | 2 | High speed | 1 | Medium speed |
| TIM/LPTIM | All | 5 | 0 | Low speed | 0 | Low speed |
| I2C | All | 1 | 0 | Low speed | 0 | Low speed |
| USART | All | 5 | 0 | Low speed | 0 | Low speed |
| SPI(4) | CLK | 50 | 1 | Medium speed | 1 | Medium speed |
| | Data/Controls | 25 | 1 | Medium speed | 0 | Low speed |
| SAI | MCLK | 15 | 1 | Medium speed | 1 | Medium speed |
| | CLK | 1 | 0 | Low speed | 0 | Low speed |
| | Data/Controls | 0.5 | 0 | Low speed | 0 | Low speed |
| MDIOS | All | 5 | 0 | Low speed | 0 | Low speed |
| SDMMC (SDR)(5) | CLK | 133 | 3 | Very high speed(3) | 2 | High speed |
| | Data/Controls | 66.5 | 1 | Medium speed | 1 | Medium speed |
| SDMMC (DDR)(5) | All | 52 | 1 | Medium speed | 1 | Medium speed |
| FDCAN | All | 5 | 0 | Low speed | 0 | Low speed |
| ETH (MII)(6) | CLK | 50 | 1 | Medium speed | 0 | Low speed |
| | Data/Controls | 25 | 0 | Low speed | 0 | Low speed |
| ETH (RMII)(6) | All | 50 | 1 | Medium speed | 0 | Low speed |
| ETH (GMII)(6) | CLK | 125 | 3 | Very high speed(3) | 2 | High speed |
| | Data/Controls | 62.5 | 1 | Medium speed | 1 | Medium speed |
| ETH (RGMII)(6) | All | 125 | 3 | Very high speed(3) | 2 | High speed |
| ETH (MDIO) | MDIO | 2.5 | 0 | Low speed | 0 | Low speed |
| TRACE(7) | All | 133 | 3 | Very high speed(3) | 2 | High speed |
| | | 100 | 2 | High speed | 1 | Medium speed |

1. HSLVEN_xxx=1 are only taken into account if OTP bit PRODUCT_BELOW_2V5 is set.
2. HSLVEN_QUADSPI=1.
3. Value for CL=20pF.
4. HSLVEN_SPI=1.
5. HSLVEN_SDMMC=1.
6. HSLVEN_ETH=1.
7. HSLVEN_TRACE=1.

## 9.5 PCB stack and technology

A trade off between the PCB cost and easy electrical connections has to be made. Below examples are either for 4 or 6 layers PCB with only PTH (suited for 0.8mm pitch package) or 4 layers PCB with both PTH and laser drilled vias (suited for 0.5mm pitch package).

Note that some STM32MP15x lines packages with outer ball pitch of 0.5 mm provide power improved center ball matrix with a pitch of 0.65 mm to allow large PTH via in between balls. This ensures better supply connection as well as optimized thermal conductivity than small buried laser drilled vias.

**Figure 23. 6 layer PCB stack example**

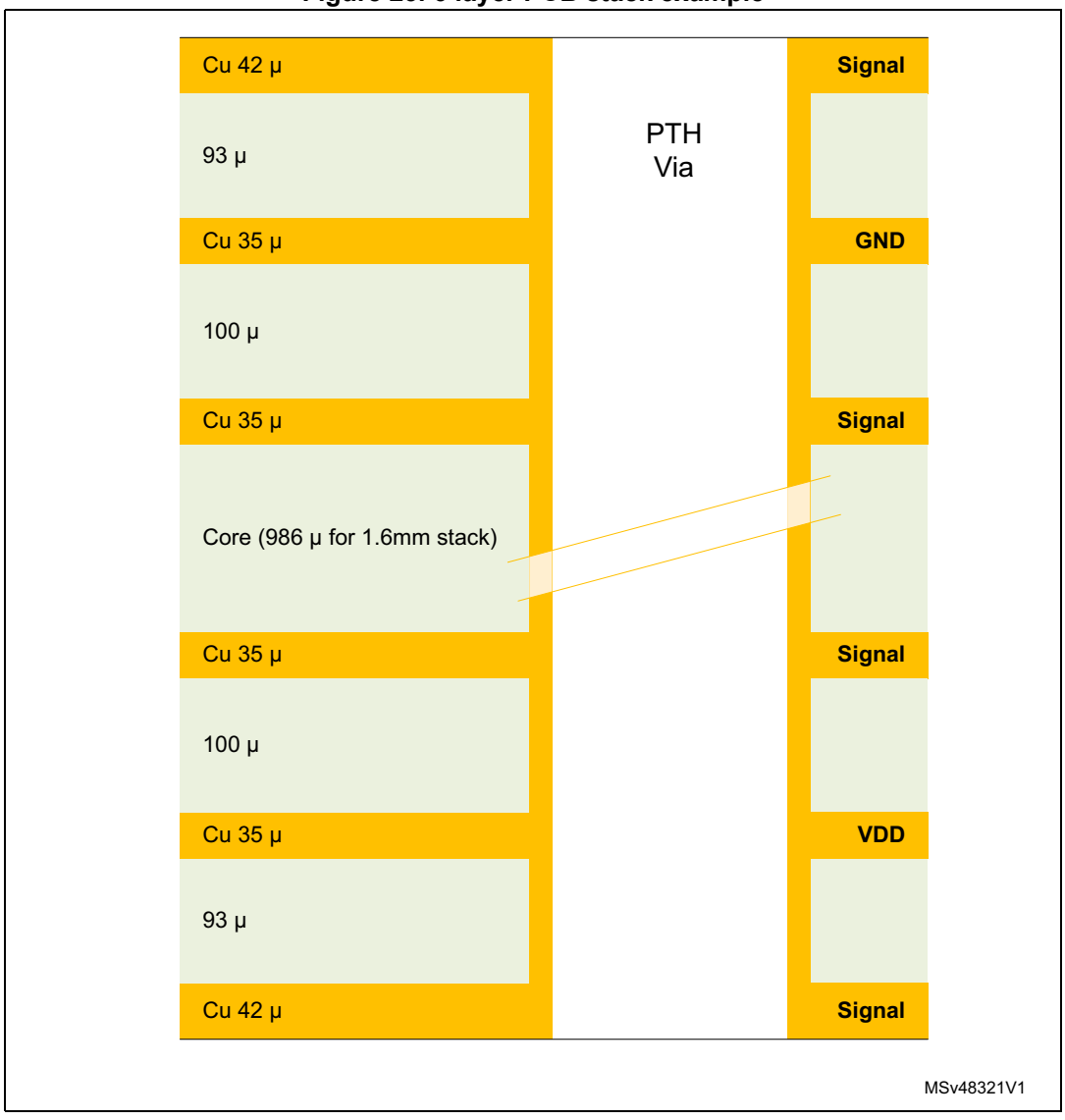


**Figure 24. 4 layer PCB stack example**

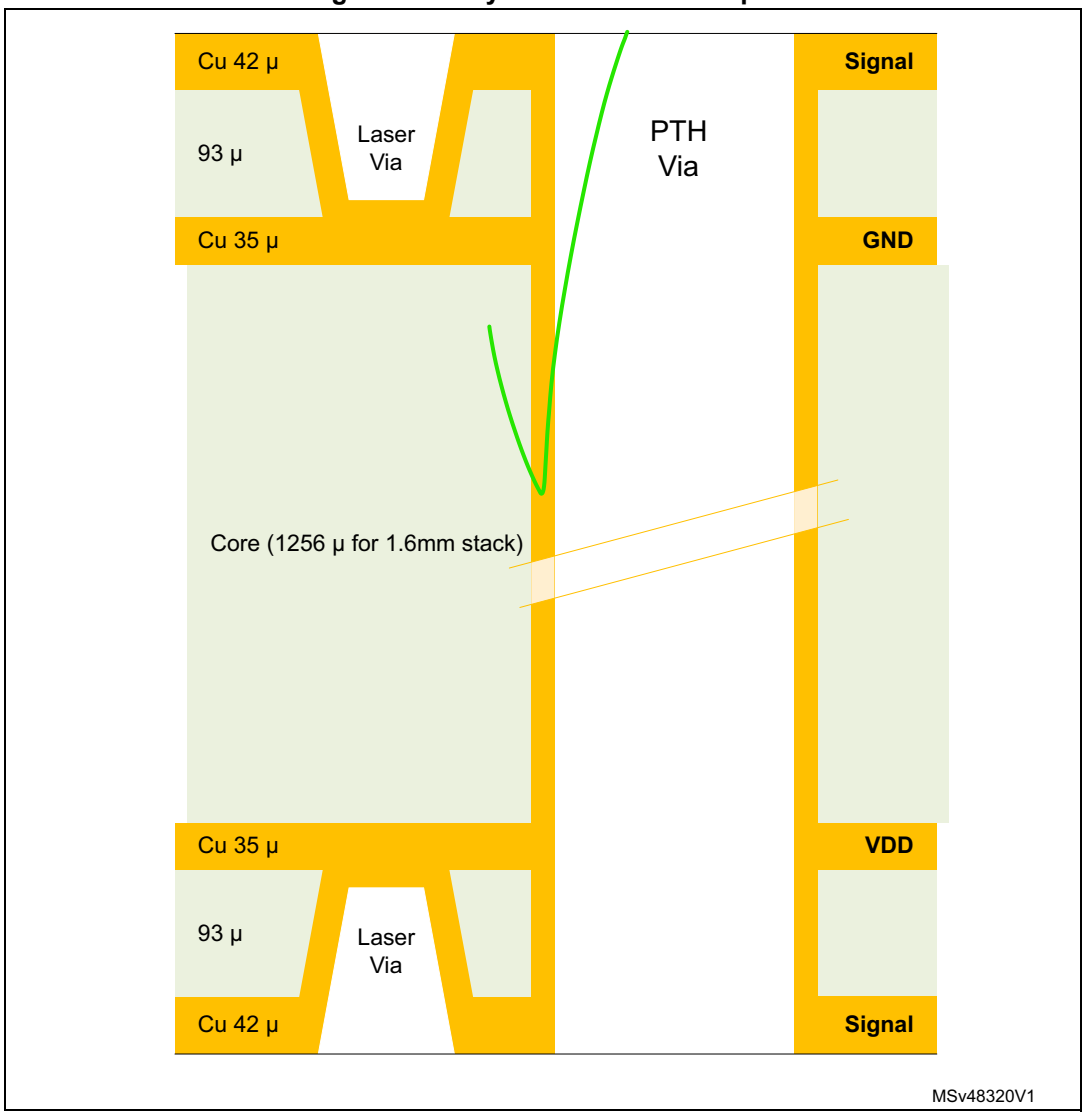


**Figure 25. PCB rule example for 0.8 mm pitch package**

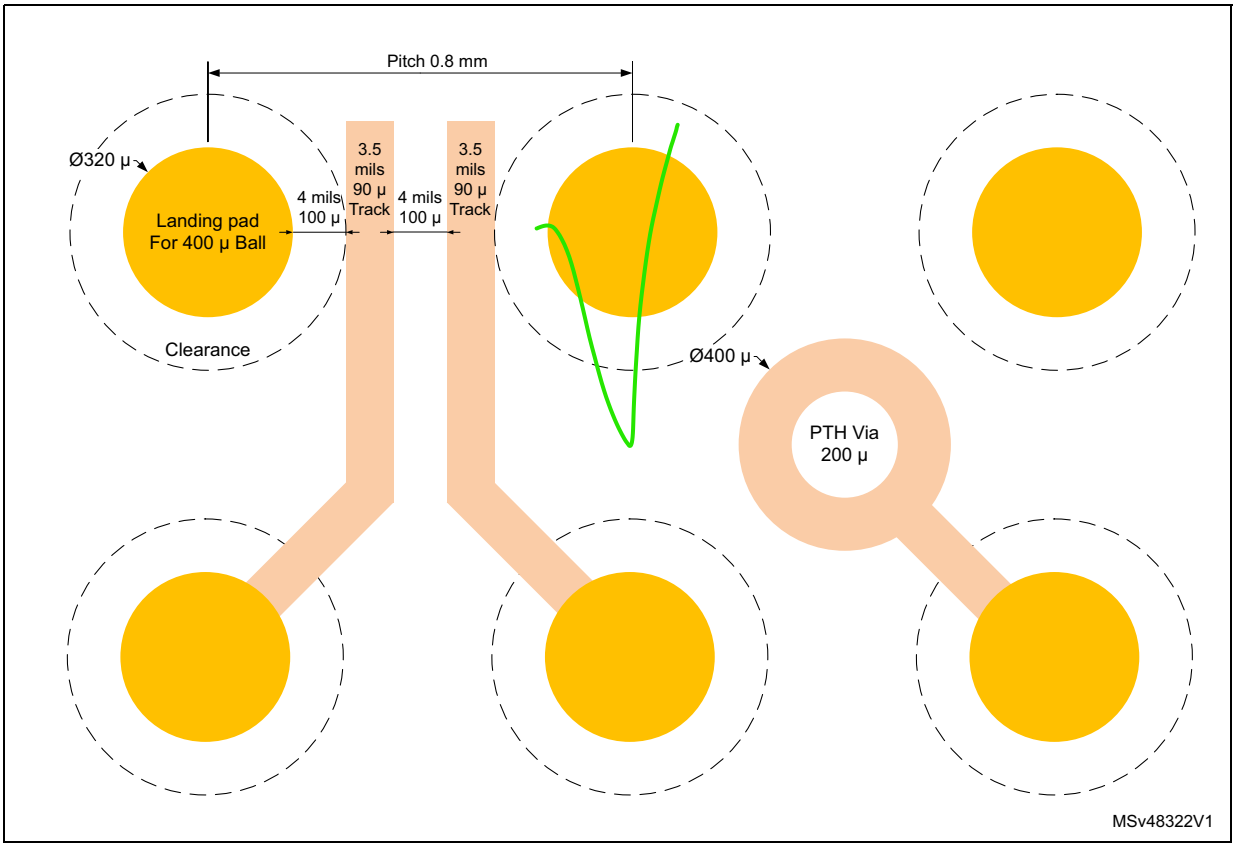


**Figure 26. PCB rule example for 0.5 mm pitch package**

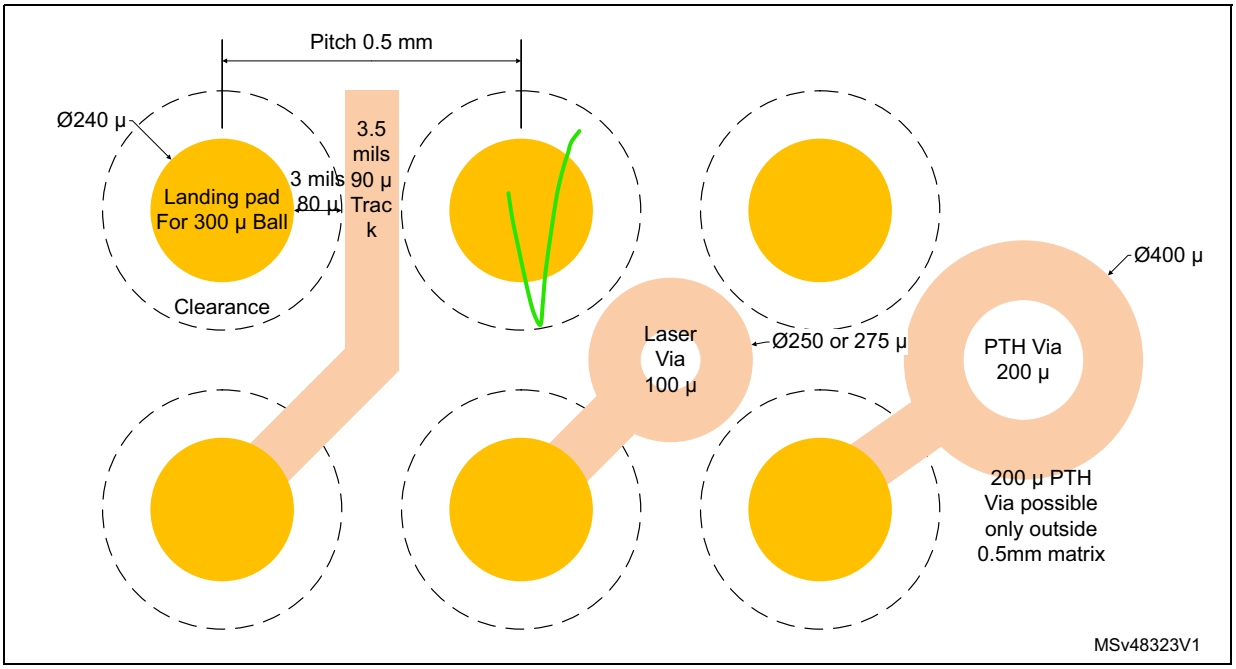
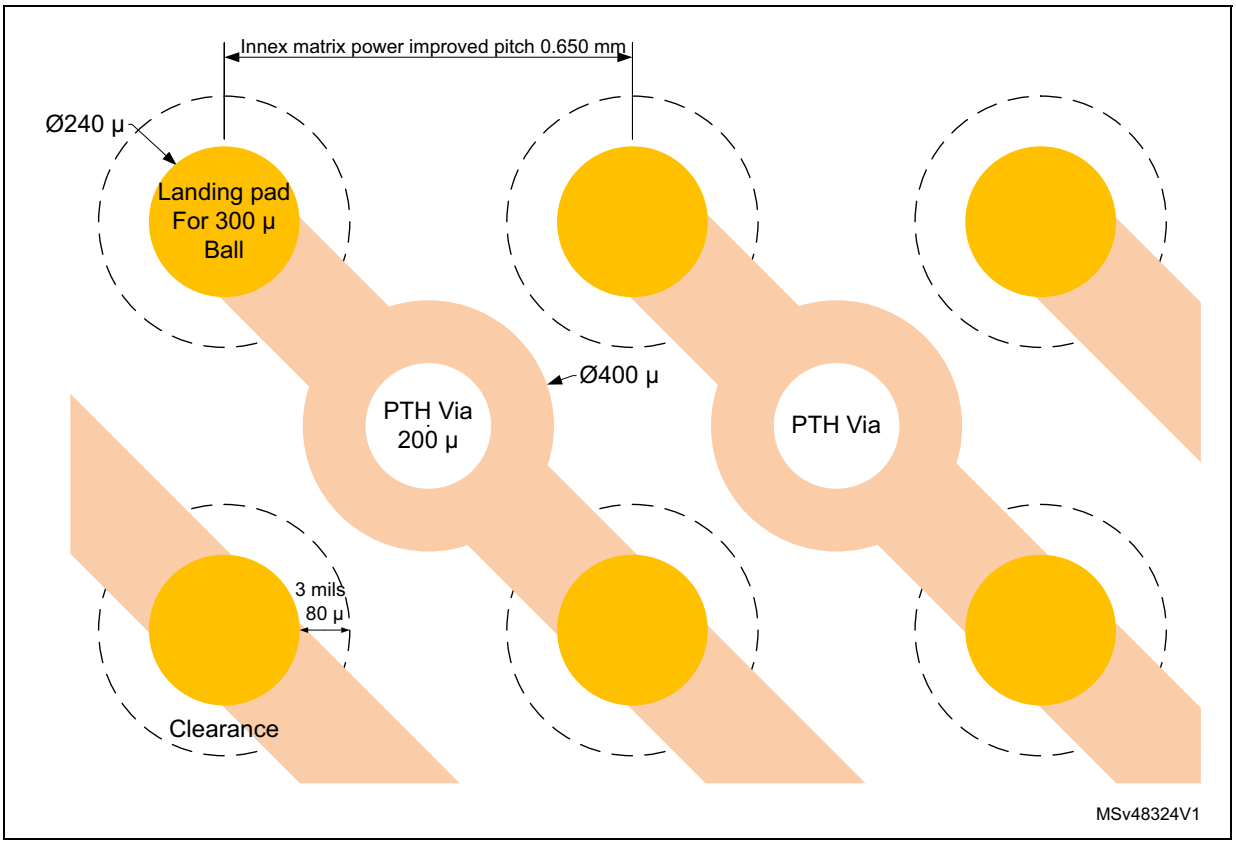



**Figure 27. PCB rule example for inner balls with 0.65mm power improved pitch**

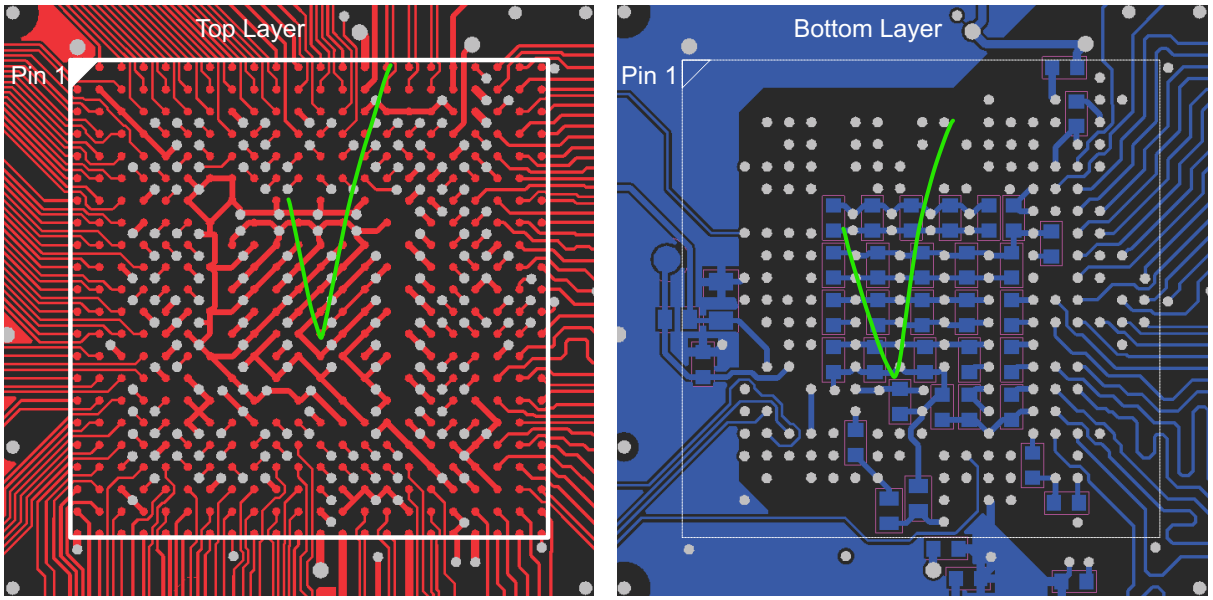


## 9.6 Decoupling

All the power supply and ground pins must be properly connected to the power supplies. These connections, including pads, tracks and vias must have as low impedance as possible. This is typically achieved with thick track widths and, preferably, the use of dedicated power supply planes in multilayer PCBs.

In addition, each power supply pair must be decoupled with ceramic capacitors (most of the time 100 nF or 1 µF, see *Table 4*). These capacitors need to be placed as close as possible to, or below, the appropriate pins on the underside of the PCB. Exact values depend on the application. *Figure 28* shows the typical layout of such a decoupling placement.

**Figure 28. Example of decoupling layout**




1. PTH via connecting supplies and decoupling capacitors to internal planes are visible in gray.

## 9.7 ESD/EMI protections

ElectroStatic Discharge (ESD) and ElectroMagnetic Interference (EMI) must be taken into account from the beginning of a product development as it can be very complex and expensive to add them later.

ESD and EMI are driven by global standards (such as IEC 61000, JESD 22) which in most countries require a certification to allow mandatory marking to be applied on a product (such as CE, FCC).

ESD and EMI are also driven by standardized interface certification or requirements (for example USB).

Although the STM32MP15x lines embed device level ESD protection, the final product protection must be done by external components, more especially on interfaces having external user access in the final product (such as Ethernet, USB, SD-card).

Some components provide ESD protection as well as EMI common mode filtering (for example ECMF02-2AMX6 used on USB).

Some examples of ESD/EMI protections are provided in *Section 10: Reference design examples*.

For more details, refer to *EMC design guide for ST microcontrollers* application note (AN1709).

## 9.8 Sensitive signals

When designing an application, the ElectroMagnetic Compatibility (EMC) performance can be improved by closely studying:

- Signals for which a temporary disturbance affects the running process permanently (the case of interrupts and handshaking strobe signals, and not the case for LED commands).
  For these signals, a surrounding ground trace, shorter lengths and the absence of noisy and sensitive traces nearby (crosstalk effect) improve the EMC performance.
  For digital signals, the best possible electrical margin must be reached for the two logical states and slow Schmitt triggers are recommended to eliminate parasitic states.
- Noisy signals such as, clock.
- Sensitive signals such as, high impedance.

For more details, refer to *EMC design guide for ST microcontrollers* application (AN1709).

## 9.9 Unused I/Os and features

The STM32MP15x lines are designed for a wide range of applications and often a particular application does not use 100% of the resources.

To increase the EMC performance, unused clocks, counters or I/Os, must not be left free, for example I/Os must be set to 0 or 1 (pull-up or pull-down to the unused I/O pins) and unused features should be “frozen” or disabled (see*Table 5*).

# 10 Reference design examples

## 10.1 Description

The following sections are example to help the user to connect major and critical interfaces to the STM32MP15x lines.

### 10.1.1 Clock

Two clock sources are used for STM32MP15x lines, with the following choice:

- LSE: 32.768 kHz crystal for the embedded RTC
- HSE: 24 MHz crystal or external oscillator as STM32MP15x lines main clock

Refer to *Section 6: Clocks on page 29*.

**Figure 29. HSE recommended schematics for both oscillator/crystal options**

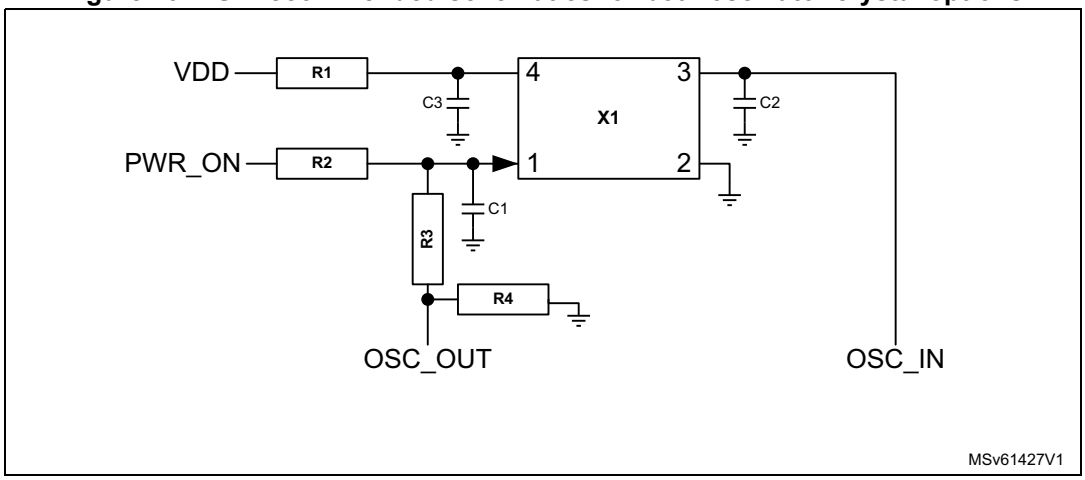



**Table 16. HSE BOM for oscillator or crystal**

| - | Oscillator | Crystal |
|---|---|---|
| X1 | NZ2016SH 24 MHz | NX2016SA 24 MHz |
| R1 | 10 ohms | - |
| R2 | 10 Kohms | - |
| R3 | - | 0 ohm |
| R4 | 1Kohm | - |
| C1 | - | 6.8 pF |
| C2 | - | 6.8 pF |
| C3 | 10 nF | - |

### 10.1.2 Reset

The NRST reset signal in *Figure 4* is active low. The reset sources include:

- Reset button
- Debugging tools via the JTAG connector

Refer to *Section : on page 17*.

### 10.1.3 Boot mode

The boot option is configured by setting permanent wires or switches SW3 (BOOT2), SW2 (BOOT1) and SW1 (BOOT0) and internal OTP. Refer to *Section 7: Boot configuration on page 33*.

In case of the UART boot using one of the possible U(S)ARTx_RX pins, (refer to *STM32MP1 Series wiki*), to avoid a floating signal sent to the host, until the initialization character is received and decoded by the BootROM, it is required to have a 10 kOhm $V_{DD}$ pull-up on the respective U(S)ARTx_TX pin.

**Table 17. UART possible boot pins**

| Peripheral | Signal | Pin |
|---|---|---|
| USART2 | RX | PA3 |
| | TX | PA2 |
| USART3 | RX | PB12 |
| | TX | PB10 |
| UART4(1) | RX | PB2 |
| | TX | PG11 |
| UART5 | RX | PB5 |
| | TX | PB13 |
| USART6 | RX | PC7 |
| | TX | PC6 |
| UART7 | RX | PF6 |
| | TX | PF7 |
| UART8 | RX | PE0 |
| | TX | PE1 |

1. Recommended default UART for Linux console (that is as VCP on STLINK STDC14 connector).

### 10.1.4 SWD / JTAG interface

The reference design shows the connections between the STM32MP15x lines and some standard connector. Refer to *Section 8: Debug management on page 37*.

*Note: If available, it is recommended to connect the debugger probe system reset pin to NRST to reset the application from the debugger.*

### 10.1.5 Power supply

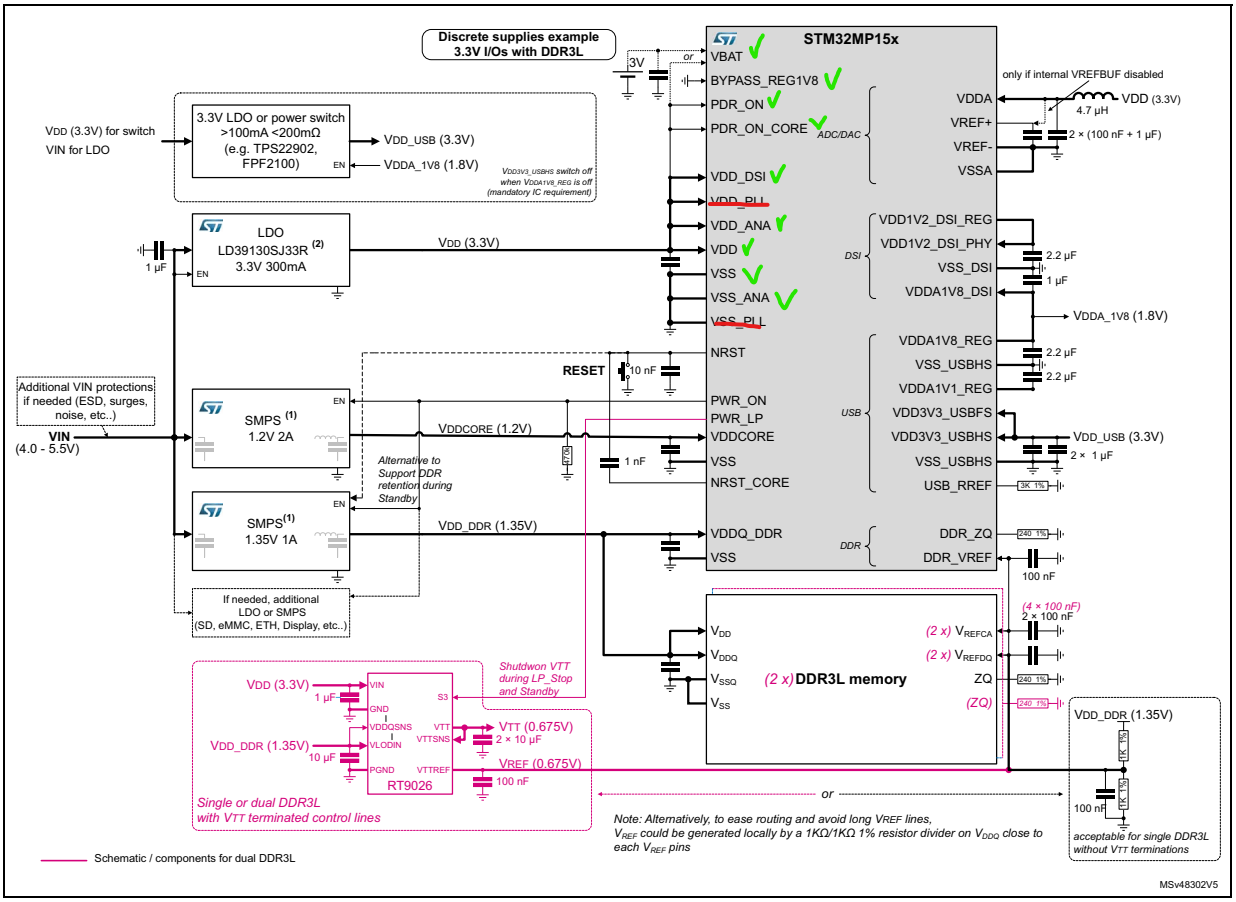
Refer to *Section 4: Power supplies on page 11*.

#### Discrete supplies example with 3.3 V I/Os with DDR3L

This reference design example targets a simple 3.3 V IOs platform with low cost DDR3L without emphasis on power reduction. The Sleep/Stop/Standby modes are supported. LP-Stop and low-power Standby with DDR3L retention can be supported while having little interest due to the use of DDR3L which has not a low-power target for self-refresh.

Refer also to STM32MP151, STM32MP153 and STM32MP157 discrete power supply hardware integration (AN5256).

**Figure 30. Discrete supplies example 3.3 V I/Os with DDR3L**

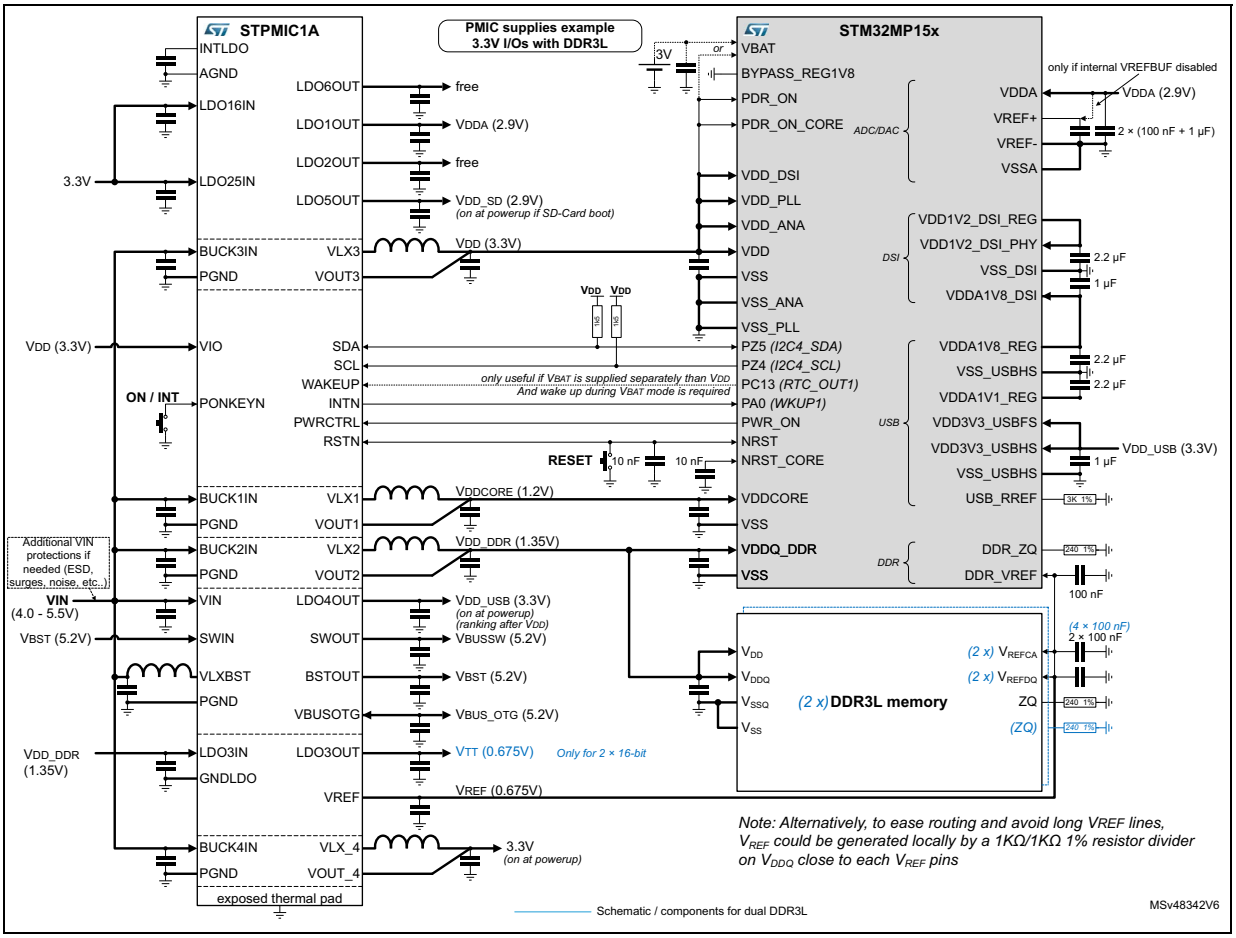



1. Additional SMPS components not shown.
2. Smaller NCP161AFCT330 can also be used.

#### PMIC supplies example 3.3 V I/Os with DDR3L

This reference design example targets a complex 3.3 V IOs platform with low cost DDR3L and high integration PMIC. Usually, all platform components are powered by the PMIC. Full-power supply control is supported thanks to PMIC I2C and side band signals. The Sleep/Stop/Standby modes are supported. See PMIC documentations for details of PMIC components.

**Figure 31. PMIC example 3.3 V I/Os with DDR3L**

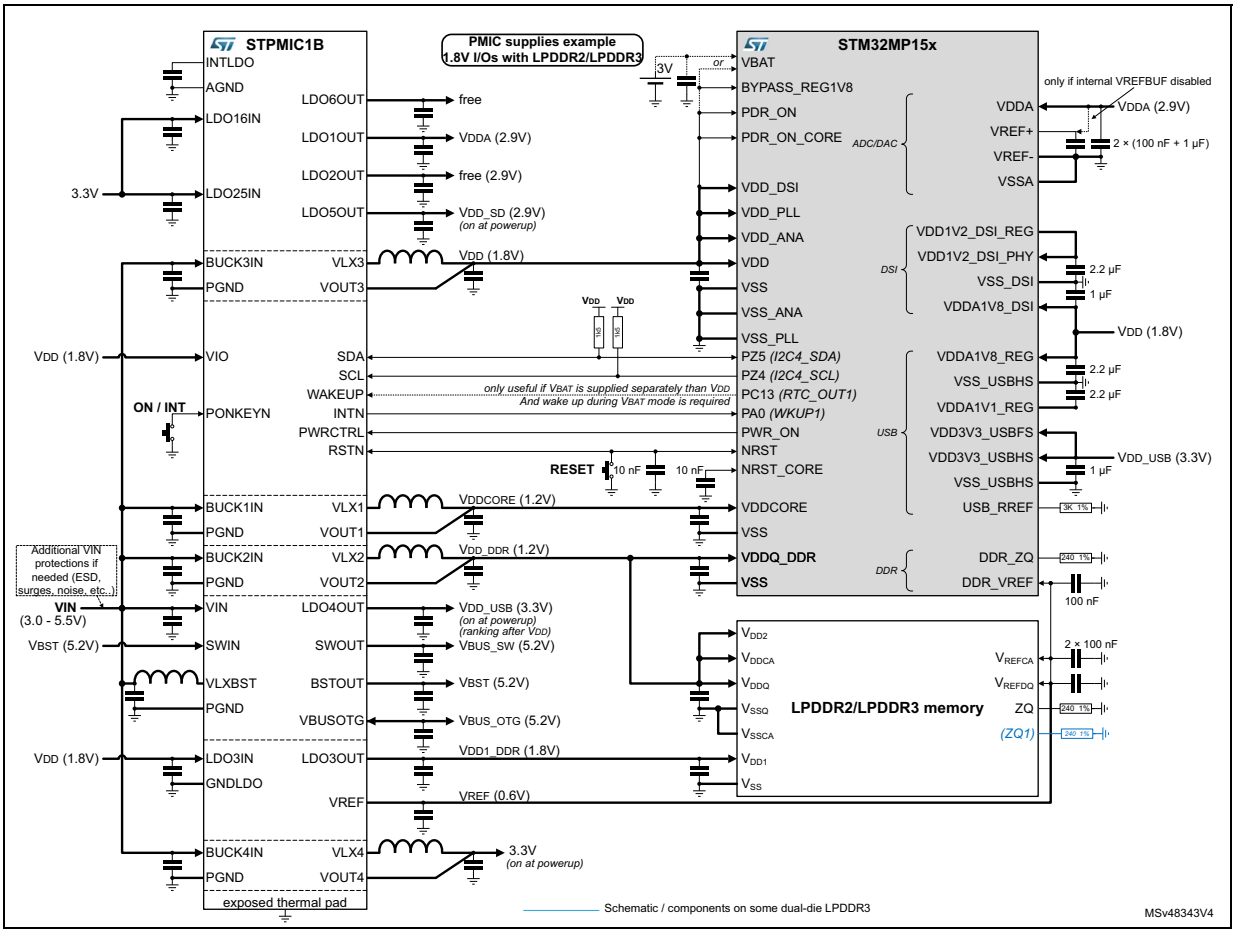



*Note: On a same I2C bus, it is not possible to share I2C devices controlled from both secure and non-secure SW. E.g. STPMIC1 is controlled by secure SW in our standard deliveries and usually belong to a distinct and securable I2C master (I2C4 or I2C6 ON STM32MP15x).*

### PMIC supplies example 1.8 V I/Os with LPDDR2/LPDDR3

This reference design example targets a complex 1.8 V IOs platform with low power LPDDR2/LPDDR3 and high integration PMIC. Usually, all platform components are powered by the PMIC. The full-power supply control is supported thanks to PMIC I2C and side band signals. The Sleep/Stop/Standby modes are supported as well as very low power Standby with LPDDR2/LPDDR3 retention. See PMIC documentations for details of PMIC components

**Figure 32. PMIC example 1.8 V I/Os with LPDDR2/LPDDR3**




*Note: On a same I2C bus, it is not possible to share I2C devices controlled from both secure and non-secure SW. E.g. STPMIC1 is controlled by secure SW in our standard deliveries and usually belong to a distinct and securable I2C master (I2C4 or I2C6 ON STM32MP15x).*

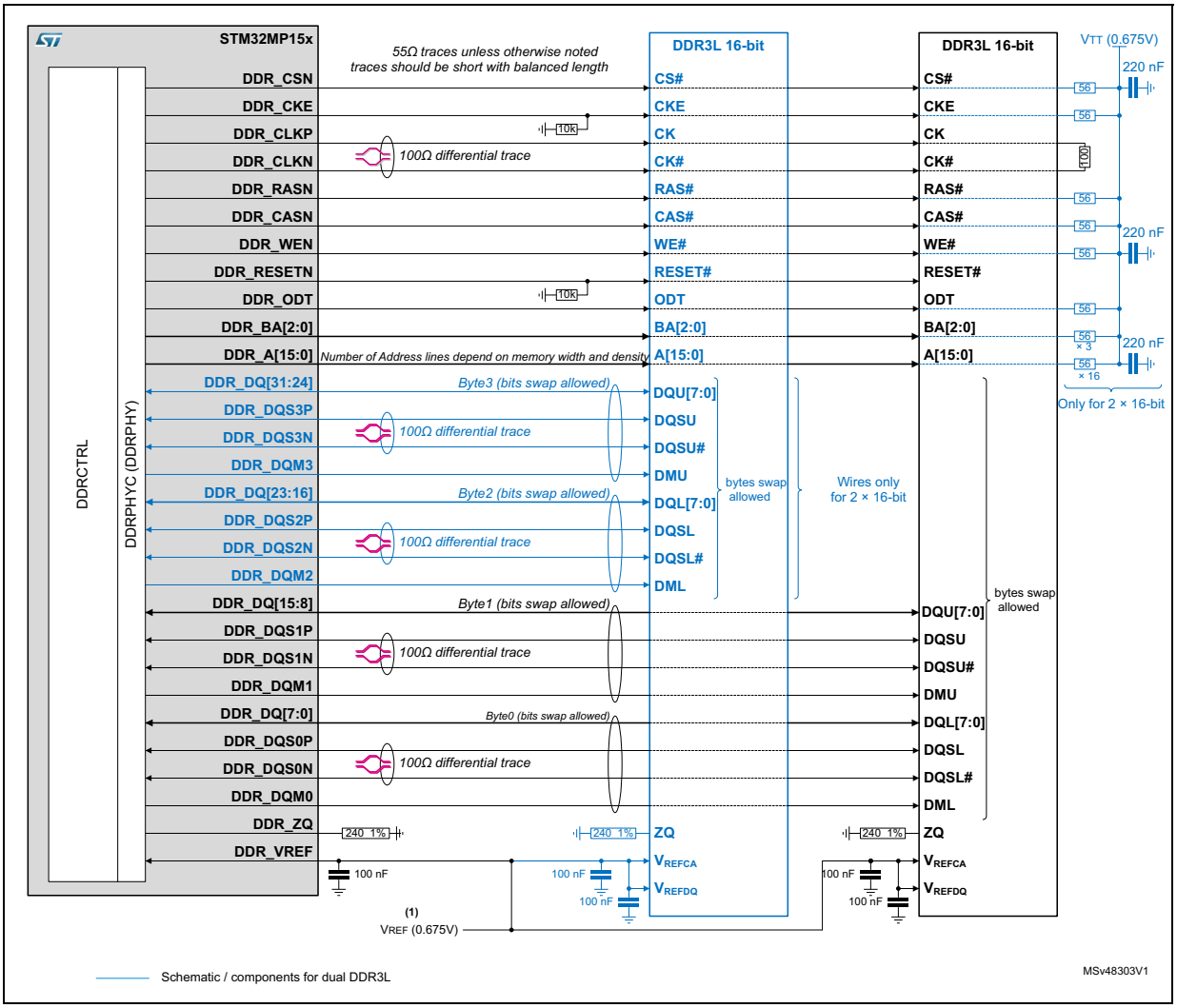
### 10.1.6 DDR3/DDR3L SDRAM

The DDR3 differs from DDR3L only by different supply voltage (1.5 V vs 1.35 V) and $V_{REF}$ level (0.75 V vs 0.675 V). DDR3L has superseded most DDR3 designs.

A 240 Ohm 1% resistor should be connected between DDR_ZQ and $V_{SS}$. This resistor must not be shared with ZQ resistors required on each DDR3/DDR3L components.

In case of 2x16-bits device, the impedance matching resistor network connected on termination voltage (VTT) supply should be placed as close as possible off the last device. *Fly-by* routing techniques must be used to avoid any impedance discontinuities. The values in the example below work in most cases, while it can be tailored to each side I/O drive strengths and PCB impedance.

**Figure 33. DDR3L 16/32 bits connection example**



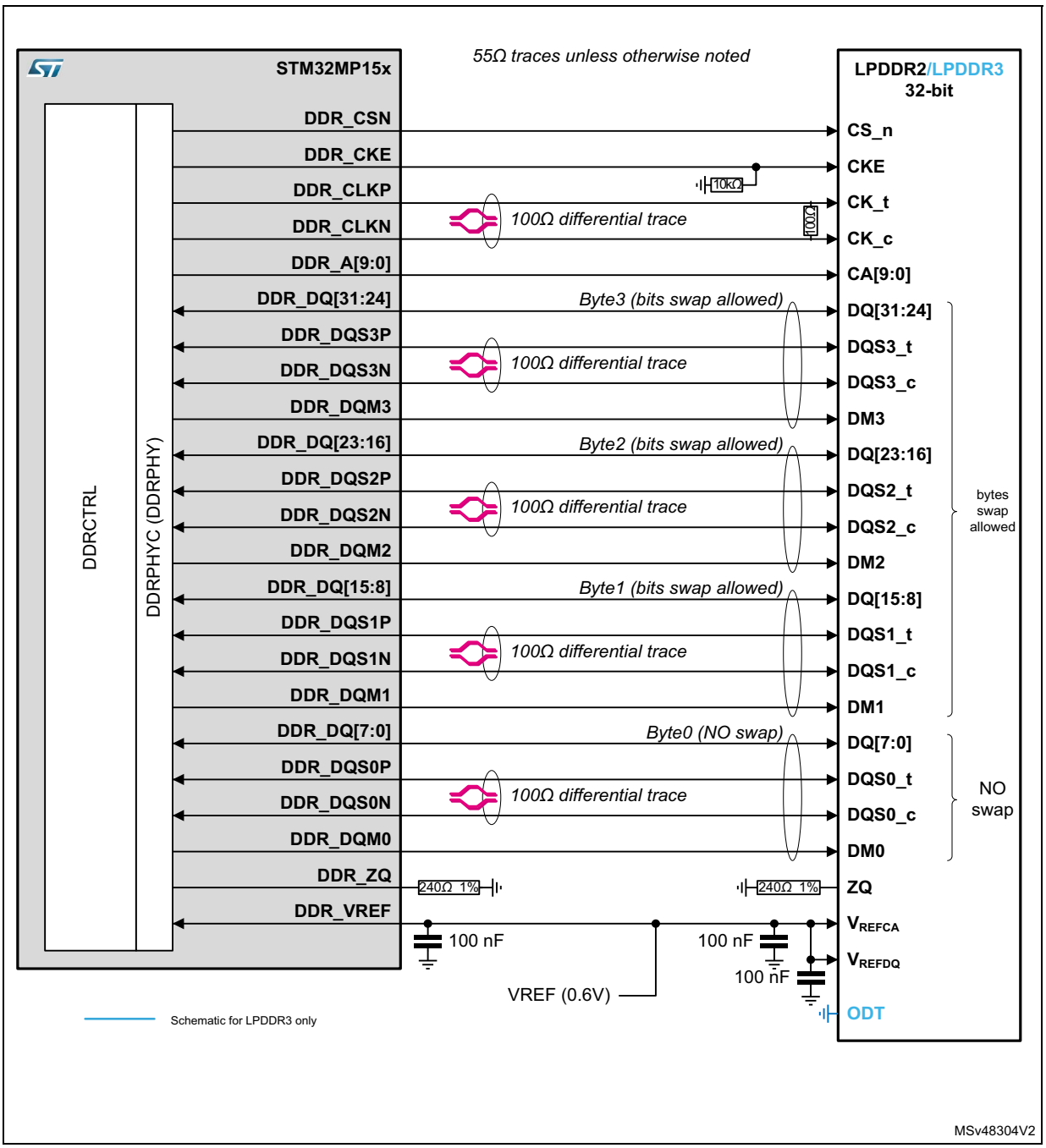

1. Alternatively, to ease routing and avoid long $V_{REF}$ lines, $V_{REF}$ can be generated locally by a 1KOhm/1KOhm 1% resistor divider on $V_{DDQ}$ close to each $V_{REF}$ pins.
2. Supplies and decoupling capacitors not shown.

Detailed routing examples are described in *STM32MP1 Series DDR memory routing guidelines* application note (AN5122).

### 10.1.7 LpDDR2/LpDDR3 SDRAM

A 240 Ohm 1% resistor should be connected between DDR_ZQ and $V_{SS}$. This resistor must not be shared with one or more ZQ resistors required on LPDDR2/LPDDR3 component.

**Figure 34. LPDDR2/LPDDR3 32-bits connection example**




1. Supplies and decoupling capacitors not shown.

Detailed routing examples are described in *STM32MP1 Series DDR memory routing guidelines* application note (AN5122).

### 10.1.8 SD card

#### External level shifter

It allows the use of UHS-I faster modes (up to SDR50 and DDR50, that is 50 MBytes/s bus speed) which need to switch to 1.8 V card I/Os voltage (SD-card is started with 3 V card I/Os).

*Note: As boot is always done in Standard mode (3 V IOs), if the card is used by the application in USH-I, a power cycle on card supply is required after Reset or Standby.*

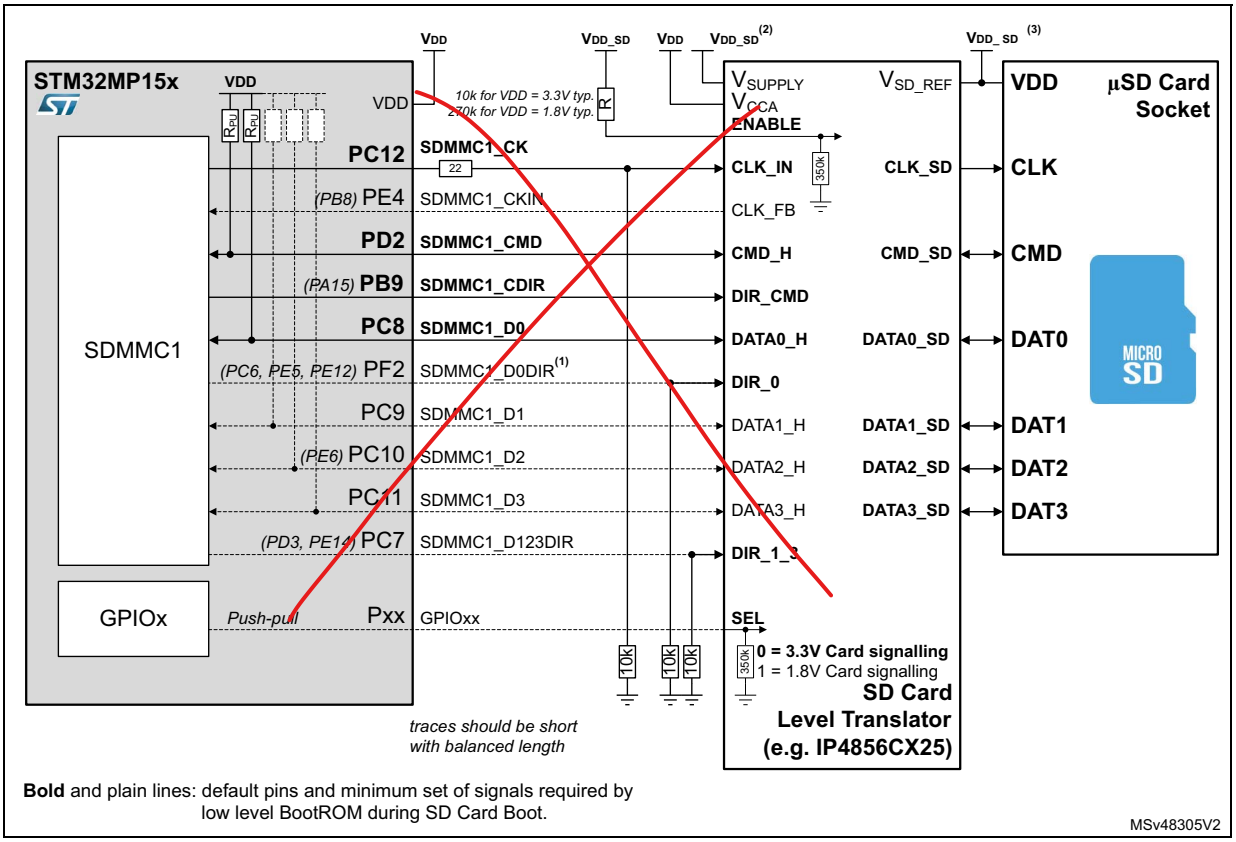
This example is independent of MPU I/O voltage $V_{DD}$ which is between 1.71 V and 3.6 V. In case of VDD at 1.8 V typical, an external level shifter is mandatory as all SD-Card start transactions in 'Standard' mode using 3 V signaling voltage.

Note that a good signal integrity is dependent on board, GPIO strength settings (GPIO_OSPEEDR registers) and $V_{DD}$ voltage.
When using $V_{DD}$ = 1.8 V, a setting in the OTP bit and the register SYSCFG_IOCTRLSETR (HSLVEN_SDMMC bit) is required to ensure the best speed on pads used on SDMMC outputs.

**Warning: HSLVEN_xxx must not be set when $V_{DD}$ is above 2.7 V otherwise permanent IC damage might occur.**

If needed, the impedance matching resistor must be placed as close as possible of the output driver pin. The values in the example below work in most cases, but can be tailored to I/O drive strengths and PCB impedance.

**Figure 35. SD-Card with external level shifter connection example**



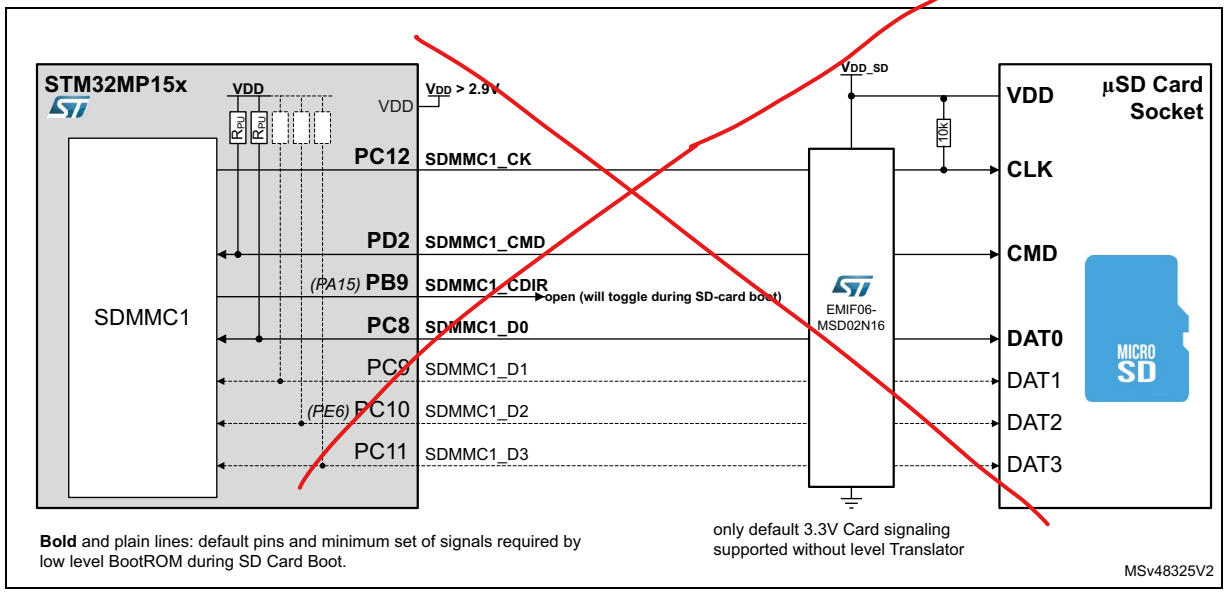

1. SDMMC1_D0DIR is not used during boot phase as only read data is requested from SD card DAT0. Nevertheless, SDMMC1_D0DIR pull-down is required to ensure correct DATA0_SD direction from card to MPU.
2. If used in USH-I, $V_{DD\_SD}$ must be cut for >1ms in to allow reboot (on Reset or Standby exit) use $V_{DD}$ if $V_{DD} > V_{DD\_SD}$.
3. If used in USH-I, $V_{DD\_SD}$ must be cut for >1ms in to allow reboot (on Reset or Standby exit).
4. Decoupling capacitors not shown.

Before $V_{DD\_SD}$ shutdown (for example before Standby), all signals going to card must be set to 0 or high-z by the SDMMC1 driver.

### Direct 3.3 V I/O voltage

It is the simpler interface which requires $V_{DD}$ > 2.9 V, limited to standard SD-Card speed (up to high-speed 25 MBytes/s bus speed). Due to high current required by the high-density SD-card, and to limit power during Standby, the $V_{DD\_SD}$ can be separated from $V_{DD}$, however the voltage level between them must be within 200 mV, except when $V_{DD\_SD}$ is cut to save power.

**Figure 36. SD-Card with 3.3 V I/Os connection example**



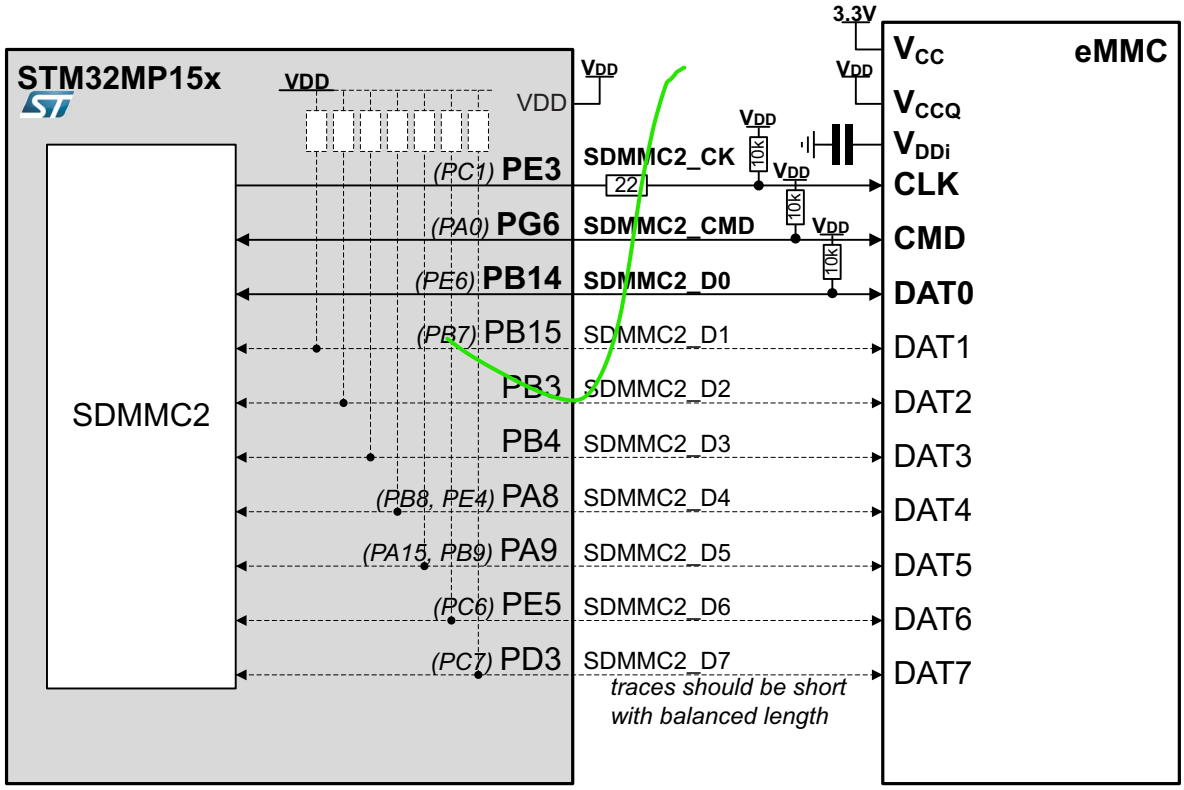

## 10.1.9 eMMC™ Flash

Note that a good signal integrity is dependent on board, GPIO strength settings (GPIO_OSPEEDR registers) and $V_{DD}$ voltage.
When using $V_{DD}$ = 1.8 V, a setting in the OTP bit and the register SYSCFG_IOCTRLSETR (HSLVEN_SDMMC bit) is required to ensure the best speed on pads used on SDMMC outputs.

**Warning: HSLVEN_xxx must not be set when $V_{DD}$ is above 2.7 V otherwise permanent IC damage might occur.**

If needed, the impedance matching resistor should be placed as close as possible of the output driver pin. The values in the example below work in most cases, however it can be tailored to I/O drive strengths and PCB impedance.

**Figure 37. eMMC™ connection example**



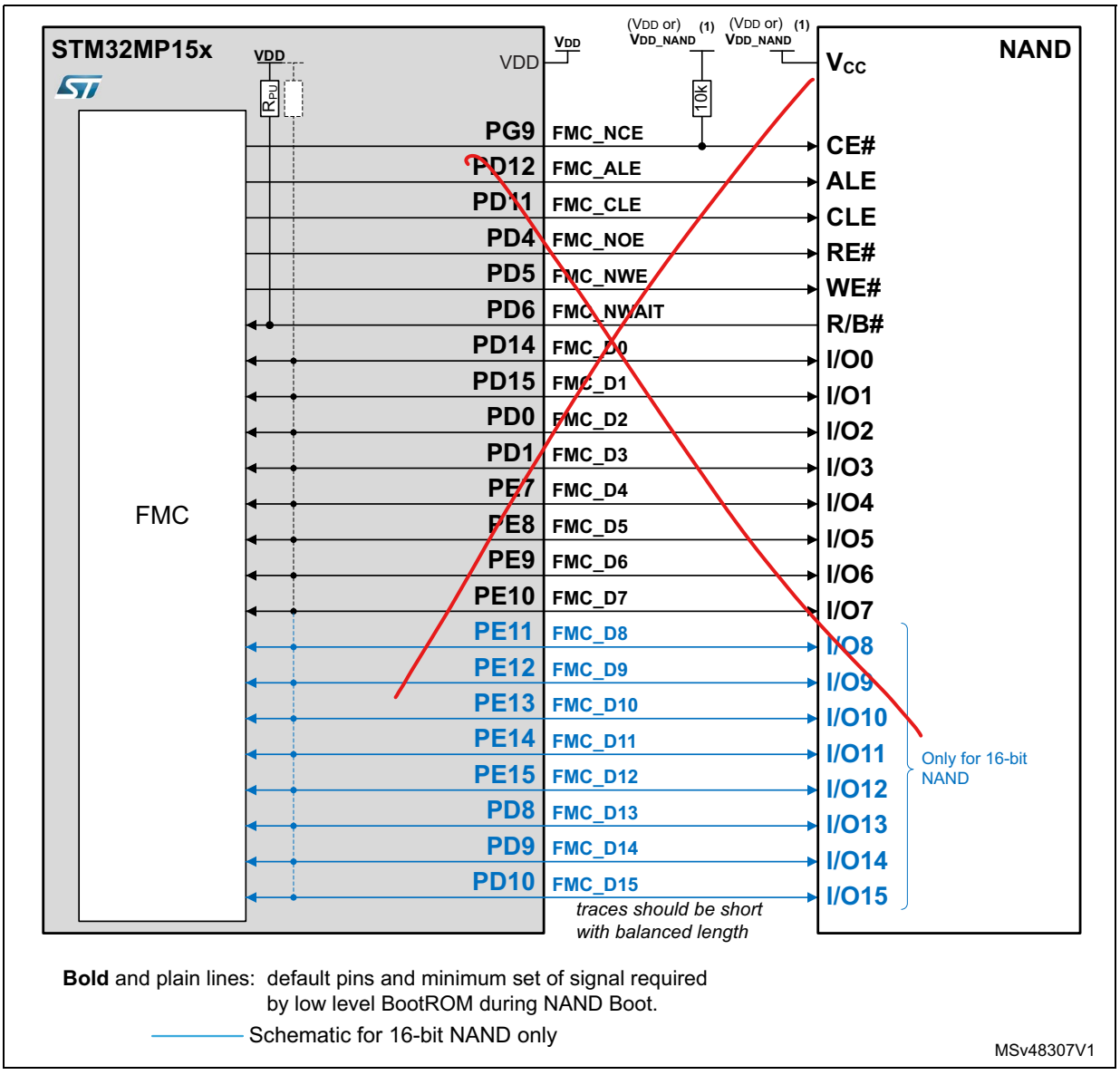

1. Decoupling capacitors not shown.

### 10.1.10 SLC NAND-Flash

The single 8 or 16-bit SLC NAND memory device (CE# = FMC_NCE) as well as two independent 8-bit SLC NAND memory devices (device1 CE# = FMC_NCE and device2 CE# = FMC_NCE2) are supported.

Note that boot is only done on the SLC NAND memory device connected to FMC_NCE.

**Figure 38. SLC NAND-Flash connection example**




1. $V_{DD\_NAND}$ must be cut for >1ms to allow reboot (on Reset or Standby exit).
2. Decoupling capacitors not shown.

*Note: Only single level cell (SLC) NAND-Flash is supported, with either Hamming, BCH4 or BCH8 error correction algorithms.*

### 10.1.11 Serial NOR-Flash/NAND-Flash

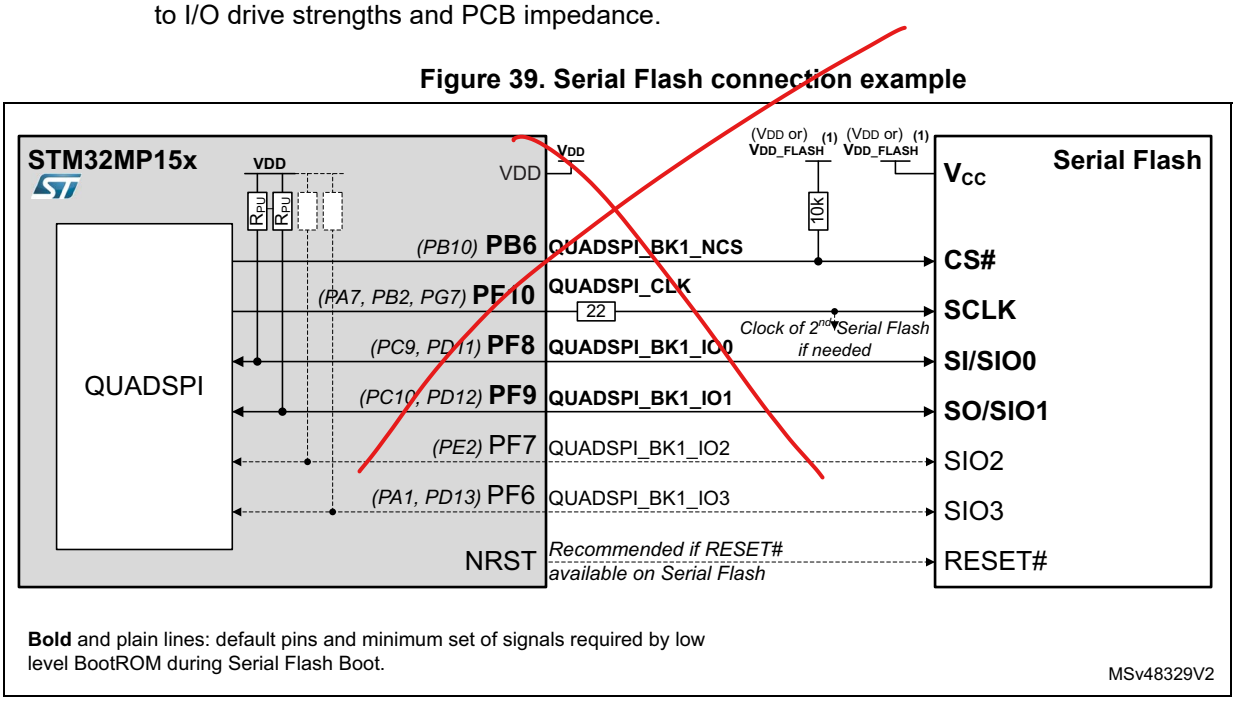
*Note: As boot is always done in SPI mode, if the Serial Flash is set by the application in multiple data lines or if sector addressing has been changed, a power cycle on Serial Flash supply is required after Reset or Standby exit.*

Note that a good signal integrity is dependent on board, GPIO strength settings (GPIO_OSPEEDR registers) and $V_{DD}$ voltage.
When using $V_{DD}$ = 1.8 V, a setting in the OTP bit and the register SYSCFG_IOCTRLSETR (HSLVEN_QUADSPI bit) is required to ensure the best speed on pads used on SDMMC outputs.

**Warning: HSLVEN_xxx must not be set when $V_{DD}$ is above 2.7 V otherwise permanent IC damage might occur.**

If needed, the impedance matching resistor should be placed as close as possible of the output driver pin. The values in the example below work in most cases, but can be tailored to I/O drive strengths and PCB impedance.

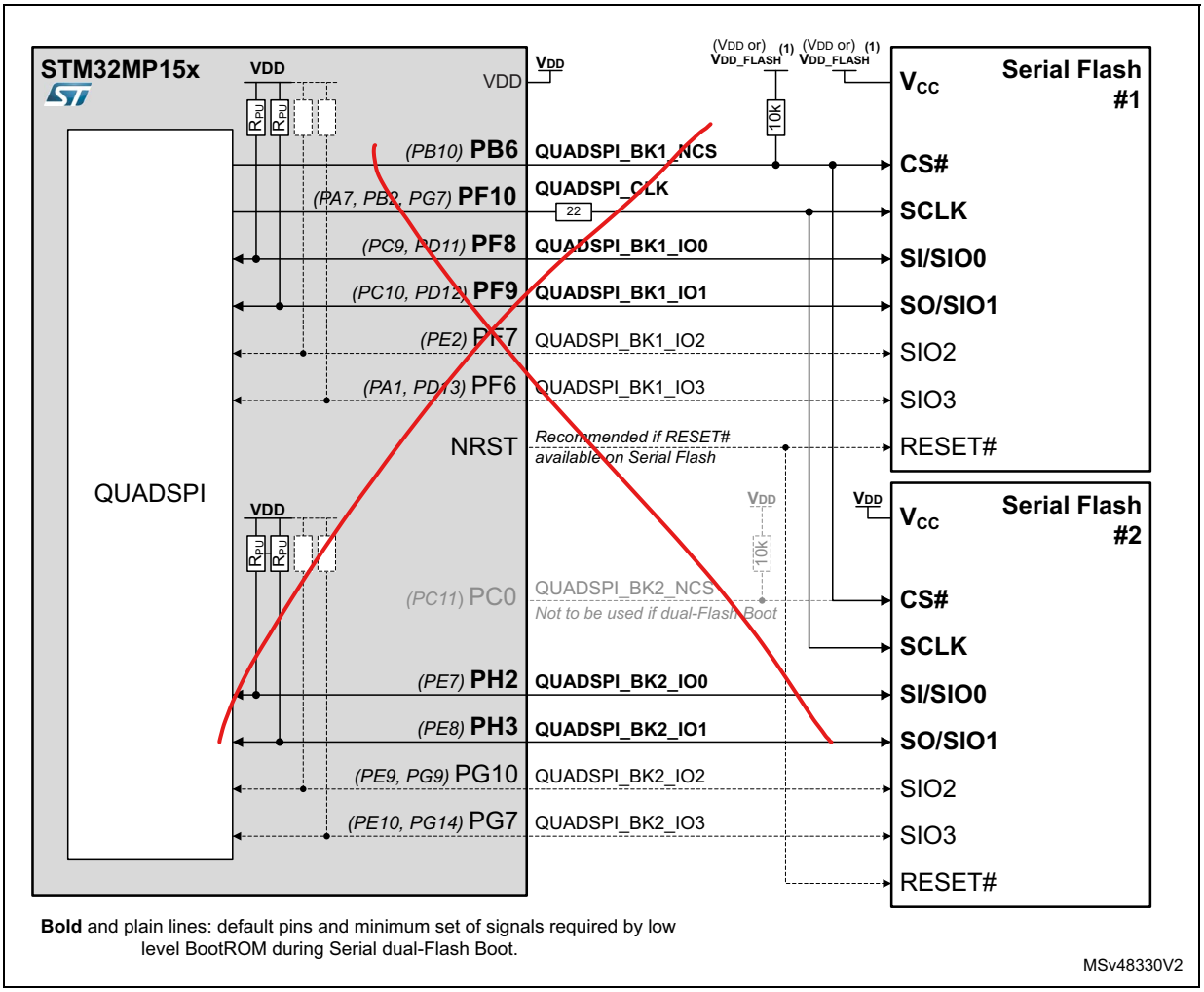
**Figure 39. Serial Flash connection example**




1. $V_{DD\_FLASH}$ must be cut for >1ms to allow reboot (on reset or Standby exit).
2. Decoupling capacitors not shown.
3. During SPI mode boot using SI/SO, some Serial memories can use IO2 and IO3 pins as additional feature such as hold. To enable such device to boot, it might be necessary to set those pins to inactive level by adding external pull-ups or by defining internal pull-up during Boot using OTP.

In case of blank or corrupted Serial Flash memory, after trying to boot from single serial Flash, the Boot ROM tries the Dual-Serial Flash mode, which means PH2 and PH3 can conflict with signals used on the board. If needed, this conflict on PH2 and PH3 can be avoided by programming OTP (Words 3, 5 and 6) to force the Boot ROM to only use the 4 pins needed in 'single serial Flash' configuration.

**Figure 40. Dual-Serial Flash connection example**




1. $V_{DD\_FLASH}$ must be cut for >1ms to allow reboot (on Reset or Standby exit).
2. Decoupling capacitors not shown.
3. During SPI mode boot using SI/SO, some Serial memories can use IO2 and IO3 pins as additional feature such as hold. To enable such device to boot, it might be necessary to set those pins to inactive level by adding external pull-ups or by defining internal pull-up during Boot using OTP.

In case the memory I/O power supply shutdowns independently than $V_{DD}$, NRST must not be directly connected to the memory reset pin and the following options are used:

- Memory reset pin left open if the memory has an internal power on reset
- Connected through a Schottky diode with the cathode on NRST side

Otherwise, NRST is pulled low by memory internal protections when its I/O supply is not present (which may cause an unwanted platform reset).

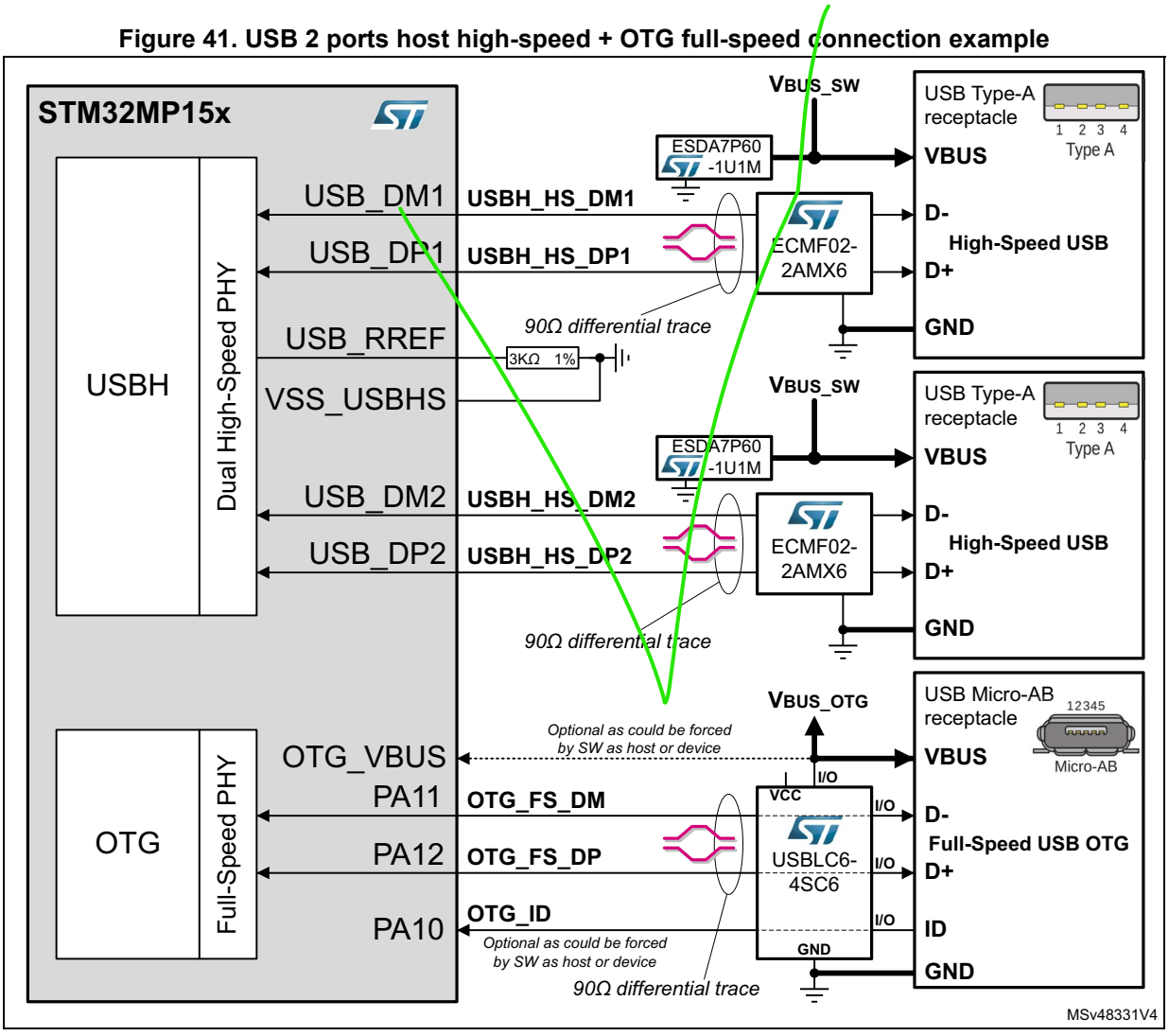
Refer to memory documentation to verify the memory reset pin requirements (especially, the presence of internal power on reset and/or internal pull-up on the reset pin)

### 10.1.12 USB

*Note: USB Type-C is supported with some external component, see www.st.com for dedicated application note.*

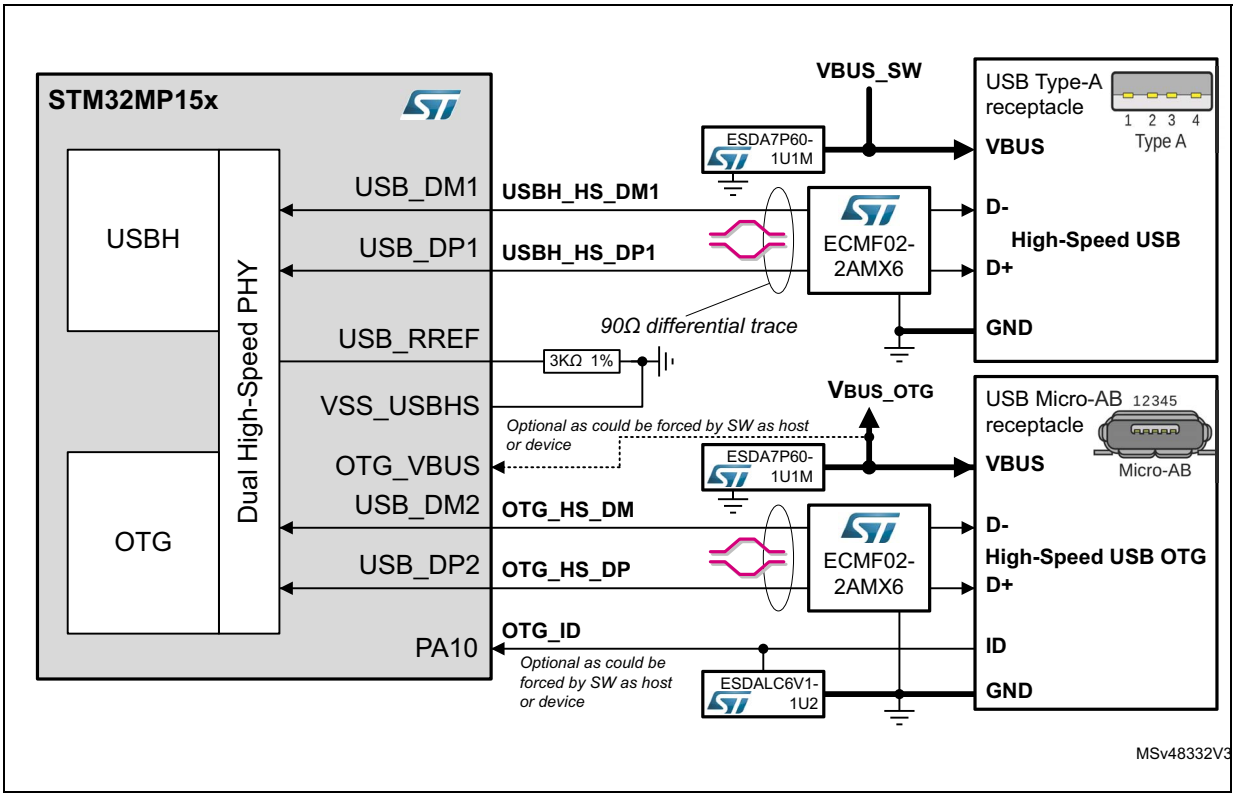
A 3 kOhm 1% resistor must be connected between USB_RREF and $V_{SS\_USBHS}$ (or $V_{SS}$ if $V_{SS\_USBHS}$ is not available on selected package).

**Figure 41. USB 2 ports host high-speed + OTG full-speed connection example**




*Note: On OTG IP, USB full-speed device is also supported by using Micro-B receptacle instead of Micro-AB and leaving the OTG_ID pin unconnected.*

**Figure 42. USB host high-speed + OTG high-speed connection example**




*Note: On OTG IP, USB high-speed device is also supported by using Micro-B receptacle instead of Micro-AB and leaving the OTG_ID pin unconnected.*

### USB high-speed PCB track length matching

Each package has been optimized to provide easier length matching when differential balls pair signals are not directly on adjacent balls. Example: package with 0.8 mm ball pitch, when differential pair are on two different rows, the package already have around 800 µm length internal difference to allow the PCB track to match total length, according to USB standard requirements, with minimum or even no additional routing complexity. The table below shows DM - DP length difference (inside package) at ball level to be taken into account by the PCB tool.

**Table 18. USB package length matching values**

| Pin name | TFBGA257 (10 x 10 pitch 0.5 mm) | | LFBGA354 (16 x 16 pitch 0.8 mm) | | TFBGA361 (12 x 12 pitch 0.5 mm) | | LFBGA448 (18 x 18 pitch 0.8 mm) | |
|---|---|---|---|---|---|---|---|---|
| | Ball position | length difference | Ball position | length difference | Ball position | length difference | Ball position | length difference |
| USB_DM1 | W14 | 486 µm | W14 | 818 µm | AB17 | -507 µm | AB15 | 792 µm |
| USB_DP1 | V14 | | V14 | | AC17 | | AA15 | |
| USB_DM2 | W10 | 494 µm | V13 | -816 µm | AB16 | -500 µm | AA14 | -850 µm |
| USB_DP2 | V10 | | W13 | | AC16 | | AB14 | |

**Figure 43. USB high-speed PCB track example for 0.8 mm ball pitch package**

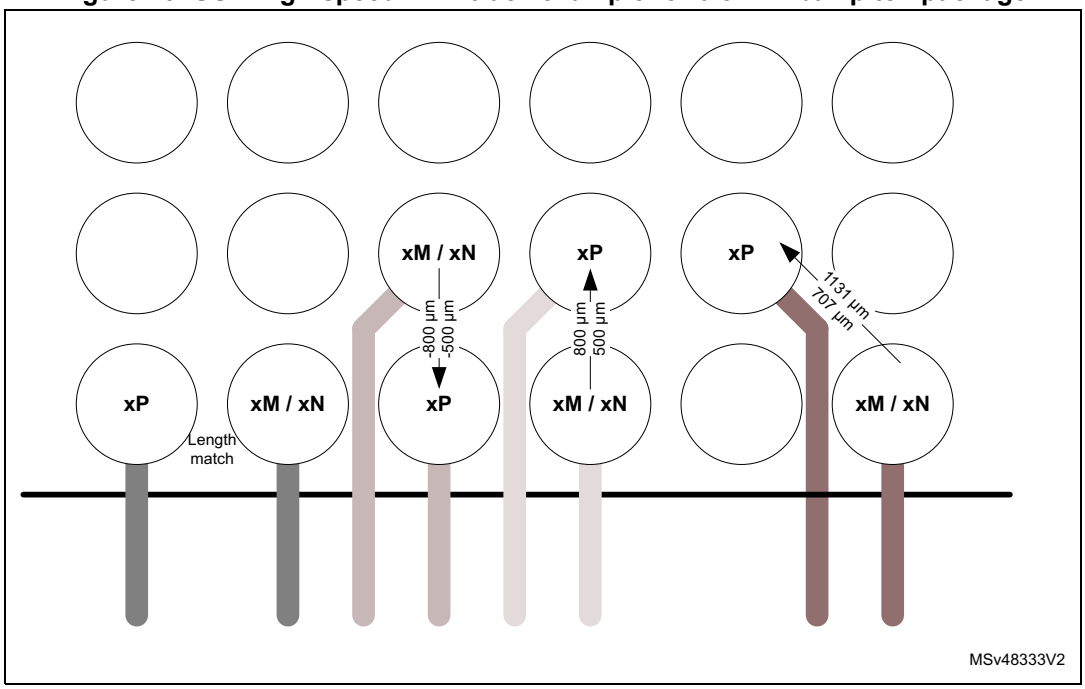


**Table 19. USB high-speed PCB routing recommendations**

| Recommendation | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|
| Differential impedance | 76.5 | 90 | 103.5 | Ω |
| Single-ended impedance | 38.25 | 45 | 51.75 | Ω |
| Length matching within a pair (including package) | -50 | - | +50 | mils |
| | -1.27 | - | +1.27 | mm |
| Maximum traces length (up to connector or first active component) | - | - | 8 | inches |
| | - | - | 203 | mm |
| Maximum number of vias (recommended value) | - | - | 2 | - |
| Distance between any differential trace and other signals | S-2S | S-3S or more | | -(1) |
| Do no route over power plane split. No stubs (point-to-point only). No right angles | | | | |

1. Definition is given for instance in DDR memory routing guidelines (AN5122).

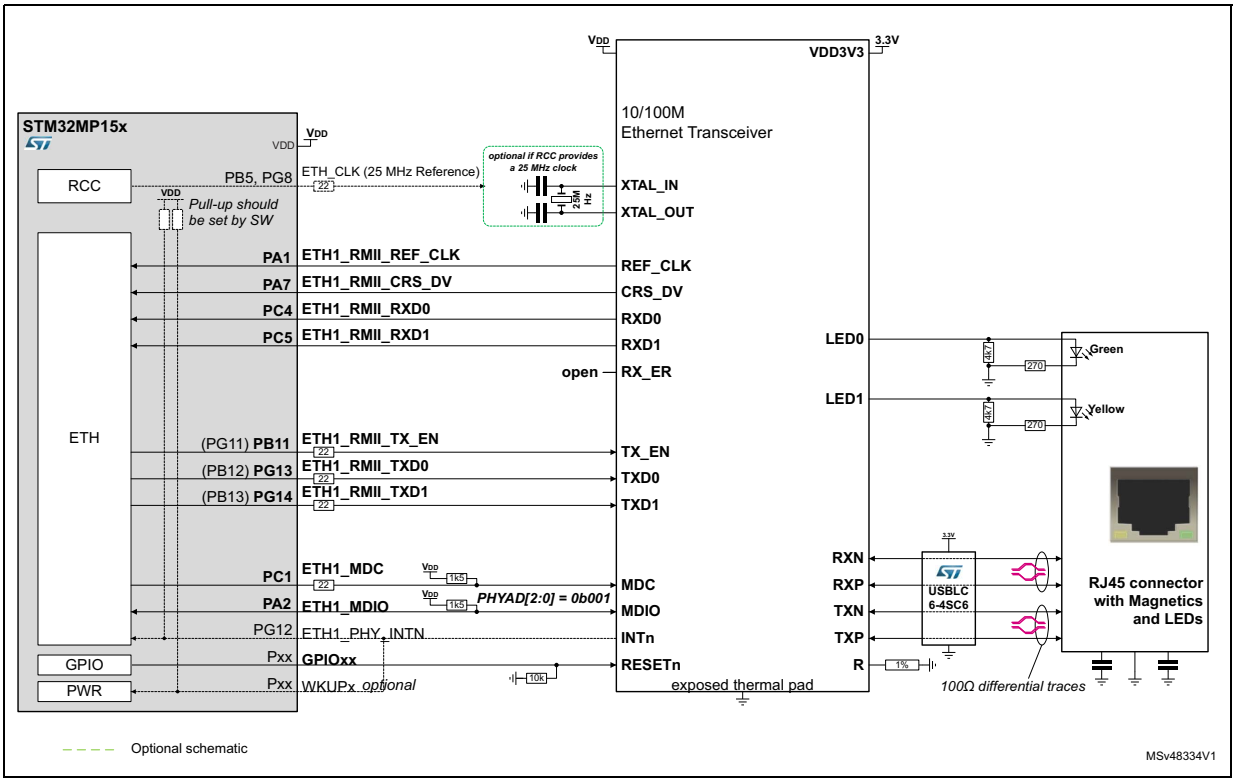
### 10.1.13 Ethernet

#### 10/100M Ethernet

Note that a good signal integrity is dependent on board, GPIO strength settings (GPIO_OSPEEDR registers) and $V_{DD}$ voltage.

If needed, the impedance matching resistors should be placed as close as possible of the output driver pin. The values in example below work in most cases, but can be tailored to each side I/O drive strengths and PCB impedance.

**Figure 44. 10/100M Ethernet PHY connection example**



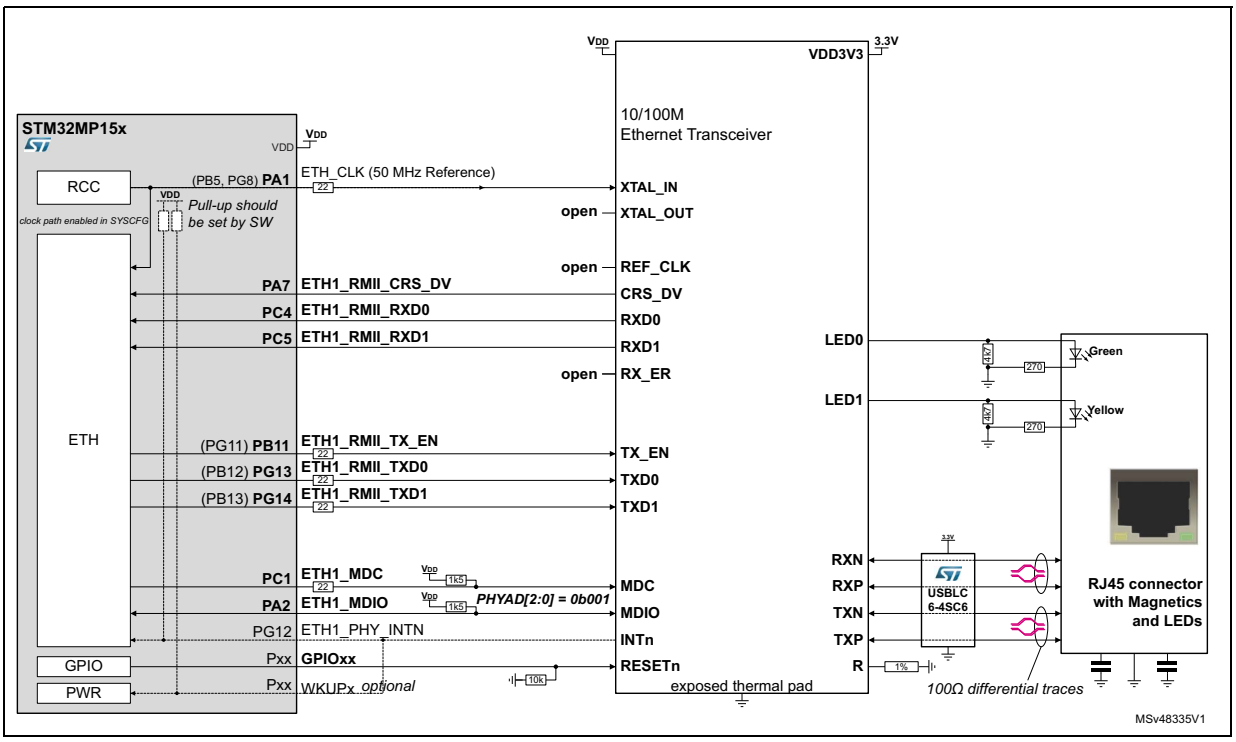

1. Decoupling capacitors not shown.

As the RCC cannot provide the 25 MHz reference clock to the PHY during low power modes, the dedicated 25 MHz crystal is required on the PHY in case wakeup on LAN (WOL) is needed for the platform.

Setting the RCC PLLs to get 25 MHz output for PHY clocking might constrain other RCC frequencies. In that case it is more flexible to put a dedicated 25 MHz crystal on the PHY.

Alternatively, if PHY allows it and if RCC can provide a precise 50 MHz clock (possibility must be checked with respect to HSE quartz frequency and RCC other peripheral/core clocks frequency settings), a 50 MHz ETH_CLK can be provided by the STM32MP15x lines to the PHY, and REF_CLK is left unconnected on both sides. This saves BOM and area, as well as some power on some PHYs.

**Figure 45. 10/100M Ethernet PHY connection with REFCLK from RCC example**




1. Decoupling capacitors not shown.

As the RCC cannot provide the 50 MHz reference clock to the PHY during low power modes, this option is not possible in case wakeup on LAN (WOL) is needed for the platform.

Setting the RCC PLLs to get 50 MHz output for PHY clocking might constrain other RCC frequencies. In that case, this option is not possible.

## Gigabit Ethernet

Note that a good signal integrity is dependent on board, GPIO strength settings (GPIO_OSPEEDR registers) and $V_{DD}$ voltage.
When using $V_{DD}$ = 1.8 V, a setting in the OTP bit and the register SYSCFG_IOCTRLSETR (HSLVEN_ETH bit) is required to ensure the best speed on pads used on Ethernet outputs.

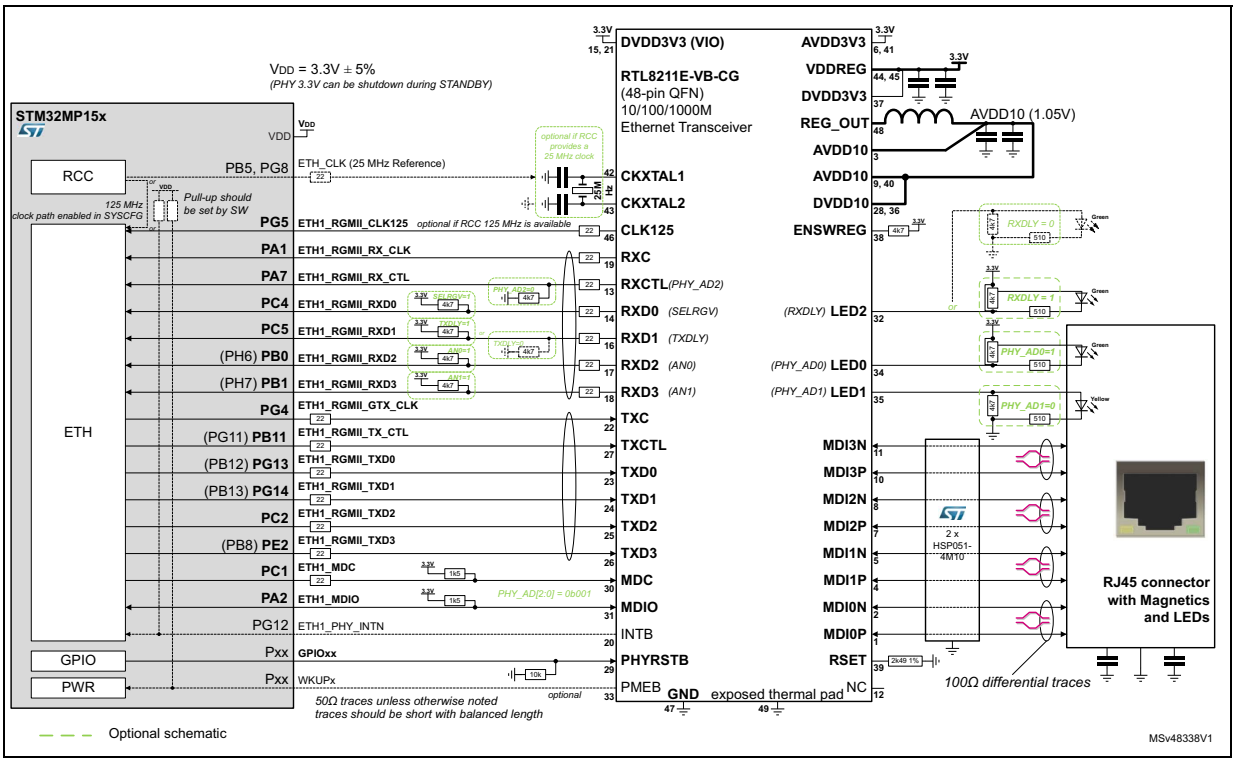
**Warning: HSLVEN_xxx must not be set when $V_{DD}$ is above 2.7 V otherwise permanent IC damage might occur.**

If needed, the impedance matching resistors should be placed as close as possible of the output driver pin. The values in the example below work in most cases, but can be tailored to each side I/O drive strengths and PCB impedance.

As the RCC cannot provide the 25 MHz reference clock to the PHY during low power modes, the dedicated 25 MHz crystal is required on the PHY in case wakeup on LAN (WOL) is needed for the platform.

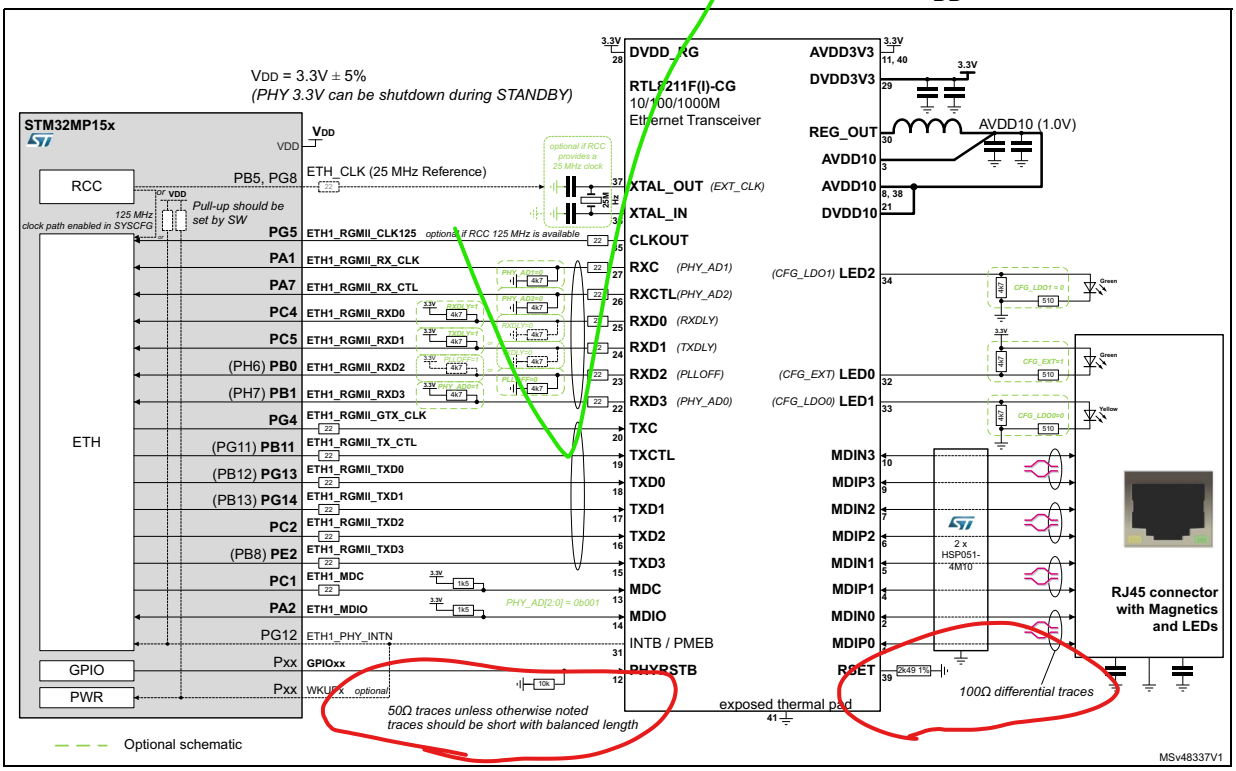
Setting the RCC PLLs to get 25 MHz output for PHY might constrain other RCC frequencies. In that case it is more flexible to put a dedicated 25 MHz crystal on the PHY.

**Figure 46. Gigabit Ethernet PHY connection example with $V_{DD}$ = 3.3 V (RTL8211E)**



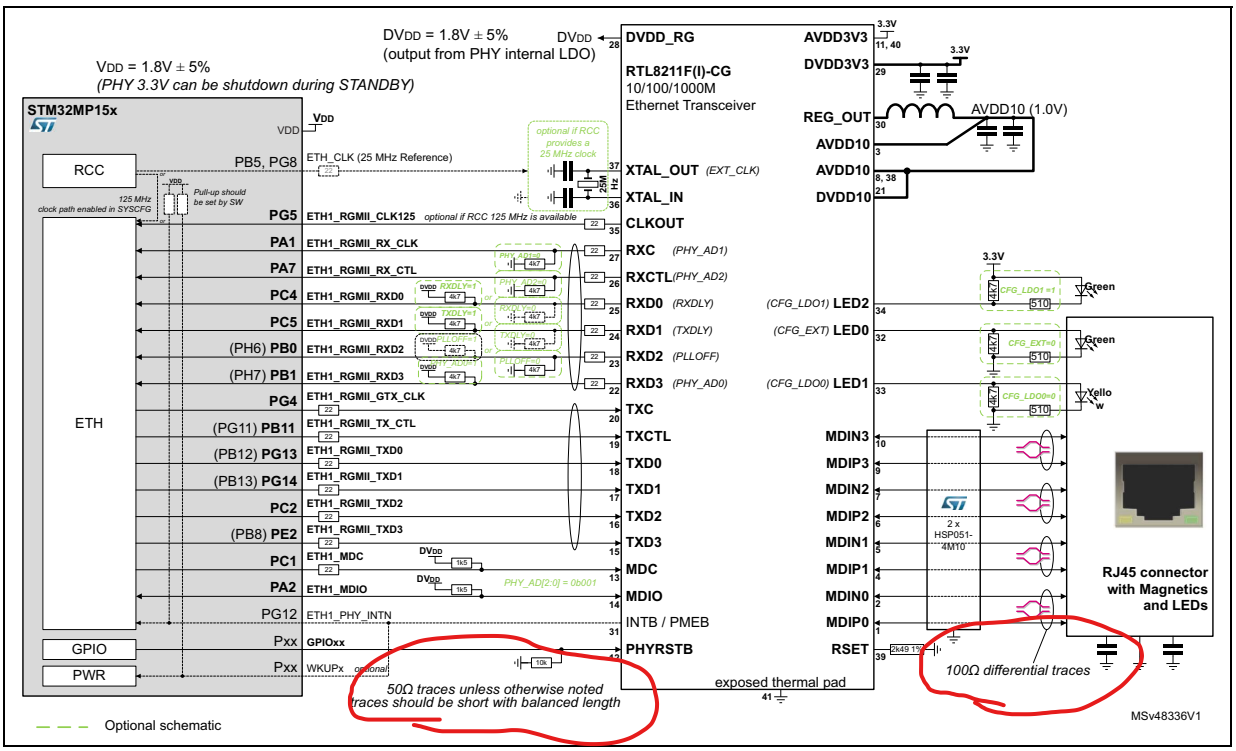

1. Decoupling capacitors not shown.

**Figure 47. Gigabit Ethernet PHY connection example with $V_{DD}$ = 3.3 V (RTL8211F)**



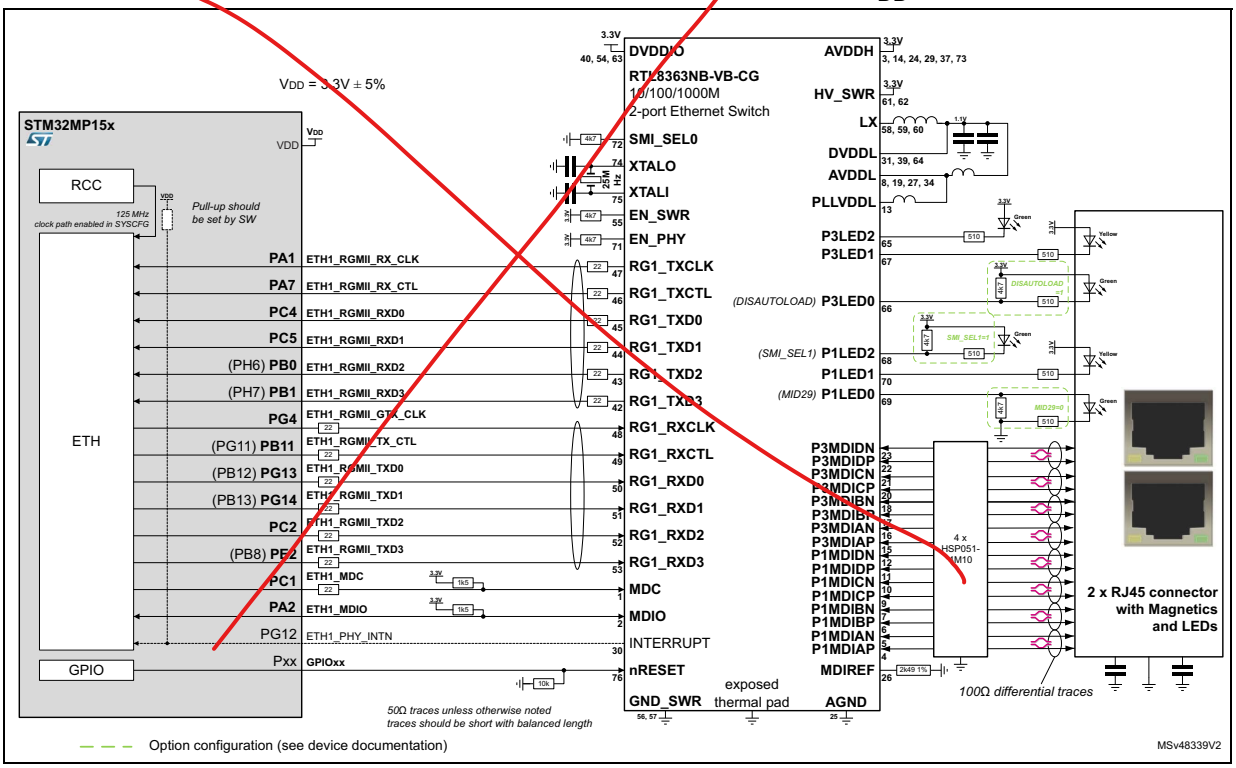

1. Decoupling capacitors not shown.

**Figure 48. Gigabit Ethernet PHY connection example with $V_{DD}$ = 1.8 V (RTL8211F)**




1. Decoupling capacitors not shown.

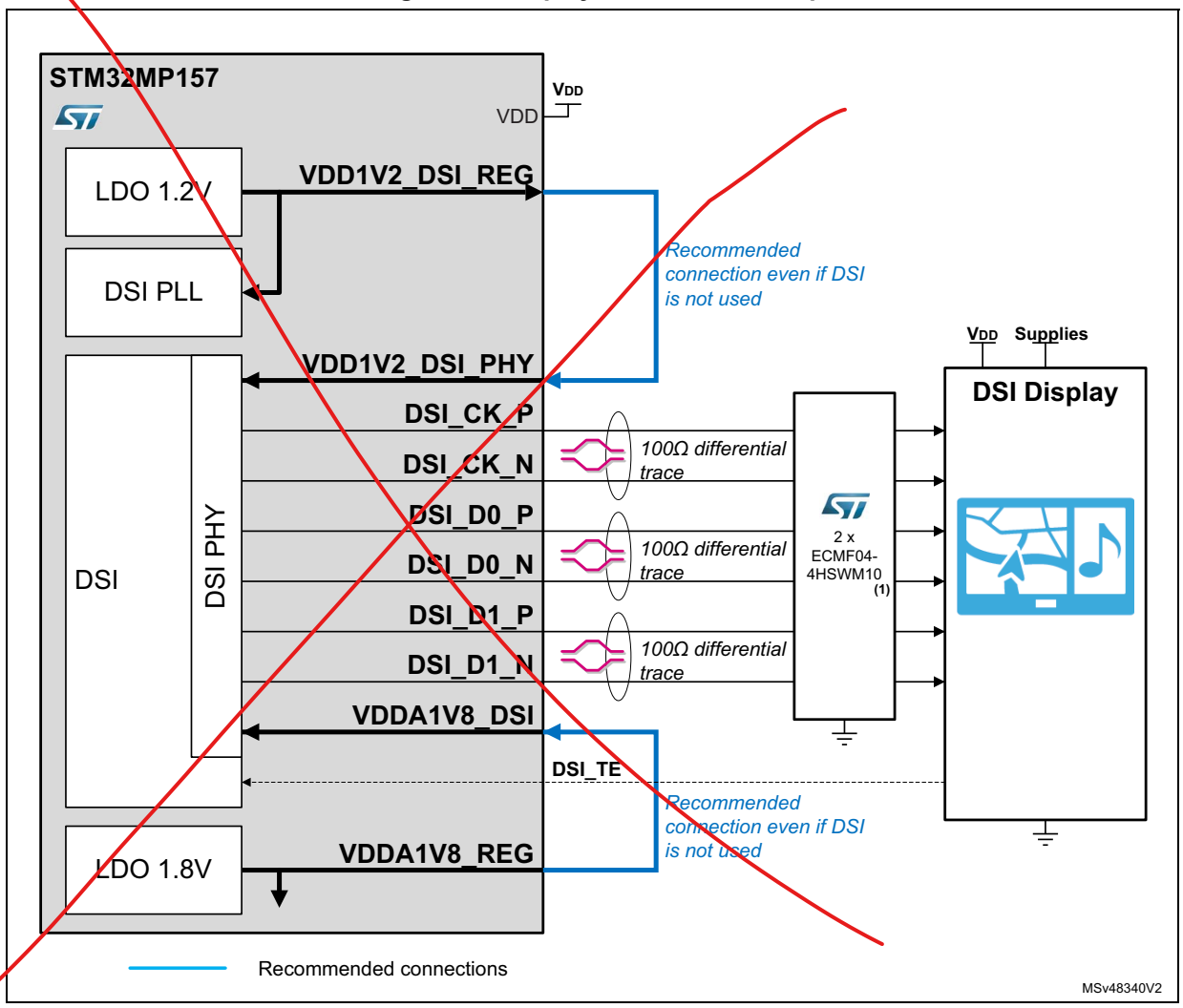
**Figure 49. Gigabit Ethernet 2-port switch example with $V_{DD}$ = 3.3 V (RTL8363NB-VG)**




1. Decoupling capacitors not shown.

### 10.1.14 Display serial interface (DSI)

**Figure 50. Display connection example with DSI**




1. ECMF04-4HSWM10 includes common mode filter for WLAN/BT bands. For ESD protection only, HSP051-4M10 can be used instead (similar while not the same footprint).
2. Decoupling capacitors not shown.
3. Availability of DSI depends on the STM32MP15x lines devices.

### DSI interface PCB track length matching

Each package has been optimized to provide easier length matching when differential balls pair signals are not directly on adjacent balls. Example: package with 0.8 mm ball pitch, when differential pairs are on two different rows, the package already have around 800 µm length internal difference to allow the PCB track to match total length with minimum or even no additional routing complexity. *Table 20* shows DM - DP length difference (inside package) at ball level to be taken into account by the PCB tool.

**Table 20. DSI package length matching values**

| Pin name | TFBGA257 (10 x 10 pitch 0.5 mm) | | LFBGA354 (16 x 16 pitch 0.8 mm) | | TFBGA361 (12 x 12 pitch 0.5 mm) | | LFBGA448 (18 x 18 pitch 0.8 mm) | |
|---|---|---|---|---|---|---|---|---|
| | Ball position | Length difference | Ball position | Length difference | Ball position | Length difference | Ball position | Length difference |
| DSI_CKN | B12 | -505 µm | A14 | 822 µm | A16 | 490 µm | A16 | 867 µm |
| DSI_CKP | A12 | | B14 | | B16 | | B16 | |
| DSI_D0N | C12 | -736 µm | A13 | 781 µm | B15 | 514 µm | A15 | 791 µm |
| DSI_D0P | B11 | | B13 | | C15 | | B15 | |
| DSI_D1N | B13 | -507 µm | A15 | 804 µm | A17 | 505 µm | A17 | 785 µm |
| DSI_D1P | A13 | | B15 | | B17 | | B17 | |

**Figure 51. DSI interface PCB track example for 0.8 mm ball pitch package**

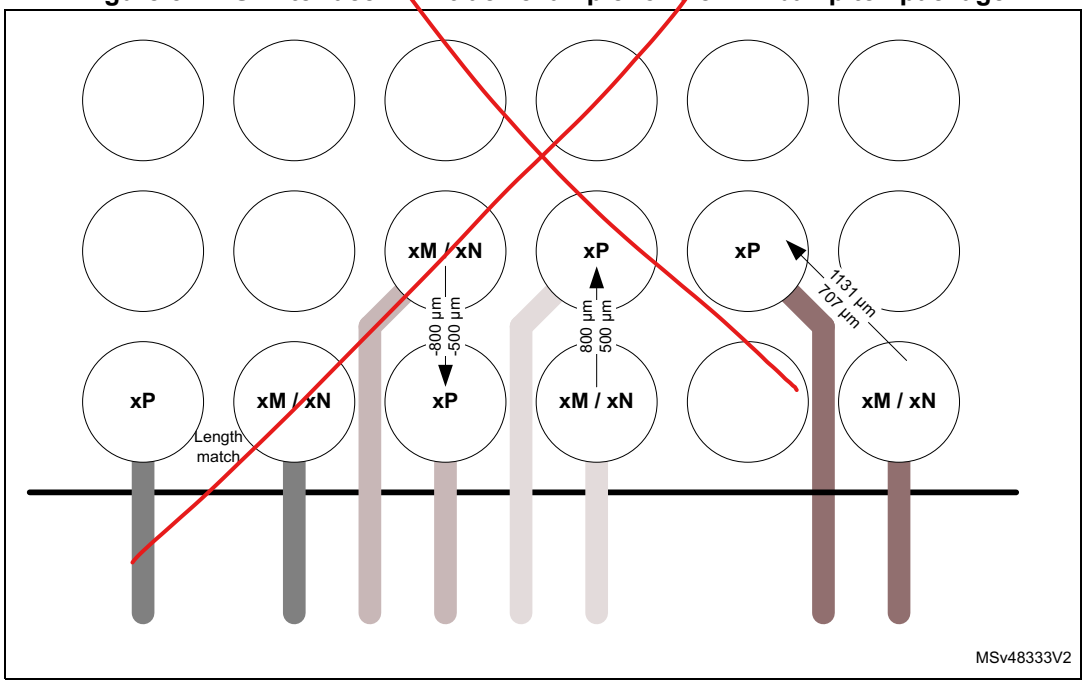


**Table 21. DSI PCB routing recommendations**

| Recommendation | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|
| Differential impedance | 90 | 100 | 110 | Ω |
| Single-ended impedance | 45 | 50 | 55 | Ω |
| Length matching within a pair (including package) | -5 | - | +5 | mils |
| | -0.127 | - | +0.127 | mm |
| Length matching between pairs | -200 | - | +200 | mils |
| | -5.08 | - | +5.08 | mm |
| Max link length (including display cables) | - | - | 8 | inches |
| | - | - | 203 | mm |
| Max number of vias (recommended value) | - | - | 2 | - |
| Distance between any differential trace and other signals | S-2S | S-3S or more | | -(1) |
| Do no route over power plane split. No stubs (point to point only). No right angles | | | | |

1. Refer to *STM32MP1 Series DDR memory routing guidelines* application note (AN5122) for the definition.

# 11 Revision history

Rev 5

**Table 22. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 01-Feb-2019 | 1 | Initial release. |
| 14-Apr-2020 | 2 | Updated:<br>– Cover replacing STM32MP1 Series by STM32MP151, STM32MP153 and STM32MP157 lines.<br>– *Table 1: Reference documents*.<br>– *Section 4.1: Introduction* USB supplies.<br>– *Section 4.2: Power supply schemes*.<br>– *Table 4: Amount of decoupling recommendation by package*.<br>– *Figure 8: 12x12 TFBGA361 compatibility*.<br>– *Figure 30: Discrete supplies example 3.3 V I/Os with DDR3L*.<br>– *Figure 31: PMIC example 3.3 V I/Os with DDR3L*<br>– *Figure 41: USB 2 ports host high-speed + OTG full-speed connection example*.<br>– *Figure 49: Gigabit Ethernet 2-port switch example with VDD = 3.3 V (RTL8363NB-VG)*.<br>Removed:<br>– ST1S31PUR SMPS details figure.<br>– Components example for 1.2 V 2A table.<br>– Components example for 1.35 V 1A table. |
| 14-Jan-2021 | 3 | Updated:<br>– Table 6: Major feature changes related to packages.<br>– Section 4.3.3: Application and system resets.<br>– Figure 4: Simplified reset pin circuit.<br>– Section 7.3: Embedded boot loader mode.<br>– Table 12: Boot modes.<br>– Figure 30: Discrete supplies example 3.3 V I/Os with DDR3L.<br>– Figure 31: PMIC example 3.3 V I/Os with DDR3L.<br>– Figure 32: PMIC example 1.8 V I/Os with LPDDR2/LPDDR3.<br>– Section 10.1.11: Serial NOR-Flash/NAND-Flash.<br>– Section 10.1.13: Ethernet.<br>– Section 10.1.14: Display serial interface (DSI) |
| 27-Jan-2022 | 4 | Updated:<br>*Section 6.1: HSE OSC clock*<br>*Section 6.2: LSE OSC clock*<br>*Section 10.1.8: SD card*<br>*Section 10.1.9: eMMC™ Flash*<br>*Section 10.1.11: Serial NOR-Flash/NAND-Flash*<br>Added:<br>*Table 5: Supply usage for unused features*<br>*Table 19: USB high-speed PCB routing recommendations* |

Table 22. Document revision history (continued)

| Date | Revision | Changes |
|---|---|---|
| 28-Sep-2022 | 5 | Updated:<br>*Figure 34*<br>*Figure 41*<br>*Figure 42*<br>Added footnotes below:<br>*Figure 31*<br>*Figure 32* |