
STM32
CubeMX

1. Description

1.1. Project

Project Name	STM32 Computer
Board Name	custom
Generated with:	STM32CubeMX 6.10.0
Date	05/12/2024

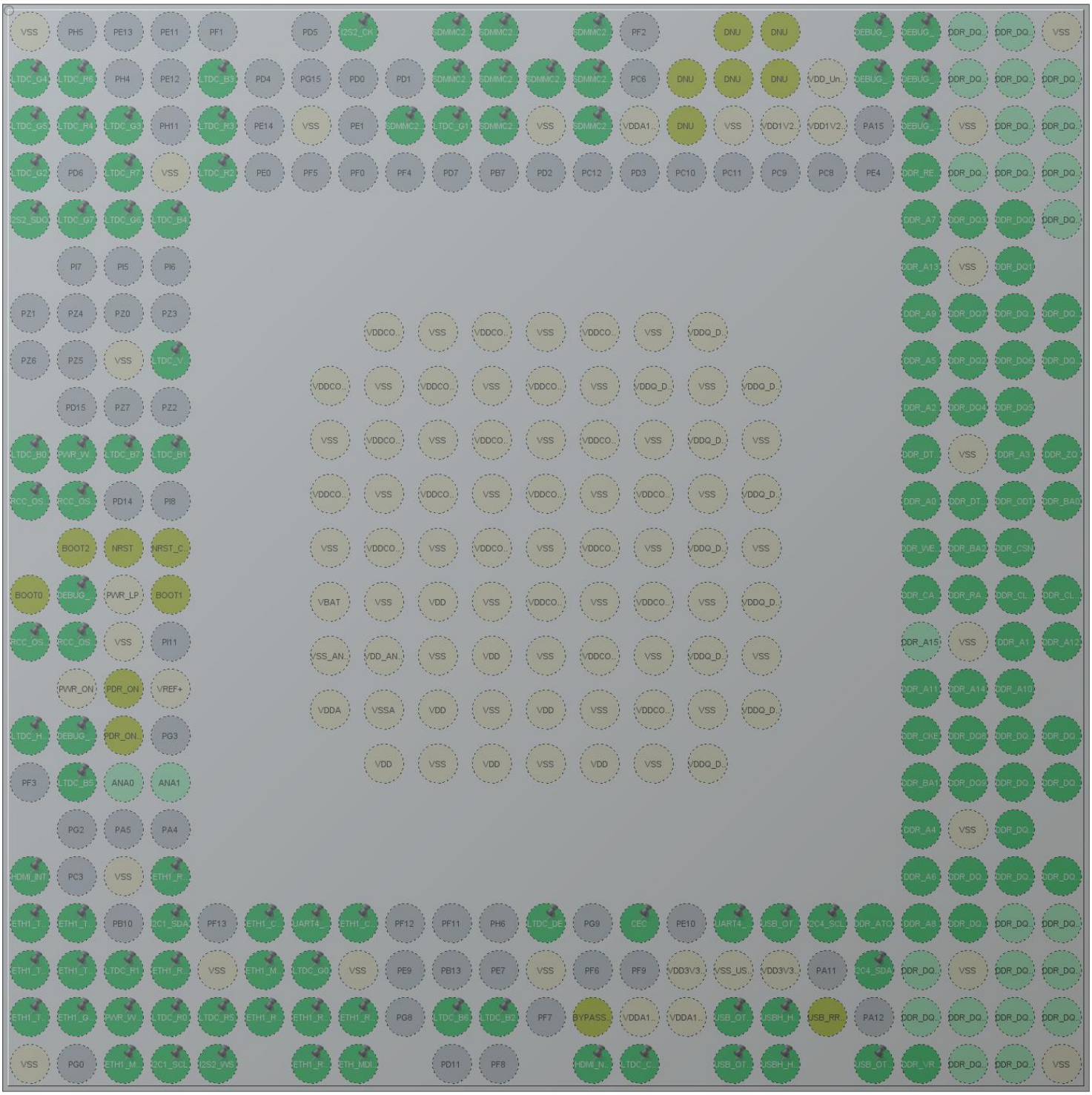
1.2. MCU

MCU Series	STM32MP1
MCU Line	STM32MP151
MCU name	STM32MP151AACx
MCU Package	TFBGA361
MCU Pin number	361

1.3. Core(s) information

Core(s)	ARM Cortex-A7 ARM Cortex-M4

2. Pinout Configuration



TFBGA361 (Top view)

3. Pins Configuration

Pin Number TFBGA361	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
A1	VSS	Power		
A8	PA9	I/O	I2S2_CK	
A10	PG6	I/O	SDMMC2_CMD	
A11	PB3	I/O	SDMMC2_D2	
A13	PA8	I/O	SDMMC2_D4	
A16	DNU	MonoIO		
A17	DNU	MonoIO		
A19	JTDO-TRACESWO	MonoIO	DEBUG_JTDO-SWO	
A20	JTDI	MonoIO	DEBUG_JTDI	
A23	VSS	Power		
B1	PH15	I/O	LTDC_G4	
B2	PH12	I/O	LTDC_R6	
B5	PD10	I/O	LTDC_B3	
B10	PB9	I/O	SDMMC2_D5	
B11	PC7	I/O	SDMMC2_D7	
B12	PB15	I/O	SDMMC2_D1	
B13	PB4	I/O	SDMMC2_D3	
B15	DNU	MonoIO		
B16	DNU	MonoIO		
B17	DNU	MonoIO		
B18	VDD_Unused	Power		
B19	NJTRST	MonoIO	DEBUG_JTRST	
B20	JTCK-SWCLK	MonoIO	DEBUG_JTCK-SWCLK	
C1	PI0	I/O	LTDC_G5	
C2	PH10	I/O	LTDC_R4	
C3	PH14	I/O	LTDC_G3	
C5	PH9	I/O	LTDC_R3	
C7	VSS	Power		
C9	PE3	I/O	SDMMC2_CK	
C10	PE6	I/O	LTDC_G1	
C11	PE5	I/O	SDMMC2_D6	
C12	VSS	Power		
C13	PB14	I/O	SDMMC2_D0	
C14	VDDA1V8_Unused	Power		
C15	DNU	MonoIO		
C16	VSS	Power		

Pin Number TFBGA361	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
C17	VDD1V2_Unused	Power		
C18	VDD1V2_Unused	Power		
C20	JTMS-SWDIO	MonoIO	DEBUG_JTMS-SWDIO	
C21	VSS	Power		
D1	PH13	I/O	LTDC_G2	
D3	PE15	I/O	LTDC_R7	
D4	VSS	Power		
D5	PH8	I/O	LTDC_R2	
D20	DDR_RESETN	MonoIO	DDR_RESETN	
E1	PI3	I/O	I2S2_SDO	
E2	PI2	I/O	LTDC_G7	
E3	PI1	I/O	LTDC_G6	
E4	PI4	I/O	LTDC_B4	
E20	DDR_A7	MonoIO	DDR_A7	
E21	DDR_DQ3	MonoIO	DDR_DQ3	
E22	DDR_DQ0	MonoIO	DDR_DQ0	
F20	DDR_A13	MonoIO	DDR_A13	
F21	VSS	Power		
F22	DDR_DQ1	MonoIO	DDR_DQ1	
G20	DDR_A9	MonoIO	DDR_A9	
G21	DDR_DQ7	MonoIO	DDR_DQ7	
G22	DDR_DQS0P	MonoIO	DDR_DQS0P	
G23	DDR_DQS0N	MonoIO	DDR_DQS0N	
H3	VSS	Power		
H4	PI9	I/O	LTDC_VSYNC	
H20	DDR_A5	MonoIO	DDR_A5	
H21	DDR_DQ2	MonoIO	DDR_DQ2	
H22	DDR_DQ6	MonoIO	DDR_DQ6	
H23	DDR_DQM0	MonoIO	DDR_DQM0	
J20	DDR_A2	MonoIO	DDR_A2	
J21	DDR_DQ4	MonoIO	DDR_DQ4	
J22	DDR_DQ5	MonoIO	DDR_DQ5	
K1	PD9	I/O	LTDC_B0	
K2	PC13	I/O	PWR_WKUP3	
K3	PD8	I/O	LTDC_B7	
K4	PG12	I/O	LTDC_B1	
K20	DDR_DTO0	MonoIO	DDR_DTO0	
K21	VSS	Power		
K22	DDR_A3	MonoIO	DDR_A3	

Pin Number TFBGA361	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
K23	DDR_ZQ	MonoIO	DDR_ZQ	
L1	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
L2	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
L20	DDR_A0	MonoIO	DDR_A0	
L21	DDR_DTO1	MonoIO	DDR_DTO1	
L22	DDR_ODT	MonoIO	DDR_ODT	
L23	DDR_BA0	MonoIO	DDR_BA0	
M2	BOOT2	Boot		
M3	NRST	Reset		
M4	NRST_CORE	Reset		
M20	DDR_WEN	MonoIO	DDR_WEN	
M21	DDR_BA2	MonoIO	DDR_BA2	
M22	DDR_CSN	MonoIO	DDR_CSN	
N1	BOOT0	Boot		
N2	PA13	I/O	DEBUG_DBTRGI	
N3	PWR_LP	Power		
N4	BOOT1	Boot		
N20	DDR_CASN	MonoIO	DDR_CASN	
N21	DDR_RASN	MonoIO	DDR_RASN	
N22	DDR_CLKP	MonoIO	DDR_CLKP	
N23	DDR_CLKN	MonoIO	DDR_CLKN	
P1	PH0-OSC_IN	I/O	RCC_OSC_IN	
P2	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
P3	VSS	Power		
P21	VSS	Power		
P22	DDR_A1	MonoIO	DDR_A1	
P23	DDR_A12	MonoIO	DDR_A12	
R2	PWR_ON	Power		
R3	PDR_ON	MonoIO		
R4	VREF+	Power		
R20	DDR_A11	MonoIO	DDR_A11	
R21	DDR_A14	MonoIO	DDR_A14	
R22	DDR_A10	MonoIO	DDR_A10	
T1	PI10	I/O	LTDC_HSYNC	
T2	PA14	I/O	DEBUG_DBTRGO	
T3	PDR_ON_CORE	MonoIO		
T20	DDR_CKE	MonoIO	DDR_CKE	
T21	DDR_DQ8	MonoIO	DDR_DQ8	
T22	DDR_DQ10	MonoIO	DDR_DQ10	

Pin Number TFBGA361	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
T23	DDR_DQ13	MonoIO	DDR_DQ13	
U2	PA3	I/O	LTDC_B5	
U20	DDR_BA1	MonoIO	DDR_BA1	
U21	DDR_DQ9	MonoIO	DDR_DQ9	
U22	DDR_DQS1P	MonoIO	DDR_DQS1P	
U23	DDR_DQS1N	MonoIO	DDR_DQS1N	
V20	DDR_A4	MonoIO	DDR_A4	
V21	VSS	Power		
V22	DDR_DQM1	MonoIO	DDR_DQM1	
W1	PG1	I/O	GPIO_EXTI1	HDMI_INT
W3	VSS	Power		
W4	PH7	I/O	ETH1_RXD3	
W20	DDR_A6	MonoIO	DDR_A6	
W21	DDR_DQ11	MonoIO	DDR_DQ11	
W22	DDR_DQ14	MonoIO	DDR_DQ14	
W23	DDR_DQ12	MonoIO	DDR_DQ12	
Y1	PE2	I/O	ETH1_TXD3	
Y2	PC2	I/O	ETH1_TXD2	
Y4	PF15	I/O	I2C1_SDA	
Y6	PG5	I/O	ETH1_CLK125	
Y7	PG11	I/O	UART4_TX	
Y8	PB5	I/O	ETH1_CLK	
Y12	PF10	I/O	LTDC_DE	
Y14	PB6	I/O	CEC	
Y16	PB2	I/O	UART4_RX	
Y17	PA10	I/O	USB_OTG_HS_ID	
Y18	PD12	I/O	I2C4_SCL	
Y19	DDR_ATO	MonoIO	DDR_ATO	
Y20	DDR_A8	MonoIO	DDR_A8	
Y21	DDR_DQ15	MonoIO	DDR_DQ15	
AA1	PG14	I/O	ETH1_TXD1	
AA2	PG13	I/O	ETH1_TXD0	
AA3	PH3	I/O	LTDC_R1	
AA4	PA1	I/O	ETH1_RX_CLK	
AA5	VSS	Power		
AA6	PC1	I/O	ETH1_MDC	
AA7	PB1	I/O	LTDC_G0	
AA8	VSS	Power		
AA12	VSS	Power		

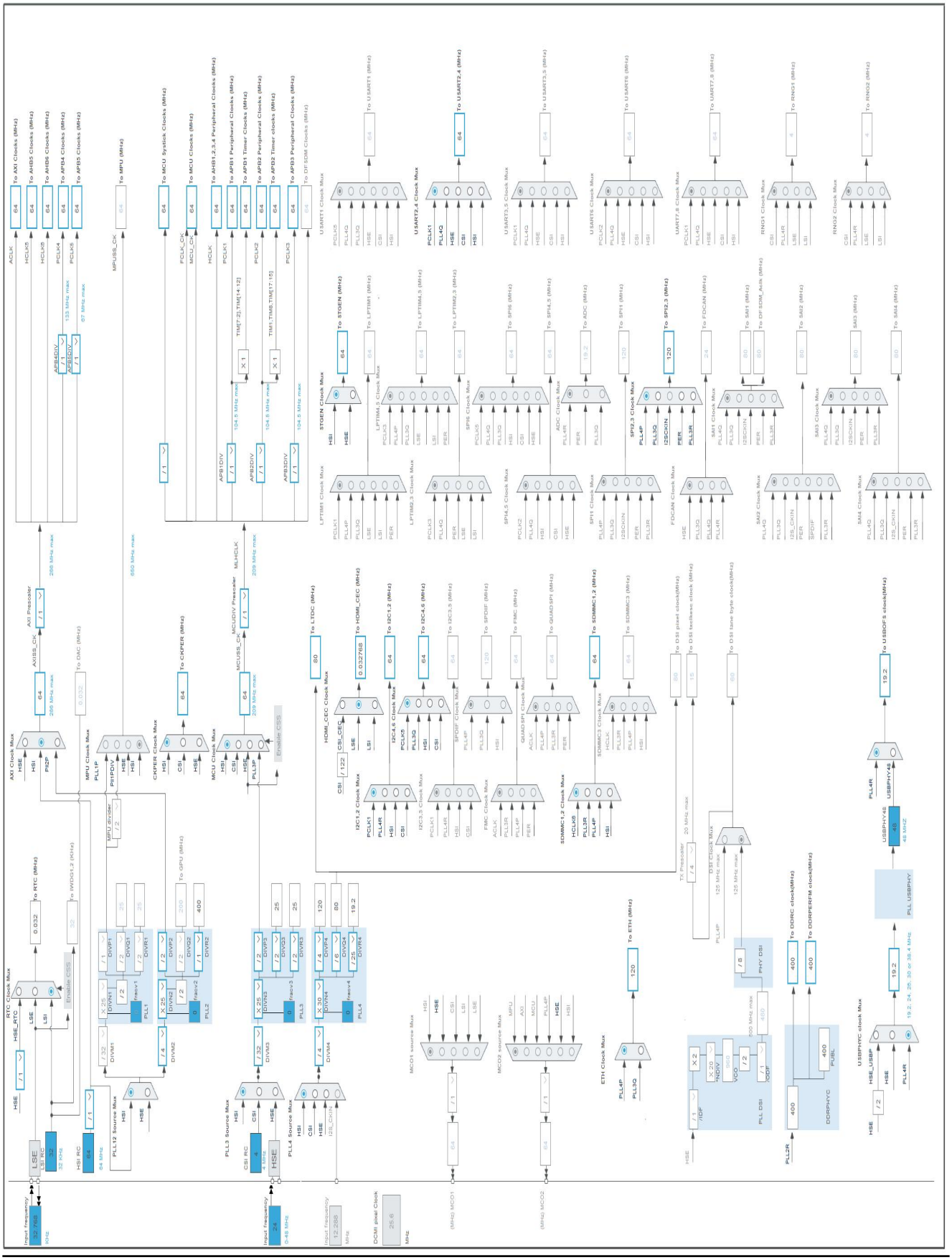
Pin Number TFBGA361	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
AA15	VDD3V3_USBHS	Power		
AA16	VSS_USBHS	Power		
AA17	VDD3V3_USBFS	Power		
AA19	PD13	I/O	I2C4_SDA	
AA21	VSS	Power		
AB1	PB11	I/O	ETH1_TX_CTL	
AB2	PG4	I/O	ETH1_GTX_CLK	
AB3	PA0	I/O	PWR_WKUP1	
AB4	PH2	I/O	LTDC_R0	
AB5	PC0	I/O	LTDC_R5	
AB6	PB0	I/O	ETH1_RXD2	
AB7	PC5	I/O	ETH1_RXD1	
AB8	PA7	I/O	ETH1_RX_CTL	
AB10	PB8	I/O	LTDC_B6	
AB11	PG10	I/O	LTDC_B2	
AB13	BYPASS_REG1V8	MonoIO		
AB14	VDDA1V8_REG	Power		
AB15	VDDA1V1_REG	Power		
AB16	USB_DM2	MonoIO	USB_OTG_HS_DM	
AB17	USB_DM1	MonoIO	USBH_HS1_DM	
AB18	USB_RREF	MonoIO		
AC1	VSS	Power		
AC3	PA2	I/O	ETH1_MDIO	
AC4	PF14	I/O	I2C1_SCL	
AC5	PB12	I/O	I2S2_WS	
AC7	PC4	I/O	ETH1_RXD0	
AC8	PA6	I/O	GPIO_EXTI6	ETH_MDINT
AC13	PE8 *	I/O	GPIO_Output	HDMI_NRST
AC14	PG7	I/O	LTDC_CLK	
AC16	USB_DP2	MonoIO	USB_OTG_HS_DP	
AC17	USB_DP1	MonoIO	USBH_HS1_DP	
AC19	OTG_VBUS	MonoIO	USB_OTG_HS_VBUS	
AC20	DDR_VREF	MonoIO	DDR_VREF	
AC23	VSS	Power		
1A2	VDDCORE	Power		
1A3	VSS	Power		
1A4	VDDCORE	Power		
1A5	VSS	Power		
1A6	VDDCORE	Power		

Pin Number TFBGA361	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1A7	VSS	Power		
1A8	VDDQ_DDR	Power		
1B1	VDDCORE	Power		
1B2	VSS	Power		
1B3	VDDCORE	Power		
1B4	VSS	Power		
1B5	VDDCORE	Power		
1B6	VSS	Power		
1B7	VDDQ_DDR	Power		
1B8	VSS	Power		
1B9	VDDQ_DDR	Power		
1C1	VSS	Power		
1C2	VDDCORE	Power		
1C3	VSS	Power		
1C4	VDDCORE	Power		
1C5	VSS	Power		
1C6	VDDCORE	Power		
1C7	VSS	Power		
1C8	VDDQ_DDR	Power		
1C9	VSS	Power		
1D1	VDDCORE	Power		
1D2	VSS	Power		
1D3	VDDCORE	Power		
1D4	VSS	Power		
1D5	VDDCORE	Power		
1D6	VSS	Power		
1D7	VDDCORE	Power		
1D8	VSS	Power		
1D9	VDDQ_DDR	Power		
1E1	VSS	Power		
1E2	VDDCORE	Power		
1E3	VSS	Power		
1E4	VDDCORE	Power		
1E5	VSS	Power		
1E6	VDDCORE	Power		
1E7	VSS	Power		
1E8	VDDQ_DDR	Power		
1E9	VSS	Power		
1F1	VBAT	Power		

Pin Number TFBGA361	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1F2	VSS	Power		
1F3	VDD	Power		
1F4	VSS	Power		
1F5	VDDCORE	Power		
1F6	VSS	Power		
1F7	VDDCORE	Power		
1F8	VSS	Power		
1F9	VDDQ_DDR	Power		
1G1	VSS_ANA	Power		
1G2	VDD_ANA	Power		
1G3	VSS	Power		
1G4	VDD	Power		
1G5	VSS	Power		
1G6	VDDCORE	Power		
1G7	VSS	Power		
1G8	VDDQ_DDR	Power		
1G9	VSS	Power		
1H1	VDDA	Power		
1H2	VSSA	Power		
1H3	VDD	Power		
1H4	VSS	Power		
1H5	VDD	Power		
1H6	VSS	Power		
1H7	VDDCORE	Power		
1H8	VSS	Power		
1H9	VDDQ_DDR	Power		
1J2	VDD	Power		
1J3	VSS	Power		
1J4	VDD	Power		
1J5	VSS	Power		
1J6	VDD	Power		
1J7	VSS	Power		
1J8	VDDQ_DDR	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	STM32 Computer
Project Folder	C:\Users\dmn\STM32Cube\Projekt\STM32 Computer
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_MP1 V1.6.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls ARM Cortex-A7

Rank	Function Name	Peripheral Instance Name

5.4. Advanced Settings - Generated Function Calls ARM Cortex-M4

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_ETZPC_Init	ETZPC

1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32MP1
Line	STM32MP151
MCU	STM32MP151AACx
Datasheet	DS12500_Rev3

1.2. Parameter Selection

Temperature	25
Vdd	3.0

1.3. Battery Selection

Battery	Li-SOCL2(DD36000)
Capacity	36000.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	450.0 mA
Max Pulse Current	1000.0 mA
Cells in series	1
Cells in parallel	1

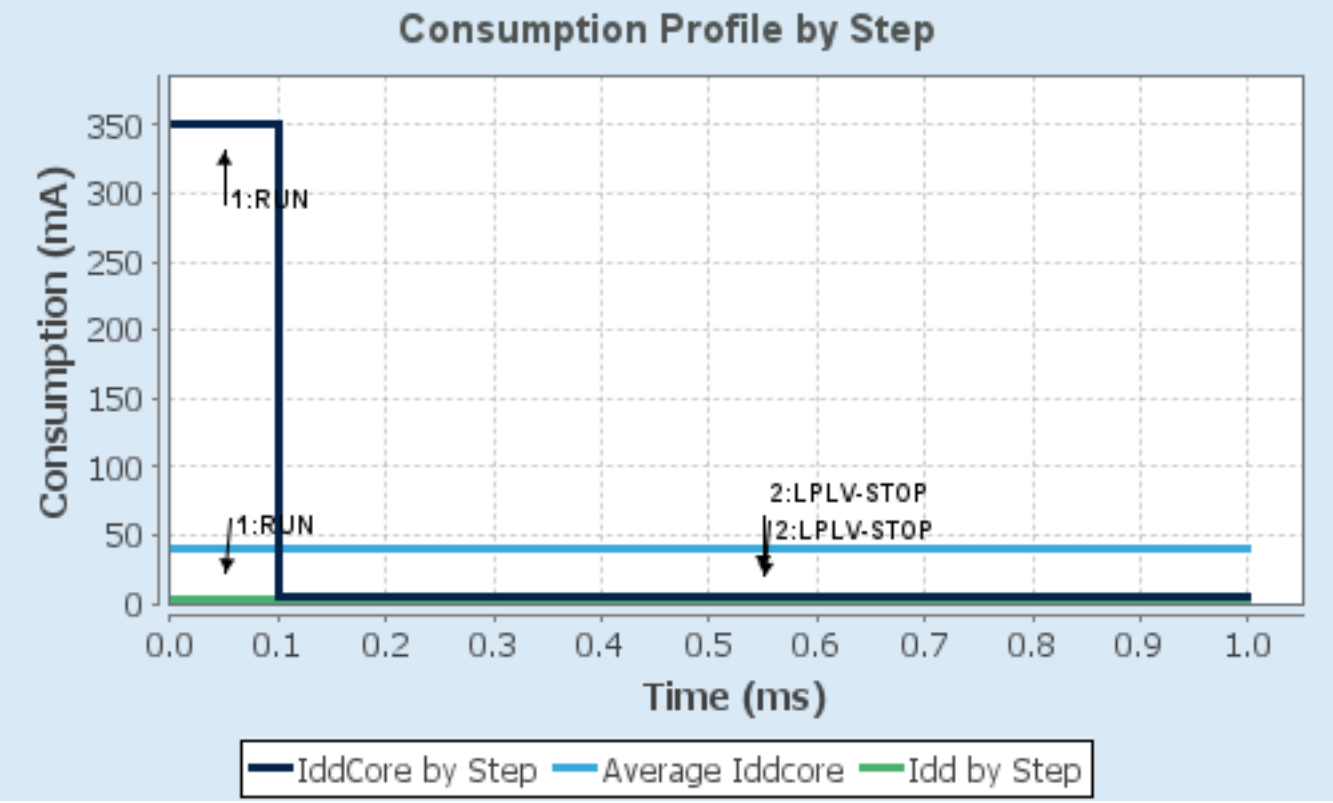
1.4. Sequence

Step	Step1	Step2
Mode	RUN	LPLV-STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Vdd Core	1.25	0.85
MPU0 Mode	P0RUN	P0STOP
MPU1 Mode	P1STOP	P1STOP
MCU Mode	CRUN	CSTOP
Fetch Type	SRAM	NA
MPU0 Frequency	648 MHz	0 Hz
Clock Configuration	HSE HSI LSI PLL ALL_IPs_ON_GPU_OFF	ALL CLOCKS OFF
MCU Frequency	210 MHz	0 Hz
AXI Frequency	264 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Idd Core	350 mA	6.05 mA
Idd	3.7 mA	0.83 mA
Duration	0.1 ms	0.9 ms
DMIPS	0.0	0.0
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	40.44 mA
Battery Life	1 month, 6 days, 15 hours	Average DMIPS	0.0 DMIPS

1.6. Chart


Consumption Profile by Step
Consumption (mA)
350
300
250
200
150
100
50
0
1:RUN
1:RUN
2:LPLV-STOP
2:LPLV-STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
IddCore by Step
Average Iddcore
Idd by Step

2. Peripherals and Middlewares Configuration

2.1. BSEC

mode: Activated

2.1.1. Core(s) Settings:

Context(s):	Cortex-A7 secure OS Cortex-A7 non secure OS
Initialized Context:	Cortex-A7 secure OS
Power Domain:	

2.2. DDR

DDR Type

DDR Type: DDR3 / DDR3L

Width

Width: 16bits

Density for DDR3(L) 16bits

Density for DDR3(L) 16bits: 4Gb

2.2.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 secure loader Cortex-A7 secure OS Cortex-A7 non secure OS
Initialized Context:	Cortex-A7 secure loader
Power Domain:	DDR subsystem frequency
400.0	Speed Bin Grade
DDR3-1066G / 8-8-8	Impedance During Read
Ron 40 ohm / ODT = 80 ohm (Default)	Impedance During Write
Ron 53 ohm / ODT = 60 ohm (Default)	Address Mapping configuration
Row - Bank - Column	Relaxed Timing mode
false	Temperature case over 85°C support
false	Burst Length (BL)
8	

2.2.2. DDR tuning:

Core(s) Settings:

Context(s):	Cortex-A7 secure loader Cortex-A7 secure OS Cortex-A7 non secure OS
Initialized Context:	Cortex-A7 secure loader
Power Domain:	

2.3. DEBUG

Debug: JTAG (5 pins)
mode: External Trigger Input
mode: External Trigger Output

2.3.1. Core(s) Settings:

Context(s):	Cortex-A7 non secure OS
Initialized Context:	Cortex-A7 non secure OS
Power Domain:	

2.4. ETH1

Mode: RGMII (Reduced GMII)
mode: ETH 125MHz Clock Input
mode: ETH Clock Output (PHY without Quartz)

2.4.1. Core(s) Settings:

Context(s):	Cortex-A7 non secure OS
Initialized Context:	Cortex-A7 non secure OS
Power Domain:	

2.5. ETZPC

mode: Activated

2.5.1. Memories Protection:

Core(s) Settings:

Context(s):	Cortex-A7 secure OS Cortex-A7 non secure OS Cortex-M4 FW
Initialized Context:	Cortex-A7 secure OS
Power Domain:	Configure Memory
Secure	Start Adress
0x00000000	Size
0x1000 *	Locking ROM
Unlock	Configure Memory
Secure	Start Adress
0x2FFE0000	Size
0x1000 *	Loking SYSRAM
Unlock	

2.5.2. Peripherals Protection:

Core(s) Settings:

Context(s):	Cortex-A7 secure OS Cortex-A7 non secure OS Cortex-M4 FW
Initialized Context:	Cortex-A7 secure OS
Power Domain:	VREFBUF
Read and Write Secure	LPTIM2
Read and Write Secure	LPTIM3
Read and Write Secure	LTDC
Read and Write Secure	DCMIPP
Read and Write Secure	USBPHYC
Read and Write Secure	DDRCTRL
Read and Write Secure	IWDG1
Read and Write Secure	STGENC
Read and Write Secure	USART1
Read and Write Secure	USART2
Read and Write Secure	SPI4
Read and Write Secure	SPI5
Read and Write Secure	I2C3
Read and Write Secure	I2C4

Read and Write Secure	I2C5
Read and Write Secure	TIM12
Read and Write Secure	TIM13
Read and Write Secure	TIM14
Read and Write Secure	TIM15
Read and Write Secure	TIM16
Read and Write Secure	TIM17
Read and Write Secure	ADC1
Read and Write Secure	ADC2
Read and Write Secure	OTG
Read and Write Secure	RNG
Read and Write Secure	HASH
Read and Write Secure	CRYP
Read and Write Secure	SAES
Read and Write Secure	PKA
Read and Write Secure	BKPSRAM
Read and Write Secure	ETH1
Read and Write Secure	ETH2
Read and Write Secure	SDMMC1
Read and Write Secure	SDMMC2
Read and Write Secure	MCE
Read and Write Secure	FMC
Read and Write Secure	QSPI
Read and Write Secure	SRAM1
Read and Write Secure	SRAM2
Read and Write Secure	SRAM3
Read and Write Secure	

2.5.3. Lock Peripherals:

Core(s) Settings:

Context(s):	Cortex-A7 secure OS Cortex-A7 non secure OS Cortex-M4 FW
Initialized Context:	Cortex-A7 secure OS
Power Domain:	VREFBUF
Unlock	LPTIM2
Unlock	LPTIM3
Unlock	LTDC
Unlock	DCMIPP
Unlock	USBPHYC

Unlock	DDRCTRL
Unlock	IWDG1
Unlock	STGENC
Unlock	USART1
Unlock	USART2
Unlock	SPI4
Unlock	SPI5
Unlock	I2C3
Unlock	I2C4
Unlock	I2C5
Unlock	TIM12
Unlock	TIM13
Unlock	TIM14
Unlock	TIM15
Unlock	TIM16
Unlock	TIM17
Unlock	ADC1
Unlock	ADC2
Unlock	OTG
Unlock	RNG
Unlock	HASH
Unlock	CRYP
Unlock	SAES
Unlock	PKA
Unlock	BKPSRAM
Unlock	ETH1
Unlock	ETH2
Unlock	SDMMC1
Unlock	SDMMC2
Unlock	MCE
Unlock	FMC
Unlock	QSPI
Unlock	SRAM1
Unlock	SRAM2
Unlock	SRAM3
Unlock	

2.6. GIC

2.6.1. Core(s) Settings:

Context(s):	Cortex-A7 secure OS

	Cortex-A7 non secure OS
Initialized Context:	Cortex-A7 secure OS
Power Domain:	

2.7. HDMI_CEC

mode: Activated

2.7.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 non secure OS
Initialized Context:	Cortex-A7 non secure OS
Power Domain:	Signal Free Time
2.5, 4 or 6 nominal data bit periods	Rx tolerance
Standard tolerance	Signal Free Time option
SFT timer starts when Transmission Start Of Message is set by software	Listening mode
Receive all messages	Logical address 0
Disable	Logical address 1
Disable	Logical address 2
Disable	Logical address 3
Disable	Logical address 4
Disable	Logical address 5
Disable	Logical address 6
Disable	Logical address 7
Disable	Logical address 8
Disable	Logical address 9
Disable	Logical address 10
Disable	Logical address 11
Disable	Logical address 12
Disable	Logical address 13
Disable	Logical address 14
Disable	Received data buffer name
cec_receive_buffer	Stop reception on bit rising error
Reception is stopped	Generate error bit on bit rising error
No error bit generation	Generate error bit on long bit period error
No error bit generation	Avoid error bit generation on error detection in broadcast
Error bit generation	

2.8. HSEM

mode: Activated

2.8.1. Core(s) Settings:

Context(s):	Cortex-A7 secure OS Cortex-A7 non secure OS Cortex-M4 FW
Initialized Context:	Cortex-A7 secure OS
Power Domain:	

2.9. I2C1

I2C: I2C

2.9.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 non secure OS
Initialized Context:	Cortex-A7 non secure OS
Power Domain:	Custom Timing
Disabled	I2C Speed Mode
Standard Mode	I2C Speed Frequency (KHz)
100	Rise Time (ns)
0	Fall Time (ns)
0	Coefficient of Digital Filter
0	Analog Filter
Enabled	Timing
0x10707DBC	Clock No Stretch Mode
Disabled	General Call Address Detection
Disabled	Primary Address Length selection
7-bit	Dual Address Acknowledged
Disabled	Primary slave address
0	

2.10. I2C4

I2C: SMBus-two-wire-Interface

2.10.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 non secure OS
Initialized Context:	Cortex-A7 non secure OS
Power Domain:	I2C Speed Mode
Standard Mode	I2C Speed Frequency (KHz)
100	Rise Time (ns)
0	Fall Time (ns)
0	Coefficient of Digital Filter
0	Analog Filter
Enabled	Timing
0x10707DBC	Packet Error Check Mode
PEC Disabled	Peripheral Mode
Peripheral Mode Smbus Slave	Clock No Stretch Mode
Disabled	General Call Address Detection
Disabled	Primary Address Length selection
7-bit	Dual Address Acknowledged
Disabled	Primary slave address
1	Extended Clock Timeout
Disabled	Idle Clock Timeout Detection
Disabled	Timeout Time (ns)
25000000	Timeout
0x0000830D	

2.11. I2S2

Mode: Master Half-Duplex Playback

2.11.1. Core(s) Settings:

Context(s):	Cortex-A7 non secure OS
Initialized Context:	Cortex-A7 non secure OS
Power Domain:	

2.12. LTDC

Display Type: RGB888 (24 bits)

2.12.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 non secure OS
Initialized Context:	Cortex-A7 non secure OS
Power Domain:	Horizontal Synchronization Width
8	Horizontal Back Porch
7	Active Width
640	Horizontal Front Porch
6	HSync Width
7	Accumulated Horizontal Back Porch Width
14	Accumulated Active Width
654	Total Width
660	Vertical Synchronization Height
4	Vertical Back Porch
2	Active Height
480	Vertical Front Porch
2	VSync Height
3	Accumulated Vertical Back Porch Height
5	Accumulated Active Height
485	Total Height
487	Horizontal Synchronization Polarity
Active Low	Vertical Synchronization Polarity
Active Low	Data Enable Polarity
Active Low	Pixel Clock Polarity
Normal Input	Red
0	Green
0	Blue
0	

2.12.2. Layer Settings:

Core(s) Settings:

Context(s):	Cortex-A7 non secure OS
Initialized Context:	Cortex-A7 non secure OS
Power Domain:	Layer 0 - Alpha
0	Layer 0 - Blue
0	Layer 0 - Green
0	Layer 0 - Red
0	Layer 1 - Alpha

0	Layer 1 - Blue
0	Layer 1 - Green
0	Layer 1 - Red
0	Number of Layers
2 layers	Layer 0 - Window Horizontal Start
0	Layer 0 - Window Horizontal Stop
0	Layer 0 - Window Vertical Start
0	Layer 0 - Window Vertical Stop
0	Layer 1 - Window Horizontal Start
0	Layer 1 - Window Horizontal Stop
0	Layer 1 - Window Vertical Start
0	Layer 1 - Window Vertical Stop
0	Layer 0 - Pixel Format
ARGB8888	Layer 1 - Pixel Format
ARGB8888	Layer 0 - Alpha constant for blending
0	Layer 0 - Blending Factor1
Alpha constant	Layer 0 - Blending Factor2
Alpha constant	Layer 1 - Alpha constant for blending
0	Layer 1 - Blending Factor1
Alpha constant	Layer 1 - Blending Factor2
Alpha constant	Layer 0 - Color Frame Buffer Start Adress
0	Layer 0 - Color Frame Buffer Line Length (Image Width)
0	Layer 0 - Color Frame Buffer Number of Lines (Image Height)
0	Layer 1 - Color Frame Buffer Start Adress
0	Layer 1 - Color Frame Buffer Line Length (Image Width)
0	Layer 1 - Color Frame Buffer Number of Lines (Image Height)
0	

2.13. PWR
mode: Wake-Up 1
mode: Wake-Up 3

2.13.1. Core(s) Settings:

Context(s):	Cortex-A7 secure OS Cortex-A7 non secure OS Cortex-M4 FW
Initialized Context:	Cortex-A7 secure OS
Power Domain:	

2.14. RCC

High Speed Clock (HSE): DIGBYPASS Clock Source

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

2.14.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 ROM code Cortex-A7 secure loader Cortex-A7 secure OS Cortex-A7 non secure OS Cortex-M4 FW
Initialized Context:	Cortex-A7 ROM code
Power Domain:	PLL1 CSG mode
DISABLED	PLL2 CSG mode
DISABLED	PLL3 CSG mode
DISABLED	PLL4 CSG mode
DISABLED	TIM Group1 Prescaler Selection
Disabled	TIM Group2 Prescaler Selection
Disabled	HSE Startup Timout Value (ms)
100	LSE Startup Timout Value (ms)
5000	LSE Drive Capability
LSE oscillator medium high drive capability	VDD voltage (V)
3.3	User defined configuration
FALSE	

2.15. RTC

mode: Activate Clock Source

2.15.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 secure OS Cortex-A7 non secure OS
Initialized Context:	Cortex-A7 secure OS
Power Domain:	Hour Format

Hourformat 24	Asynchronous Predivider value
127	Synchronous Predivider value
255	

2.16. SDMMC2

Mode: MMC 8 bits Wide bus

2.16.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 non secure OS
Initialized Context:	Cortex-A7 non secure OS
Power Domain:	Clock transition on which the bit capture is made
Rising transition	SDMMC Clock output enable when the bus is idle
Disable the power save for the clock	SDMMC hardware flow control
The hardware control flow is disabled	SDMMCCLK clock divide factor
0	

2.17. SYS

Timebase Source: SysTick

2.17.1. Core(s) Settings:

Context(s):	Cortex-M4 FW
Initialized Context:	Cortex-M4 FW
Power Domain:	

2.18. TAMP

mode: Activated

2.18.1. Core(s) Settings:

Context(s):	Cortex-A7 ROM code Cortex-A7 secure loader Cortex-A7 secure OS Cortex-A7 non secure OS
Initialized Context:	

	Cortex-A7 ROM code
Power Domain:	

2.19. UART4

Mode: Asynchronous

2.19.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 non secure OS
Initialized Context:	Cortex-A7 non secure OS
Power Domain:	Baud Rate
115200	Word Length
8 Bits (including Parity)	Parity
None	Stop Bits
1	Data Direction
Receive and Transmit	Over Sampling
16 Samples	Single Sample
Disable	ClockPrescaler
1	Fifo Mode
FIFO mode disable	Txfifo Threshold
1 eighth full configuration	Rxfifo Threshold
1 eighth full configuration	Auto Baudrate
Disable	TX Pin Active Level Inversion
Disable	RX Pin Active Level Inversion
Disable	Data Inversion
Disable	TX and RX Pins Swapping
Disable	Overrun
Enable	DMA on RX Error
Enable	MSB First
Disable	

2.20. USBH_HS1

mode: USB Host controller

2.20.1. Core(s) Settings:

Context(s):	Cortex-A7 non secure OS
Initialized Context:	

	Cortex-A7 non secure OS
Power Domain:	

2.21. USB_OTG_HS

High Speed: OTG/Dual_Role_Device

mode: Activate_VBUS

2.21.1. Core(s) Settings:

Context(s):	Cortex-A7 non secure OS
Initialized Context:	Cortex-A7 non secure OS
Power Domain:	

*** User modified value**

3. System Configuration

3.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
DDR	DDR_RESETN	DDR_RESETN	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_A7	DDR_A7	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_DQ3	DDR_DQ3	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_DQ0	DDR_DQ0	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_A13	DDR_A13	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_DQ1	DDR_DQ1	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_A9	DDR_A9	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_DQ7	DDR_DQ7	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_DQS0P	DDR_DQS0P	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_DQS0N	DDR_DQS0N	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_A5	DDR_A5	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_DQ2	DDR_DQ2	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_DQ6	DDR_DQ6	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_DQM0	DDR_DQM0	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
	DDR_A2	DDR_A2	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_DQ4	DDR_DQ4	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_DQ5	DDR_DQ5	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_DTO0	DDR_DTO0	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_A3	DDR_A3	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_ZQ	DDR_ZQ	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_A0	DDR_A0	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_DTO1	DDR_DTO1	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_ODT	DDR_ODT	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_BA0	DDR_BA0	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_WEN	DDR_WEN	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_BA2	DDR_BA2	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_CSN	DDR_CSN	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_CASN	DDR_CASN	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_RASN	DDR_RASN	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_CLKP	DDR_CLKP	n/a	n/a	n/a		Cortex-A7 secure loader*	Cortex-A7 secure loader*

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
							Cortex-A7	Cortex-A7
	DDR_CLKN	DDR_CLKN	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_A1	DDR_A1	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_A12	DDR_A12	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_A11	DDR_A11	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_A14	DDR_A14	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_A10	DDR_A10	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_CKE	DDR_CKE	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_DQ8	DDR_DQ8	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_DQ10	DDR_DQ10	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_DQ13	DDR_DQ13	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_BA1	DDR_BA1	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_DQ9	DDR_DQ9	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_DQS1P	DDR_DQS1P	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_DQS1N	DDR_DQS1N	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_A4	DDR_A4	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
	DDR_DQM1	DDR_DQM1	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_A6	DDR_A6	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_DQ11	DDR_DQ11	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_DQ14	DDR_DQ14	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_DQ12	DDR_DQ12	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_ATO	DDR_ATO	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_A8	DDR_A8	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_DQ15	DDR_DQ15	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
	DDR_VREF	DDR_VREF	n/a	n/a	n/a		Cortex-A7 secure loader* Cortex-A7	Cortex-A7 secure loader* Cortex-A7
DEBUG	JTDO-TRACESWO	DEBUG_JTDO-SWO	n/a	n/a	n/a		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	JTDI	DEBUG_JTDI	n/a	n/a	n/a		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	NJTRST	DEBUG_JTRST	n/a	n/a	n/a		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	JTCK-SWCLK	DEBUG_JTCK-SWCLK	n/a	n/a	n/a		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	JTMS-SWDIO	DEBUG_JTMS-SWDIO	n/a	n/a	n/a		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PA13	DEBUG_DBTRGI	n/a	n/a	n/a		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PA14	DEBUG_DBTRGO	n/a	n/a	n/a		Cortex-A7 non secure OS	Cortex-A7 non secure OS
ETH1	PH7	ETH1_RXD3	Alternate function	No pull-up and no pull-down	n/a		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PE2	ETH1_TXD3	Alternate Function Push Pull	No pull-up and no pull-down	High		Cortex-A7 non secure OS	Cortex-A7 non secure OS

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
	PC2	ETH1_TXD2	Alternate Function Push Pull	No pull-up and no pull-down	High		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PG5	ETH1_CLK125	Alternate Function Push Pull	No pull-up and no pull-down	High		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PB5	ETH1_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PG14	ETH1_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	High		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PG13	ETH1_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	High		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PA1	ETH1_RX_CLK	Alternate function	No pull-up and no pull-down	n/a		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PC1	ETH1_MDC	Alternate Function Push Pull	No pull-up and no pull-down	High		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PB11	ETH1_TX_CTL	Alternate Function Push Pull	No pull-up and no pull-down	High		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PG4	ETH1_GTX_CLK	Alternate Function Push Pull	No pull-up and no pull-down	High		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PB0	ETH1_RXD2	Alternate function	No pull-up and no pull-down	n/a		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PC5	ETH1_RXD1	Alternate function	No pull-up and no pull-down	n/a		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PA7	ETH1_RX_CTL	Alternate function	No pull-up and no pull-down	n/a		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PA2	ETH1_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PC4	ETH1_RXD0	Alternate function	No pull-up and no pull-down	n/a		Cortex-A7 non secure OS	Cortex-A7 non secure OS
HDMI_CEC	PB6	CEC	Alternate Function Open Drain	No pull-up and no pull-down	Low		Cortex-A7 non secure OS	Cortex-A7 non secure OS
I2C1	PF15	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PF14	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low		Cortex-A7 non secure OS	Cortex-A7 non secure OS
I2C4	PD12	I2C4_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PD13	I2C4_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low		Cortex-A7 non secure OS	Cortex-A7 non secure OS
I2S2	PA9	I2S2_CK	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PI3	I2S2_SDO	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PB12	I2S2_WS	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-A7 non secure OS	Cortex-A7 non secure OS
LTDC	PH15	LTDC_G4	Alternate Function	No pull-up and no pull-	Low		Cortex-A7 non	Cortex-A7 non

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
			Push Pull	down			secure OS	secure OS
	PH12	LTDC_R6	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PD10	LTDC_B3	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PI0	LTDC_G5	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PH10	LTDC_R4	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PH14	LTDC_G3	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PH9	LTDC_R3	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PE6	LTDC_G1	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PH13	LTDC_G2	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PE15	LTDC_R7	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PH8	LTDC_R2	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PI2	LTDC_G7	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PI1	LTDC_G6	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PI4	LTDC_B4	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PI9	LTDC_VSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PD9	LTDC_B0	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PD8	LTDC_B7	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PG12	LTDC_B1	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PI10	LTDC_HSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PA3	LTDC_B5	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PF10	LTDC_DE	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PH3	LTDC_R1	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PB1	LTDC_G0	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure OS	Cortex-A7 non secure OS

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
	PH2	LTDC_R0	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PC0	LTDC_R5	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PB8	LTDC_B6	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PG10	LTDC_B2	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PG7	LTDC_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-A7 non secure OS	Cortex-A7 non secure OS
PWR	PC13	PWR_WKUP3	n/a	n/a	n/a		Cortex-A7 secure OS* Cortex-A7 non	Cortex-A7 secure OS* Cortex-A7 non
	PA0	PWR_WKUP1	n/a	n/a	n/a		Cortex-A7 secure OS* Cortex-A7 non	Cortex-A7 secure OS* Cortex-A7 non
RCC	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a		Cortex-A7 ROM code* Cortex-A7	Cortex-A7 ROM code* Cortex-A7
	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a		Cortex-A7 ROM code* Cortex-A7	Cortex-A7 ROM code* Cortex-A7
	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a		Cortex-A7 ROM code* Cortex-A7	Cortex-A7 ROM code* Cortex-A7
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a		Cortex-A7 ROM code* Cortex-A7	Cortex-A7 ROM code* Cortex-A7
SDMMC2	PG6	SDMMC2_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PB3	SDMMC2_D2	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PA8	SDMMC2_D4	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PB9	SDMMC2_D5	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PC7	SDMMC2_D7	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PB15	SDMMC2_D1	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PB4	SDMMC2_D3	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PE3	SDMMC2_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PE5	SDMMC2_D6	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-A7 non secure OS	Cortex-A7 non secure OS

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
	PB14	SDMMC2_D0	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-A7 non secure OS	Cortex-A7 non secure OS
UART4	PG11	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	PB2	UART4_RX	Alternate function	No pull-up and no pull-down	n/a		Cortex-A7 non secure OS	Cortex-A7 non secure OS
USBH_HS1	USB_DM1	USBH_HS1_DM	n/a	n/a	n/a		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	USB_DP1	USBH_HS1_DP	n/a	n/a	n/a		Cortex-A7 non secure OS	Cortex-A7 non secure OS
USB_OTG_HS	PA10	USB_OTG_HS_ID	Analog mode	n/a	n/a		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	USB_DM2	USB_OTG_HS_DM	n/a	n/a	n/a		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	USB_DP2	USB_OTG_HS_DP	n/a	n/a	n/a		Cortex-A7 non secure OS	Cortex-A7 non secure OS
	OTG_VBUS	USB_OTG_HS_VBUS	n/a	n/a	n/a		Cortex-A7 non secure OS	Cortex-A7 non secure OS
GPIO	PG1	GPIO_EXTI1	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	HDMI_INT	Cortex-A7 non secure OS Cortex-M4 FW	Cortex-A7 non secure OS Cortex-M4 FW
	PA6	GPIO_EXTI6	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	ETH_MDINT	Cortex-A7 non secure OS Cortex-M4 FW	Cortex-A7 non secure OS Cortex-M4 FW
	PE8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	HDMI_NRST	Cortex-A7 non secure OS Cortex-M4 FW	Cortex-A7 non secure OS Cortex-M4 FW

* Initialized context

3.2. DMA configuration

nothing configured in DMA service

3.3. MDMA configuration

nothing configured in DMA service

3.4. NVIC configuration

3.4.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	1	0
Pre-fetch fault, memory access fault	true	1	0
Undefined instruction or illegal state	true	1	0
System service call via SWI instruction	true	1	0
Debug monitor	true	1	0
Pendable request for system service	true	1	0
System tick timer	true	15	0
RCC global interrupt	unused		
EXTI line1 interrupt	unused		
EXTI line6 interrupt	unused		
FPU global interrupt	unused		
HSEM interrupt 2	unused		
Cortex-A7 send event interrupt through EXTI line 66	unused		
RCC wake-up interrupt	unused		

3.4.2. NVIC Code generation

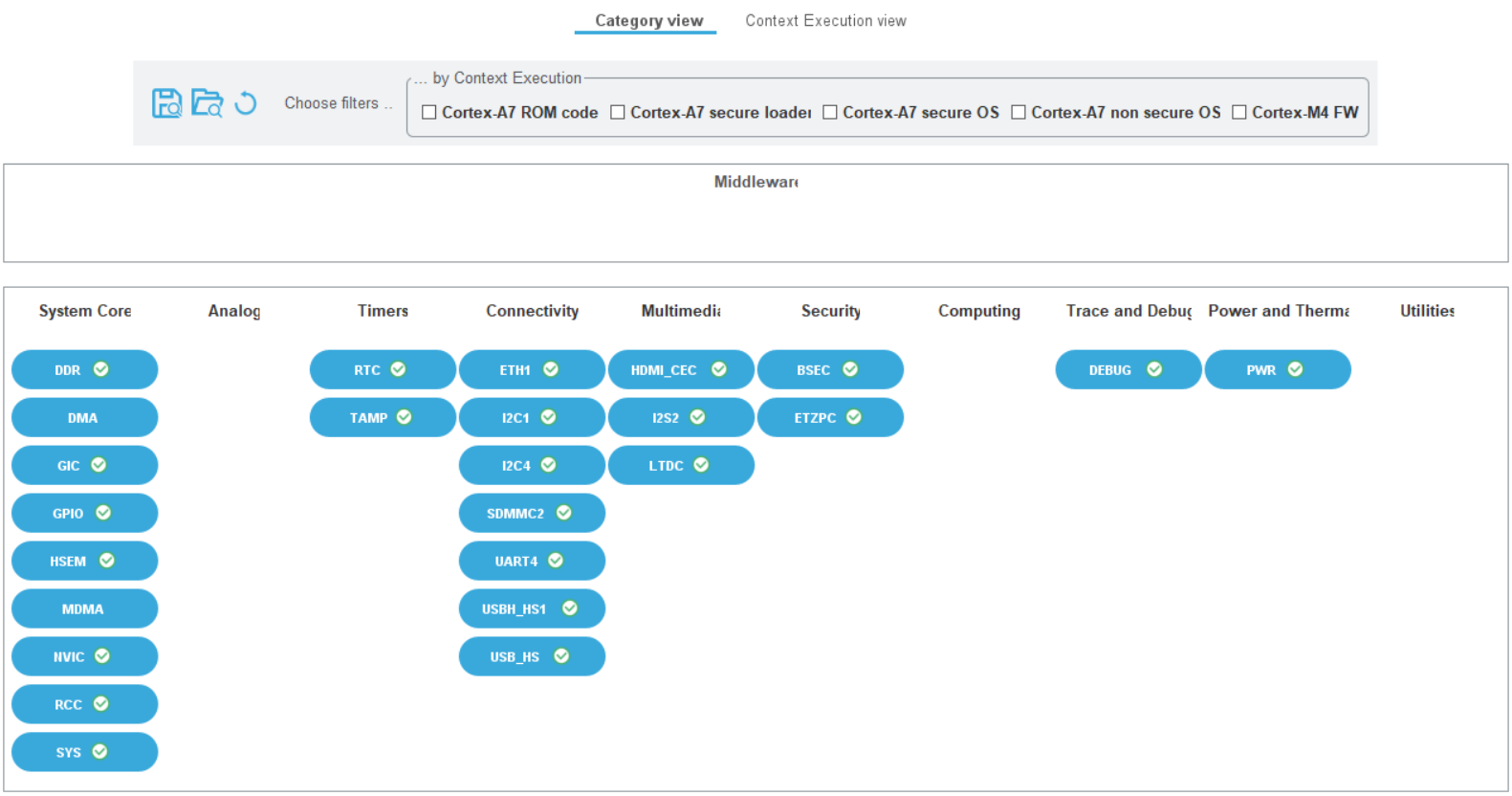
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

*** User modified value**

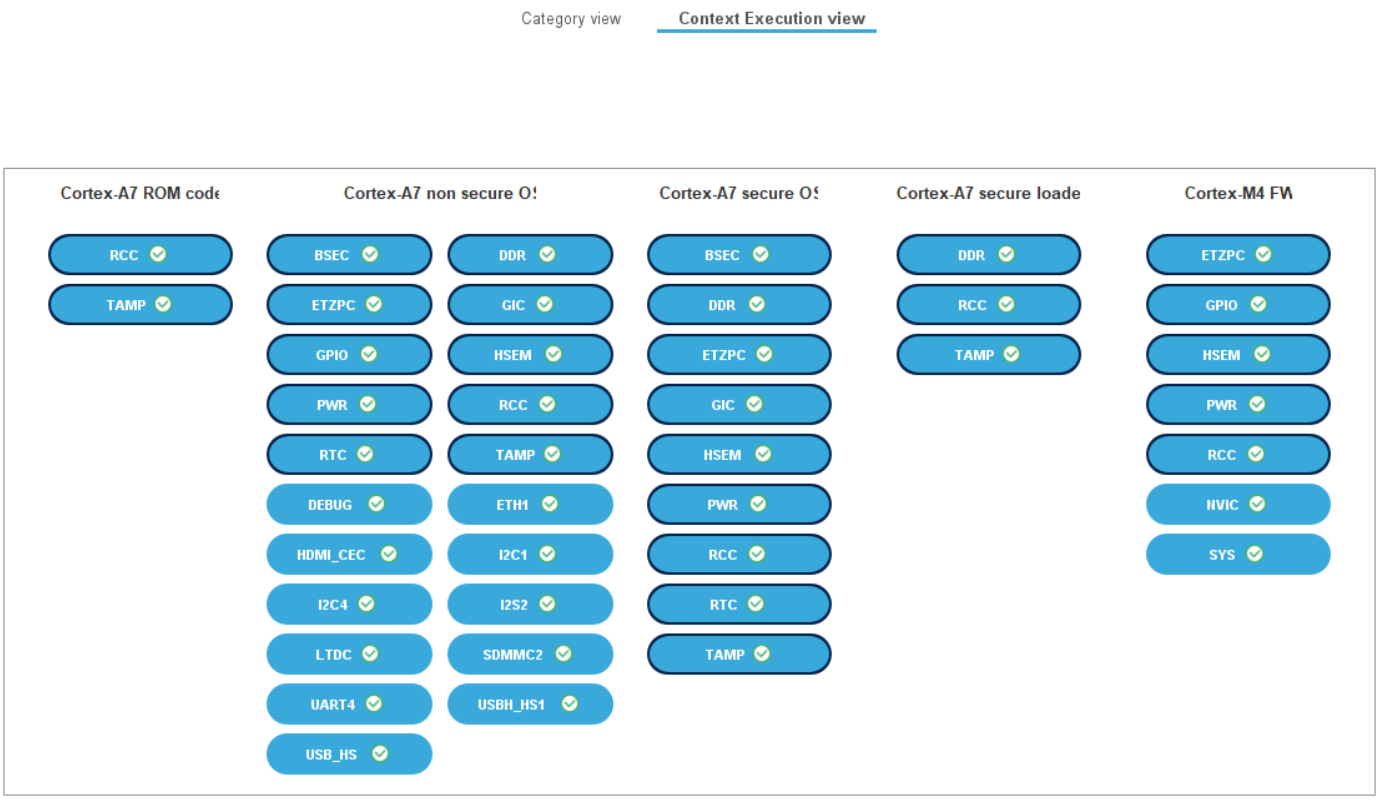
4. System Views

4.1. Category view

4.1.1. Current



4.2. Context Execution view



5. Docs & Resources

Type	Link
BSDL files	https://www.st.com/resource/en/bsdl_model/en-stm32mp1xx-bsdl-v4-0.zip
HW Models	https://www.st.com/resource/en/hw_model/stm32mp15x-series-ddr-memory-routing-guidelines-examples.zip
IBIS models	https://www.st.com/resource/en/ibis_model/stm32mp15x-ibis.zip
System View Description	https://www.st.com/resource/en/svd/stm32mp1_lauterbach_trace_script.zip
System View Description	https://www.st.com/resource/en/svd/stm32mp1_svd.zip
Presentations	https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32mp1_press-pres.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32trust-product-overview.pdf
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32mp13.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32mp15.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2639-soldering-recommendations-and-package-information-for-leadfree-ecopack-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2867-oscillator-design-guide-for-stm8afals-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an3126-audio-and-waveform-generation-using-the-dac-in-stm32-products-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4803-highspeed-si-

	simulations-using-ibis-and-boardlevel-simulations-using-hyperlynx-si-on-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5027-interfacing-pdm-digital-microphones-using-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5031-getting-started-with-stm32mp151-stm32mp153-and-stm32mp157-line-hardware-development-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5109-stm32mp15x-lines-using-lowpower-modes-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5122-stm32mp1-series-ddr-memory-routing-guidelines-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5224-stm32-dmamux-the-dma-request-router-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5253-migrating-from-stm32f469479-line-to-stm32mp151-stm32mp153-and-stm32mp157-lines-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5256-stm32mp151-stm32mp153-and-stm32mp157-discrete-power-supply-hardware-integration-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5260-stm32mp151153157-mpu-lines-and-stpmic1-integration-on-a-battery-powered-application-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5275-usb-dfuusart-protocols-used-in-stm32mp1-series-bootloaders-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5284-stm32mp1-series-system-power-consumption-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5438-stm32mp1-series-lifetime-estimates-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5510-overview-of-the-secure-secret-provisioning-ssp-on-stm32mp1-series-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5543-enhanced-methods-to-handle-spi-communication-on-stm32-devices-

	stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4760-quadspi-interface-on-stm32-microcontrollers-and-microprocessors--stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5612-esd-protection-of-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5089-stm32mp151153157-mpu-lines-and-stpmic1-integration-on-a-wall-adapter-supply-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5348-introduction-to-fdcan-peripherals-for-stm32-product-classes-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4230-random-number-generation-validation-using-nist-statistical-test-suite-for-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5168-how-to-configure-ddr-on-stm32mp1-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5475-migration-of-applications-from-stm32mp15x-lines-to-stm32mp13x-lines-microprocessor-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5827-guidelines-for-entering-rma-state-on-stm32mp1-series-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5225-introduction-to-usb-typec-power-delivery-for-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5816-how-to-build-stm32-lpbam-application-using-stm32cubemx-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5036-guidelines-for-thermal-management-on-stm32-applications-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/dm00693021-stm32mp15x-series-interfacing-with-a-mipi-csi2-camera-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5690-how-to-use-vrefbuf-peripheral-on-stm32-mcus-and-mpus-stmicroelectronics.pdf

Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5418-how-to-build-a-simple-usbpd-sink-application-with-stm32cubemx-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5426-migrating-graphics-middleware-projects-from-stm32cubemx-540-to-stm32cubemx-550-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5698-adapting-the-xcubestl-functional-safety-package-for-stm32-iec-61508-compliant-to-other-safety-standards-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5731-stm32cubemx-and-stm32cubeide-threadsafe-solution-stmicroelectronics.pdf
Errata Sheets	https://www.st.com/resource/en/errata_sheet/es0438-stm32mp151x3x7x-device-errata-stmicroelectronics.pdf
Datasheet	https://www.st.com/resource/en/datasheet/dm00489382.pdf
Programming Manuals	https://www.st.com/resource/en/programming_manual/pm0214-stm32-cortexm4-mcus-and-mpus-programming-manual-stmicroelectronics.pdf
Reference Manuals	https://www.st.com/resource/en/reference_manual/rm0441-stm32mp151-advanced-armbased-32bit-mpus-stmicroelectronics.pdf
Technical Notes & Articles	https://www.st.com/resource/en/technical_note/tn1433-reference-device-marking-schematics-for-stm32-microcontrollers-and-microprocessors-stmicroelectronics.pdf
Technical Notes & Articles	https://www.st.com/resource/en/technical_note/tn1489-security-bulletin-tn1489stpsirt-physical-attacks-on-stm32-and-stm32cube-firmware-stmicroelectronics.pdf
User Manuals	https://www.st.com/resource/en/user_manual/um2714-stm32mp1-series-safety-manual-stmicroelectronics.pdf
User Manuals	https://www.st.com/resource/en/user_manual/um3190-stm32mp1-series-ulcsaiec-607301603351-selftest-library-user-guide-stmicroelectronics.pdf