A High Performance Hearing Aid System with Fully Programmable Ultra Low Power DSP

Yunseo Ku[(1)], Junil Sohn[(1)], Jonghee Han[(1)], Yonghyun Baek[(2)] and Dongwook Kim[(1)]
(1) Samsung Advanced Institute of Technology, Samsung Electronics, Yongin, Korea
(2) Division of Computer & Telecomm. Eng, Yonsei University, Wonju, Korea

***Abstract*-- This paper presents the design of fully programmable digital signal processor for the hearing aid system and optimized implementation of digital hearing aid algorithms. The average performance of the developed processor is measured by performing Fast Fourier Transform (FFT) algorithm. The proposed applications such as variable multi-band loudness compensation algorithm with wide dynamic range compression and sub-band based adaptive feedback cancellation algorithm are optimized for real-time processing by exploiting the data and instruction parallelism of the developed processor. The results show that the computational ability and power consumption of the developed processor are suitable to use for the hearing aid system. The optimization achieves that the computational time to perform the full applications on the processor takes only under 40% of the constraint for real-time processing.**

I. INTRODUCTION

Digital hearing aids require low power consumption and high computation performance at the same time due to limited battery capacity and signal processing complexity. As modern hearing aids are getting smaller for cosmetic matter, it becomes hard to use the bigger sized battery which has enough capacity to process complex hearing aid algorithms. [1] Therefore, the performance of digital signal processor (DSP) in the hearing aids and the algorithm optimization play a major role to fully exploit the benefits from sophisticated hearing aid algorithms. Flexibility and programmability of the processor are also significant because the applied algorithms in the hearing aids vary based on different types of the hearing impaired and their ambient environment. [2] In order to achieve the low power consumption and small size of chip area, the fixed-point DSP is generally used in digital hearing aids since the fixed-point hardware is much simpler than floating-point hardware. [3] When implementing signal processing algorithms on the fixed-point DSP, however, the careful optimization process is needed to minimize quantization error and to avoid overflow/underflow. [4] This paper concerns not only the development of low power fixed-point DSP for the hearing aids but also the hearing aid algorithm optimization.

II. DIGITAL SIGNAL PROCESSOR FOR HEARING AID

A 16/32-bit customized low power programmable DSP is designed to perform the hearing aid algorithms and to meet low power consumption requirement. Memory data path size and instruction-set are customized by the simulation when performing signal processing algorithms such as Fast Fourier Transform (FFT), which is mostly applied to hearing aid algorithms. The simulation result shows that maximum 128-bit data vector processing with twelve 16-bit multipliers is most suitable for the hearing aid system in the view of the computational ability and the power consumption. Fig.1 shows the overall architecture of developed processor which includes the low power SRAM and the peripherals such as SPI and I2S.

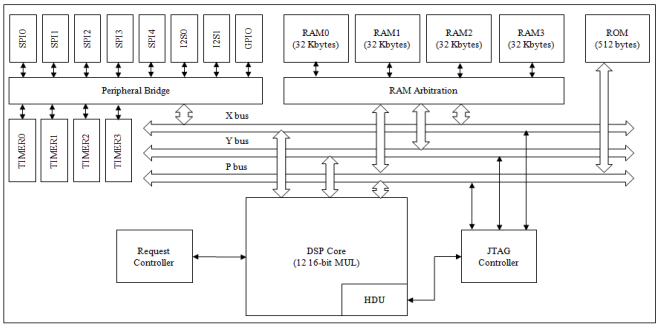

Fig.1. Proposed Digital Signal Processor for Hearing Aids

In order to evaluate the performance of developed DSP in the view of the computational ability and the power consumption, the required cycles for 256-point radix-4 FFT is profiled by the simulator and the power consumption for DSP core when computing FFT infinitely is measured on the test board which has the developed DSP chips on it. The average computational ability of the DSP core can be measured by calculating total operations to perform FFT and the number of required cycles to execute FFT. The number of required cycles of proposed processor is 900 while other low power processors need more than 3K cycles as shown in Table I. [5]

TABLE I
COMPARISON OF NUMBER OF CLOCK CYCLES FOR 256 FFT

Processor	Required Cycles
Blackfin BF531 (Analog Devices)	3.2K
CoolFlux DSP (NXP)	5.5K
LSI403LP (LSI Logic)	5K
Proposed DSP	**0.9K**

The number of operations of proposed processor is 15,000, which leads that the average number of operations is 16.7 per cycle. The measured power consumption for DSP core is 935uA at 0.9V supply voltage and 8.25MHz operating clock frequency. These lead that the number of million operations

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per one second (MOPS) per one milliwatt (mW) is 163, which can be considered as the average performance of developed DSP in this work.

III. HEARING AID ALGORITHM OPTIMIZATION

Due to smaller hearing dynamic range of the hearing impaired, the proper gains should be applied to the input signal according to input signal intensity and hearing loss level of each frequency band. The FFT filter bank is used to split frequency bands of the input signal according to the critical band frequency scale of the human auditory system. Thanks to the programmability of the developed DSP, variable band number processing (up to 64) can be performed according to the different hearing characteristics. Fig.2 shows that the variable band architecture compensates the hearing loss more accurately than the fixed band architecture.

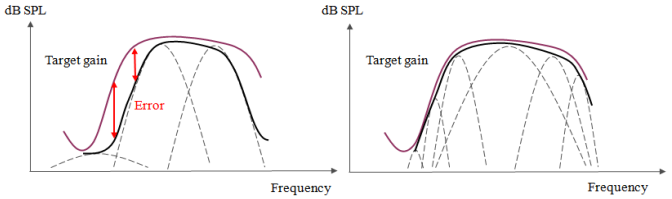

Fig.2. Compensation Error Difference between the Fixed & Variable Band Architecture

In each band, the band energy of input signal is calculated and then the proper gain is determined based on the loudness scaling function and the calculated current band energy. The determined gains are applied the analysis output and the compensated output are synthesized through inverse FFT filter bank. Due to very close distance between the microphone and the loudspeaker in the hearing aids, the acoustic feedback is prone to occur when the sound from the loudspeaker loops back through the microphone. The acoustic feedback limits the maximum gain and degrades the sound quality of the hearing aids. In this work, the sub-band based adaptive feedback cancellation algorithm is adopted in order to integrate with the multi-band loudness compensation algorithm in the frequency domain. Fig.3 shows the block diagram of multi-band loudness compensation algorithm with sub-band based adaptive feedback cancellation algorithm.

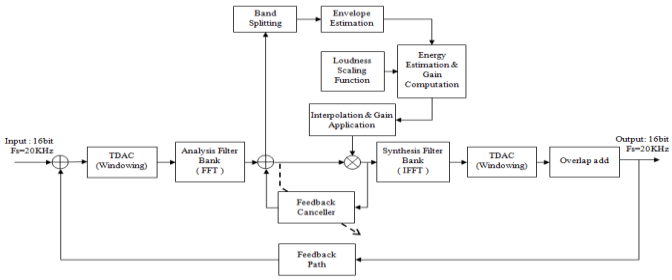

Fig.3. Multi-Band Wide Dynamic Range Compression & Sub-Band based Adaptive Feedback Cancellation Algorithm

In order to optimize critical functions down to the assembly language level, the candidate functions are identified to perform the parallelism in the view of data level and instruction level. To reduce the number of loop iterations, single instruction-multi data instructions are applied to perform 64-bit to 128-bit vector data processing. Instruction level parallelism for reducing the code lines is also performed by avoiding or tolerating the instruction latency. Moreover, reconfigurable addressing instructions are used for specialized addressing such as the bit-reversed addressing for FFT processing. For the real time implementation, maximum 51,200 cycles are allowed for the algorithm computation under the condition of 8MHz operating clock frequency, 256-point FFT, half overlapping and 20KHz sampling frequency. After the optimization procedure, the total computational load of both algorithms is 37.5% as shown in Table II. Even for the maximum band number case (64 bands), the computational load is only 46.1%.

TABLE II
THE NUMBER OF CYCLES FOR HEARING AID ALGORITHMS

Algorithm Type	Required Cycles	Computational Load (%)
Multi-Band Wide Dynamic Range Compression (8 bands) & Sub-Band based Adaptive Feedback Cancellation	19,199	37.5
Multi-Band Wide Dynamic Range Compression (64 bands)	23,621	46.1

IV. CONCLUSION

Fully programmable ultra low power DSP for the hearing aid system is developed and two main hearing aid algorithms are optimized for real-time processing. The results show that the computational efficiency of the developed processor is suitable to use for digital hearing aids. The power consumption may be further decreased by modifying the operating clock frequency. Moreover, further software optimizing also would allow further decreasing the power consumption.

ACKNOWLEDGMENT

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