AN ULTRA-LOW POWER ANALOGUE DIRECTIONALITY SYSTEM FOR DIGITAL HEARING AIDS

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ABSTRACT

An ultra-low power analogue system used to provide adaptive directionality in hearing aids is proposed. A digital algorithm converted to analogue is shown to be considerably more power efficient. Power reduction is obtained by designing all the circuit blocks in a CMOS technology using transistors in weak inversion. The system performs comparably to a digital equivalent in terms of the algorithm but with a total power consumption of *5 μW* at a power supply voltage of *900 mV*.

1. INTRODUCTION

Processing abilities of hearing aids, as with many small bio-medical devices, is often limited by power consumption. The small physical dimensions of such devices place limitations on battery power. Therefore, more efficient means of using the available power are required.

Directionality or beamforming systems are used in high quality digital hearing aids. Two microphones are placed a short distance apart providing the hearing aid with stereophonic hearing. Adaptive systems allow the hearing aids to focus in the direction of greatest signal to noise ratio thus improving the perceived intelligibility [1].

This paper demonstrates an analogue directionality system that leads to a two fold power saving. The directionality system implemented in analogue itself consumes less power. Also, by placing a single ADC after the analogue directionality system rather than two before a digital directionality system, the power consumption for analogue to digital conversion is reduced.

2. THE ALGORITHM

A block diagram of the digital adaptive directionality system [2] may be seen in figure 1 with table 1 as key. *f(n)* and *b(n)* are the inputs that originate from omni-directional front and back microphones, respectively (n being the sample number). By delaying one of these inputs and subtracting from the other, directionality is achieved. This is in the form of two cardioid signals, *x(n)* and *y(n)* which are shown in figures 2(a) and 2(b) respectively.

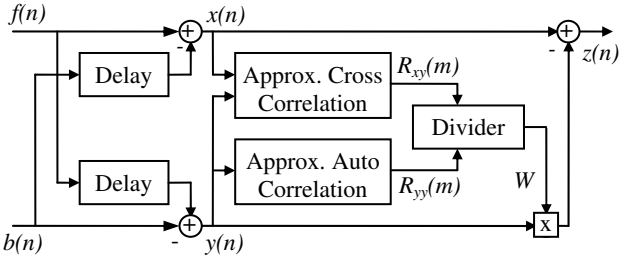

Fig. 1: *Block diagram of the digital system*

Variable	Meaning
f(n)	Front microphone input (omni-directional)
b(n)	Back microphone input (omni-directional)
x(n)	Forward facing signal (cardioid)
y(n)	Backward facing signal (cardioid)
R_{xy}	Approximation of cross-correlation
R_{yy}	Approximation of auto-correlation of y(n)
W	Adaptive weight
z(n)	Output signal

Tab. 1: *Definition of variables*

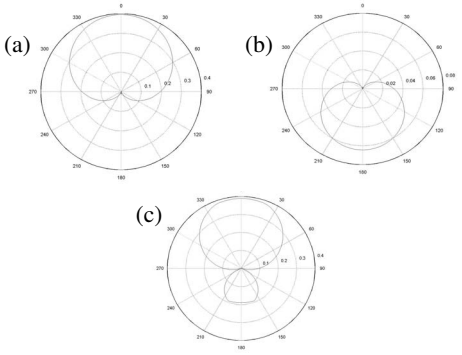

Fig. 2: *The angle dependence of: (a) signal x(n); (b) signal y(n); (c) signal z(n) with W = 0.33.*

By multiplying a weight, *W*, with *y(n)* and subtracting from *x(n)*, the null direction may be varied. An adaptive weight of *W = 0.33* places the null at an angle of *120* degrees as in figure 2(c). With an adaptive system altering the weight, this null may be placed in the

direction of greatest noise. Taking approximate correlations $R_{xy}(m)$ and $R_{yy}(m)$ (eq. (1) and (2), respectively) and dividing provides an estimate of the optimum solution (Wiener solution), eq.(3) [2]. α and β are constants such that $\alpha + \beta = 1$ where $\alpha > 0$ and $\beta > 0$. A frame based system is used where m is frame number and n the data sample number, M data samples per frame.

$$R_{xy}(m) = \frac{\alpha}{M}\sum_{n=0}^{M-1} x(n)\,y(n) + \beta R_{xy}(m-1) \quad (1)$$

$$R_{yy}(m) = \frac{\alpha}{M}\sum_{n=0}^{M-1} y^2(n) + \beta R_{yy}(m-1) \quad (2)$$

$$W_{opt}(m) = \frac{R_{xy}(m)}{R_{yy}(m)} \quad (3)$$

3. CONVERSION TO CONTINUOUS TIME

A block diagram of the continuous time system may be seen in figure 3. This proposed system provides, in analogue, equivalent processing to that of the digital system. Each system block is converted from a discrete time implementation to a continuous time version. Multipliers, dividers and summation blocks use direct analogue equivalent multiplying, dividing and summing circuits. The delay elements are replaced with allpass filters and the correlators with appropriate circuits as discussed in section 3.2.

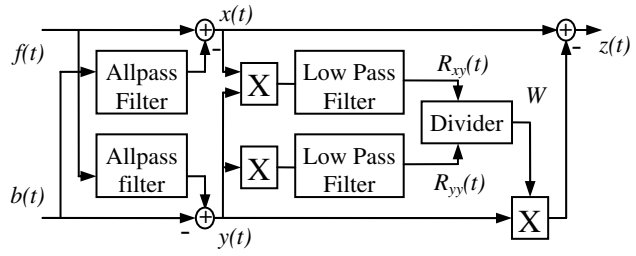

Fig. 3: *The proposed analogue system*

3.1. Delay elements

The delay blocks, figure 1, have short delays of the time taken for sound to travel the distance between microphones. For microphones *10 mm* apart, this time is approximately *30 μs*. These are realised in the continuous domain as second order allpass filters with maximally flat group delay. The transfer function, *T(s)*, is given by

$$T(s) = \frac{s^2 - (\omega_0/Q)s + \omega_0^2}{s^2 + (\omega_0/Q)s + \omega_0^2}. \quad (4)$$

Where $\omega_o/Q = 2.1\times10^5$ and $\omega_o = 1.44\times10^8$.

3.2. Correlators

Considering eq.(1) and (2) which offer approximations to cross and auto correlation respectively, it is possible to construct a generic equation for the correlators,

$$v(m) = \frac{\alpha}{M}\sum_{n=0}^{M-1} t(n) + \beta v(m-1) \quad (5)$$

Where $t(n) = x(n).y(n)$ and $v(m) = R_{xy}(m)$ for cross-correlation or $t(n) = y^2(n)$ and $v(m) = R_{yy}(m)$ for auto-correlation.

A further substitution yields

$$v(m) = \alpha u(m) + \beta v(m-1) \quad (6)$$

where

$$u(m) = \frac{1}{M}\sum_{n=0}^{M-1} t(n) \quad (7)$$

Therefore $v(m)$ is a first order infinite-impulse-response (*IIR*) process at the frame sample (m) rate. This is considerably slower than the data sample (n) rate. The *IIR* process is converted to a continuous time first order lowpass filter. $u(m)$ is a finite-impulse-response (*FIR*) process that, by further analysis, can be shown to be an anti-aliasing filter for the implicit downsampling from the data sample rate to the frame sample rate, f_s, so may be neglected in an analogue realisation. $t(n)$ is either a squaring or multiplying operation as appropriate. Thus the correlation blocks are realisable in the s-domain as in figure 4, where $\tau = -1/f_s \ln\beta$ seconds.

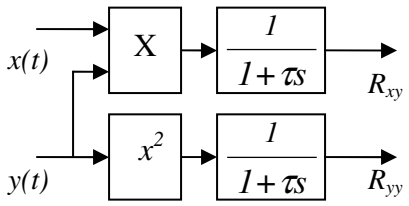

Fig. 4: *The analogue correlation system*

3.3. Simulation results

Figure 5(a) shows simulation results of the analogue implementation and figure 5(b) its digital counterpart. Pulsed white noise is applied to the system in at an angle of *135* degrees and a sine wave at *45* degrees. Both sets of graphs show like waveforms as the two systems adapt to the input in similar ways.

4. CIRCUITS

Circuits are implemented using the continuous time blocks discussed in section 3. All blocks are designed and simulated in the *0.35μm CSD AMS CMOS* process with a power supply of *900 mV* and using *BSIM3v3* models.

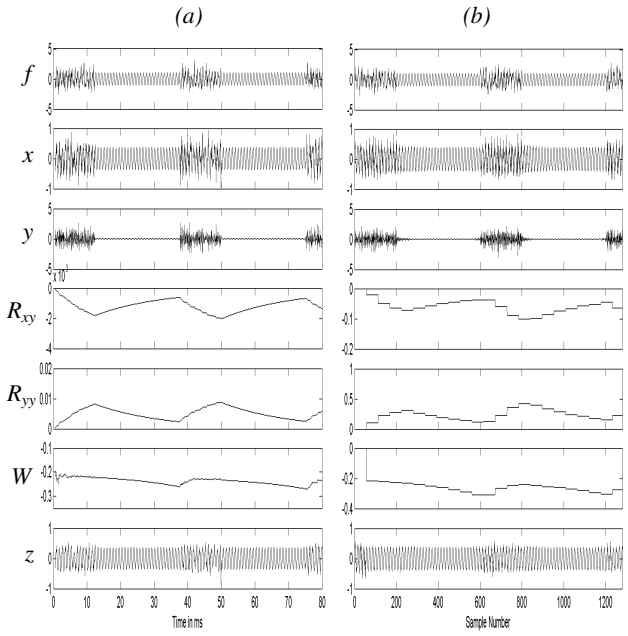

Fig. 5: *Simulations of (a) the analogue system and (b) the digital system*

4.1. Integrator

A log domain *CMOS* integrator is chosen based on a *BiCMOS* implementation [3]. Figure 6 shows one differential half of the proposed circuit. Both i_{in+}, the positive input, and i_{out-} the output from the other differential half are applied to the circuit. Likewise, the output i_{out+} from this circuit is fed into the other half.

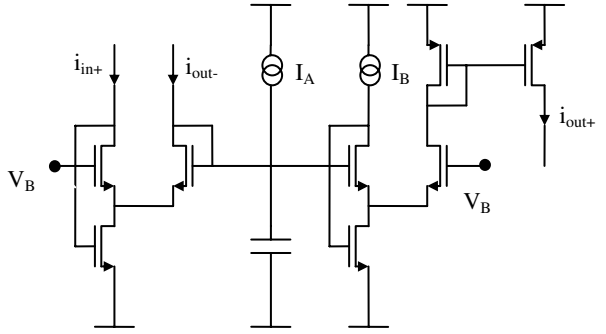

Fig. 6: *A differential half of the integrator*

The drain current, I_D, for an *nMOS* transistor in the weak inversion saturation region is approximately given by

$$I_D = I_S \exp\left(\frac{V_G - nV_S - V_{th}}{nU_T}\right). \qquad (8)$$

Where I_S, V_G, V_S, V_{th}, U_T and n are the specific current, gate voltage, source voltage, threshold voltage, thermal voltage and slope factor, respectively. Using this expression without further approximation, the differential equations for each half of the circuit become

$$\frac{nU_TC}{I_A}\frac{di_{out+}}{dt} + \frac{I_B + i_{out-}}{I_A} i_{out+} = i_{in+} \qquad (9)$$

$$\frac{nU_TC}{I_A}\frac{di_{out-}}{dt} + \frac{I_B + i_{out+}}{I_A} i_{out-} = i_{in-} \qquad (10)$$

When the differential output $i_{out+} - i_{out-}$ is calculated the $i_{out+}\ x\ i_{out-}$ terms cancel providing a linear system with transfer function

$$T(s) = \frac{I_A / nU_TC}{s + I_B / nU_TC}. \qquad (11)$$

4.2. Allpass filter

A block diagram of the allpass filter used may be seen in figure 7 [4]. A fully differential approach is taken using the integrator proposed in section 4.1. Values for the constants are $\tau_1 = 1.4 \times 10^{-5}\ s$ and $\tau_2 = 4.8 \times 10^{-6}\ s$.

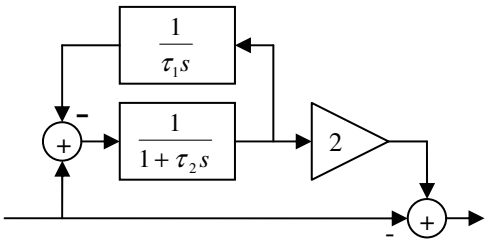

Fig. 7: *The allpass filter block*

Power consumption for the allpass filter is *1.26 μW* with a dynamic range of *44 dB* and a total harmonic distortion of *1.2%*. Group delay over the audio frequency range of *20 Hz* to *20 kHz* is *30.5 ± 0.5 μs*.

4.3. Lowpass filters

The integrator in section 4.1 is used as the first order lowpass filter, implementing equation (11). The cut-off frequency is *9.7 Hz* so the current I_A has to be in the order of tens of picoamps for an integrating capacitance of *20 pF*. Power consumption for the filter is *40 nW* and the dynamic range is *64 dB*.

4.4. Multiplier

This circuit, figure 8, is an adaptation of a Gilbert cell [5] with a proposed input current mirroring scheme applying a form of pre-distortion. Since the input signals are currents, pre-distortion is created by diode connected transistors T1, T4, T7 and T10. Further, using this arrangement three translinear loops are formed T1 - T4, T4 - T6 and T7 - T10. Considering eq.(8) as a model for transistors in weak inversion saturation with no further approximations, i_{out} may be calculated as

$$i_{out} = i_{out+} - i_{out-} = I_0 \frac{(i_{inA+} - i_{inA-})(i_{inB+} - i_{inB-})}{(i_{inA+} + i_{inA-})(i_{inB+} + i_{inB-})}. \qquad (12)$$

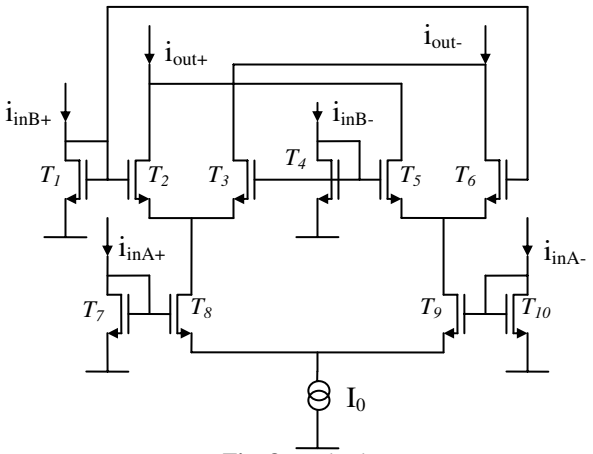

Fig. 8: *Multiplier circuit*

For multiplication to occur only, the input signals must be conditioned suitably such that the denominator terms in eq.(12) ($i_{inA+} + i_{inA-}$) and ($i_{inB+} + i_{inB-}$) are constant. The circuit for providing such conditioning, figure 9, uses current mirrors ($M_1 - M_3$) and current sources to maintain a constant value for the common sum, the dc level of each output being I_2. The arrow on each current mirror ($M_1 - M_3$) indicating the input. Both differential input signals are conditioned in this way.

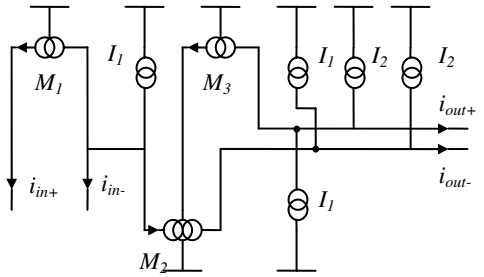

Fig. 9: *Multiplier input conditioning circuit*

Power consumption for the multiplier as a whole is *560 nW* with a dynamic range of *50 dB*.

4.5. Divider

A divider is implemented by considering the multiplier in section 4.4. Should one pair of inputs in eq.(12) be conditioned differently so that the numerator $i_{inA+} - i_{inA-} = I$, a constant, and the denominator $i_{inA+} + i_{inA-} = i_{inA}$ then a two-quadrant divider is realised. Thus the input conditioning circuit for one input must fulfil the transformation

$$i_{inB+} = \frac{i_D - I_0}{2} \qquad (13)$$

$$i_{inB-} = \frac{i_D + I_0}{2} \qquad (14)$$

The circuit to achieve this may be seen in figure 10. Thus, this circuit connects to the inputs i_{inB+} and i_{inB-} of the Gilbert cell and the circuit shown in figure 9 to the other inputs.

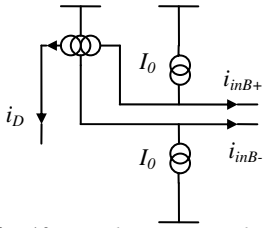

Fig. 10: *Divider input conditioning circuit*

Power consumption for the divider circuit is *560 nW* with a dynamic range of *55 dB*.

4.6. Total power consumption

The circuit blocks are combined to construct the complete analogue system as in figure 3. The power consumption for the whole system is shown in table 2.

Block	Number off	Power Consumption in *nW*
All Pass	2	2520
Low Pass	2	180
Multiplier	3	1680
Divider	1	560
	Grand Total	4940

Tab. 2: *Power consumption summary*

5. CONCLUSION

An algorithm for directionality in hearing aids using analogue techniques is proposed. The discrete digital system is converted to the continuous domain block by block. The reduction in the number of A to D converters together with the blocks designed using *CMOS* technology with transistors operating in the weak inversion region bring with them a very important reduction in terms of power. The complete analogue system operates at *0.9 V* with a power consumption of *5 μW*.

6. REFERENCES

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