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Analogue-to-digital and digital-to-analogue conversion for broadcast quality sound

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SUMMARY

A 13-channel p.c.m. system forms a significant part of the BBC's national radio distribution network, and is used to carry high-quality sound-programme material hundreds of miles with minimal impairment from noise, interference and distortion.

High-quality analogue-to-digital converters (a.d.c.) and digital-to-analogue converters (d.a.c.) are required for use in sound-programme links, and other applications for these converters, such as digital sound studio equipment, can be foreseen, To date, the BBC has used 13-bit a.d.cs and d.a.cs developed within the Corporation. The next generation of digital equipment is likely to require coders and decoders giving 14 bits/sample or even higher resolution.

In this paper, some of the defects which may be encountered with various types of a.d.c. and d.a.c. are discussed, and the merits of different types of converter for high-quality sound are considered.

1 Introduction

The BBC first used pulse code modulation on a regular basis in the broadcasting service from May 1972, when a digital 'sound-in-syncs' system was installed to carry the sound accompaniment to the BBC-1 and BBC-2 television signals over the major part of the television distribution network. This particular p.c.m. sound system uses 10 bits/sample coding with a sampling rate of 31·25 kHz (i.e. twice the television line frequency of 15·625 kHz), and the sound signal is compressed using an analogue compressor prior to coding, with corresponding expansion after decoding.

P.c.m. was also introduced into the sound-programme distribution network in the same year (1972) when a 13-channel multiplex system was installed to carry signals from London (Broadcasting House) to the transmitter at Wrotham in Kent; a monochrome television s.h.f. radio link was used to carry the p.c.m. bit stream. The p.c.m. system has been expanded over the years, and now it extends into Wales, Scotland and Northern Ireland and forms a significant part of the BBC radio distribution network.

Programmes which originate in the regions are sent to London for distribution over this network but analogue contribution circuits carry the programmes into London, at the present time. The use of p.c.m. systems for these circuits would be most desirable, as these programme signals from the regions travel even greater distances than those originating in London.

The 13-channel distribution system employs 13-bit coding and this is the minimum coding resolution which can be accepted. Future developments in p.c.m. systems for use with high-quality sound-programme material are likely to use 14-bit coding. The higher resolution gives lower levels of idle-channel noise which is compatible with the rest of the transmission network and the best domestic receivers. The sampling rate in the current system is 32 kHz and this will be retained in future systems for the distribution of sound programmes.†

There are applications for p.c.m. in the studio as well. Digital recording is an obvious use, and the increased signal-to-noise ratio obtainable by the use of digital techniques in tape-recording equipment would be of considerable benefit. Studio presentation and mixing equipment would benefit from the increased dynamic range of digital systems; it is likely that even higher resolution a.d.cs and d.a.cs could be of value here in order to achieve lower levels of quantizing noise in signals which undergo digital processing. There may also be some advantage in using a higher sampling rate than 32 kHz in studio equipment, but this has yet to be decided.

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† The use of 32 kHz sampling rate for digital links carrying high-quality sound programmes has been agreed within Europe.

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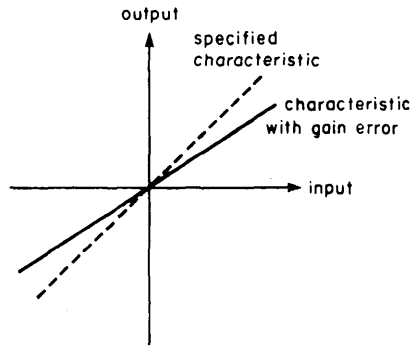
The conversion of the analogue programme signal into digital form and back again is the heart of any p.c.m. system and it is this interface between the analogue and digital forms which creates the most difficulty. Apart from the fundamental distortions which arise out of the quantization process, many converters suffer from instrumental defects which can produce audible impairments.

2 Errors Encountered in Practical Analogue-to-digital and Digital-to-analogue Converters

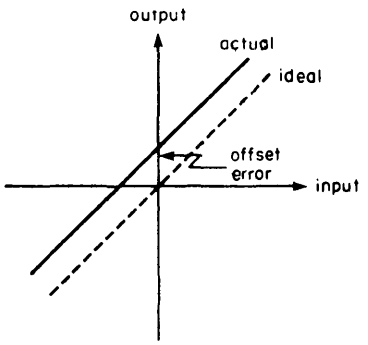
An ideal a.d.c.–d.a.c. combination (codec) would have a linear transfer characteristic, although this linear characteristic would comprise a large number of very small, equal quantizing steps. In a practical codec, the transfer characteristic may differ from that of the ideal codec in a number of ways. The principal differences found are in the slope and linearity of the transfer characteristic and in offset effects caused by d.c. drift.

Figure 1(a) shows the effect of gain error upon the transfer characteristic, which then has a slope differing from the design value. Gain error is unimportant for sound signals, as the analogue circuits in the equipment can be used to compensate for this. The effect of offset error is not too disastrous, either. With offset error (see Fig. 1(b)) the d.c. shift in the transfer characteristic results in asymmetry of the overload characteristic, and may restrict dynamic range somewhat. It can be more serious if a codec with offset error is used in a digitally companded† system;[1] low-level signals may suffer an increased quantizing distortion and programme-modulated noise may be enhanced.

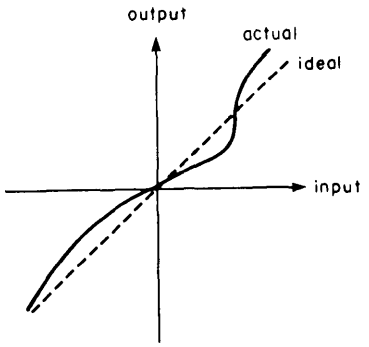
Non-linearity of the transfer characteristic (Fig. 1(c)) is very important, and the degree of non-linearity which can be tolerated is the same as for analogue sound equipment. In fact, when non-linearity occurs it normally does so in the associated analogue circuits. But the non-linear distortion can occur in the digital circuits, if the quantum steps which make up the transfer characteristics are not of uniform size. This type of distortion, known as differential linearity error, is illustrated in Fig. 1(d). If the differential linearity error exceeds the magnitude of one least significant bit, this can cause the slope of the transfer characteristic to reverse over part of the coding range; this non-monotonicity would have serious consequences in digital audio equipment. An example of a non-monotonic d.a.c. transfer characteristic is shown in Fig. 2. Under some circumstances, severe differential linearity error causes a convertor to omit codes (one such situation would be if a non-monotonic d.a.c. were to form part of a successive-approximation a.d.c.). Figure 3 shows an a.d.c. transfer characteristic which exhibits missed codes.



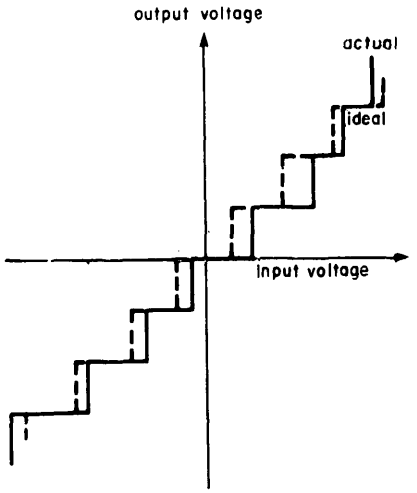
(a) Gain error



(b) Offset error.



(c) Linearity error.



(d) Differential linearity error.

Fig. 1. Errors in a.d.c.-d.a.c. combinations. (a) Gain error.

† Digital companding (compressing and expanding) techniques can be used to reduce the bit-rate requirements for the transmission of digital sound signals.

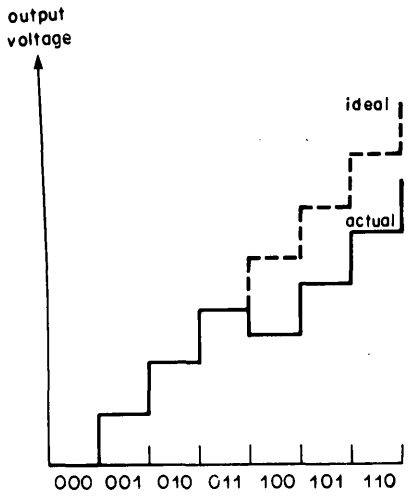


Fig. 2. Non-monotonicity in a d.a.c.

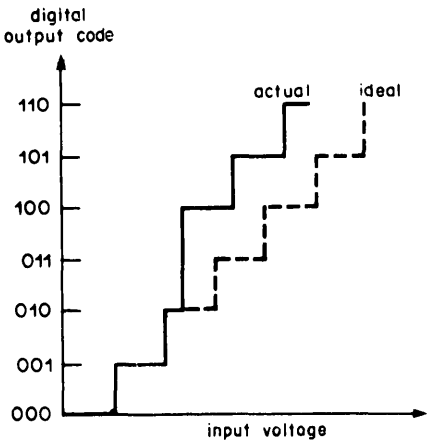


Fig. 3. Missing code in an a.d.c.

If the signal at the input to the a.d.c. changes during the conversion process, this can sometimes introduce errors in coding. Sample-and-hold circuits are therefore often used at the inputs of a.d.cs so that the signal is held constant during conversion. They can also be used after d.a.cs to remove spurious transients (sometimes known as 'glitches') from the signal, and thereby ease the task of low-pass filtering the decoded analogue signal. This is illustrated in Fig. 4. As a result of non-linearity in the sample-and-hold circuits, audible intermodulation products can be formed by signal components beating with the sampling frequency. It is therefore necessary to ensure that sample-and-hold circuits for use with a.d.cs and d.a.cs do not introduce any significant amount of non-linear distortion.

3 Types of A.D.C. and D.A.C.

As stated in the Introduction a relatively large number of bits (at least 13) is needed in order to code a sound signal sufficiently accurately for sound-programme purposes,[2] and the available conversion time is about 30 μs for a 32 kHz sampling rate. In contrast, for coding broadcast quality video signals 8-bit resolution is normally considered to be sufficient but the conversion time is very much shorter (100 ns or less).

In the following descriptions of conversion techniques digital-to-analogue converters are considered first, as some types of audio analogue-to-digital converters employ a d.a.c. within a feedback loop.

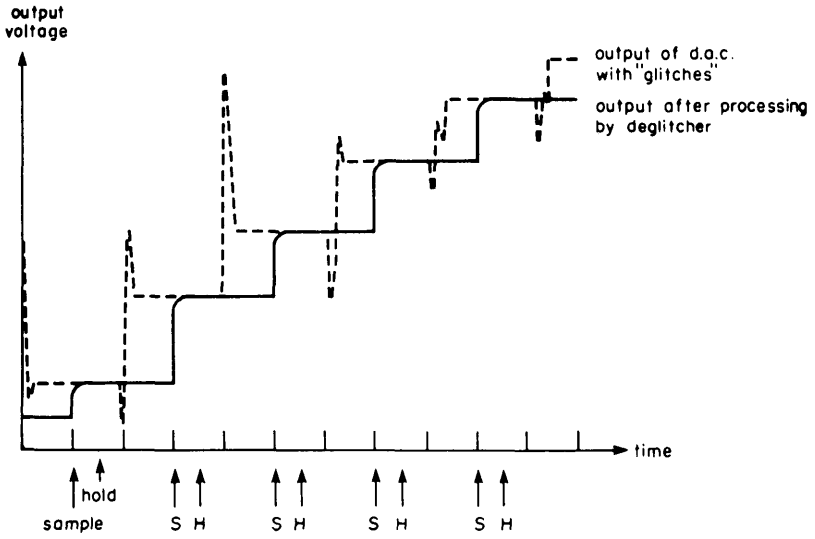


Fig. 4. Operation of a deglitcher.

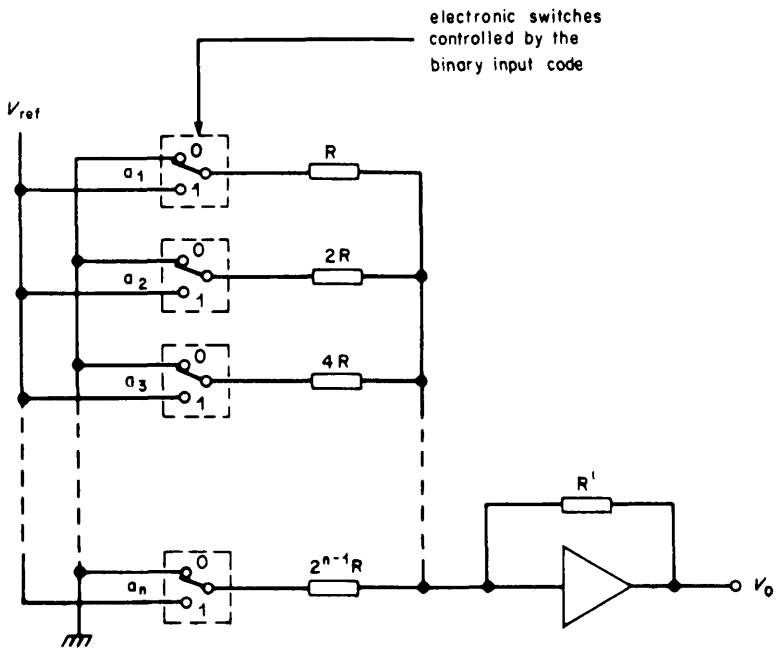


Fig. 5. Weighted current d.a.c.

3.1 Techniques for Digital-to-analogue Conversion

Figure 5 shows a weighted current d.a.c. in which a number of precision resistors produce binary-related currents from a reference voltage source. The binary input code (in parallel form) controls the switches which turn the currents on and off. The currents are added in the summing amplifier. The main problem with this type of d.a.c. is the extensive range of precision resistor values which is needed. An n-bit d.a.c. requires n precision resistors over a range of $1 : 2^{n-1}$ in value, and the ratios must remain constant over the operational temperature range and life of the decoder. An error of 0·012% in the resistor supplying the current controlled by the most significant bit of a 14-bit decoder will cause it to become non-monotonic. Another problem with this circuit is that resistance in the switches will affect accuracy, and, if the switches do not operate simultaneously, 'glitches' will be induced in the output as illustrated in Fig. 4.

Some of the problems can be overcome by using a resistive ladder network of the form shown in Fig. 6. Only two resistor values are involved in the ladder network type of d.a.c. and these are in the ratio 1 : 2. This network has the characteristic that the resistances of the three branches associated with any node are equal ($2R$) so that a current fed into a node from one branch splits equally between the other two branches. One could, therefore, make a parallel d.a.c. using the simple arrangement in Fig. 7(a). As before, the switches are operated by the input code.

It is, in fact, better to adopt the arrangement shown in Fig. 7(b) and drive the network from one end with the reference voltage whilst currents from the shunt arms are switched into a summing amplifier. This arrangement does not depend upon network time-constants, as the currents are constant (the switches operate between earth and 'virtual earth' points). Consequently, resistor values may be made higher to reduce the significance of switch resistance.

This type of modified ladder-network converter is quite popular in the commercial field where 13-bit or greater resolution is required. An error of 0·012% in the value of the resistors determining the most significant bit (m.s.b.) current in a 14-bit d.a.c. can make it non-monotonic at its mid-range point, and an error of 0·024% in the resistors determining the current for the next m.s.b. causes discontinuities at the $\frac{1}{4}$ and $\frac{3}{4}$ range points as well. Discontinuities can be introduced at other points on the transfer characteristic by correspondingly larger errors in the other resistors of the ladder network. Most ladder-network converters use thin-film resistor networks in order to obtain resistances of the required accuracy. Thin-film resistor networks can be made with sufficient accuracy and stability for use in 13-bit resolution converters;[3] however it may not be possible to obtain sufficient accuracy and stability using this technique for converters with 14-bit or greater resolution without providing for adjustment of the m.s.b. resistors.

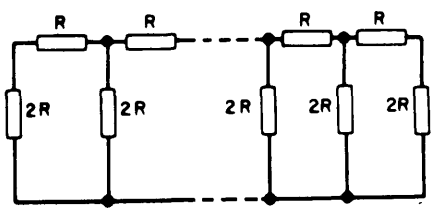
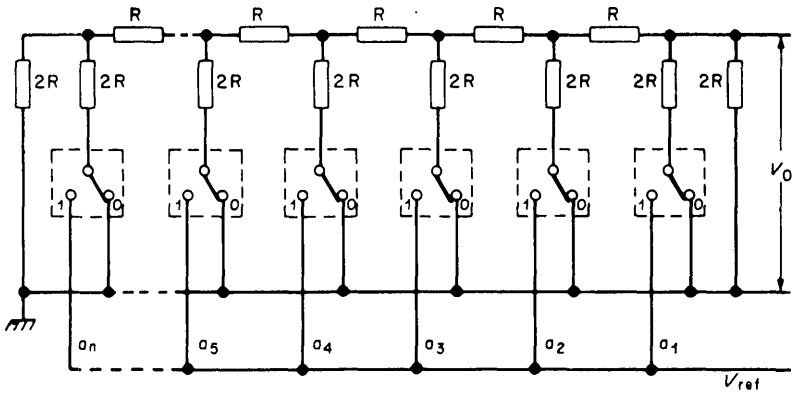
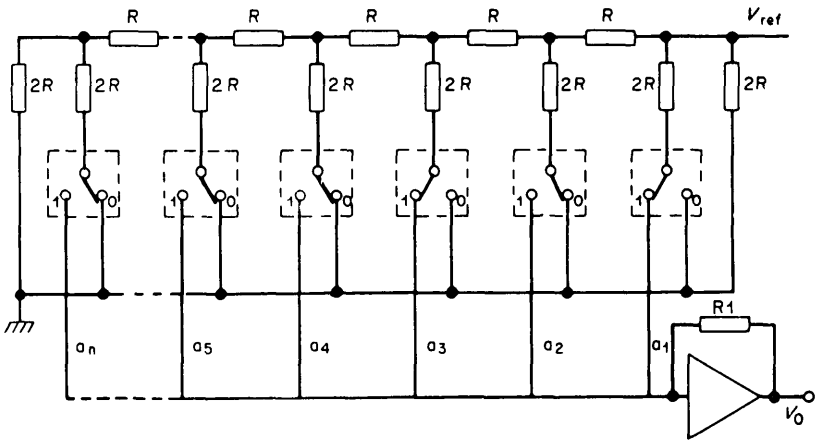


Fig. 6. $R : 2R$ ladder network.



(a) Using voltage switching.



(b) Using current routing switches.

Fig. 7. Ladder network d.a.cs.

3.2 Techniques for Analogue-to-digital Conversion

Probably the most popular type of commercial analogue-to-digital converter is the successive approximation a.d.c. shown in Fig. 8. This converter uses a parallel d.a.c. (see the previous Section) fed from logic circuits which adjust the d.a.c. input code until its output is as close as possible to the analogue input voltage. Each bit of the d.a.c. input code is set to '1' in turn, starting with the most significant. If the d.a.c. output is then less than the analogue signal to be coded, the bit remains set to '1'; if it is greater the bit is reset to '0', and so on. When the process is complete, the d.a.c input code is taken as the a.d.c. output.

The accuracy of the successive approximation a.d.c. depends upon that of the associated d.a.c. This type of a.d.c. gives missed codes if the d.a.c. becomes non-monotonic. During conversion, the input signal to the successive approximation a.d.c. must be kept constant, so a sample-and-hold circuit is essential at the input.

Another technique for analogue-to-digital conversion which has been studied uses a delta-modulator[4] with subsequent conversion to p.c.m. A basic delta modulator

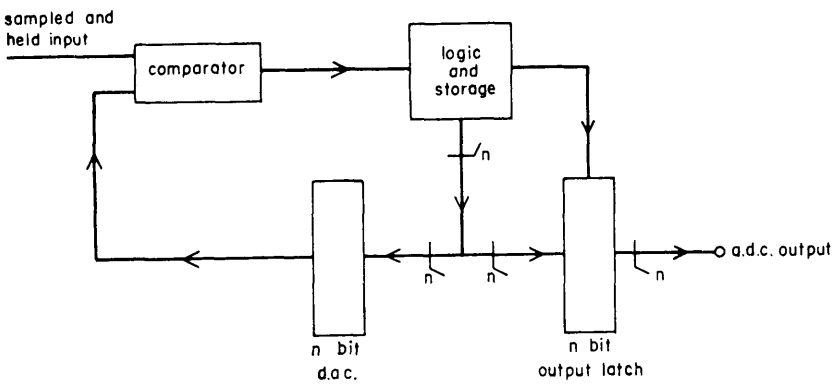


Fig. 8. Successive approximation a.d.c.

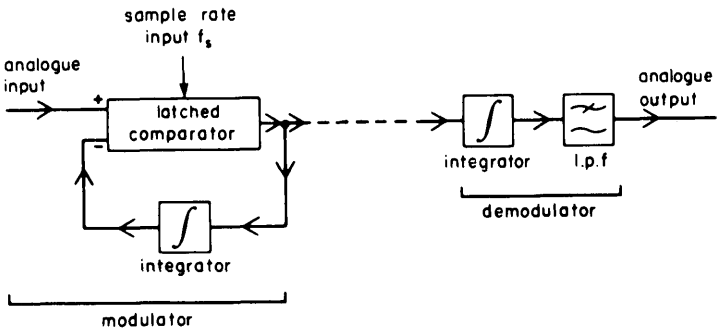


Fig. 9. Block diagram of delta modulator and demodulator.

with demodulator is shown in Fig. 9, and operation is as follows. The comparator compares the analogue input signal with the output of the integrator in the feedback path. If the analogue input level is greater than the integrator output, the comparator gives a logical '1' at its output which causes the integrator output level to increase by a defined amount. If the analogue input level is less than the integrator output, the comparator output is logical '0' causing the integrator output to decrease (by the same defined amount). Thus the feedback system in the modulator causes the integrator output to follow the analogue input signal in steps, and the output of the modulator is a one-bit p.c.m. signal.

The delta demodulator is simply an integrator which is identical with the integrator in the feedback path of the modulator. A low-pass filter after the integrator removes the residual components at $f_s/2$ and harmonics.

A delta modulator may be used to convert analogue signals to p.c.m. using the arrangement shown in Fig. 10. The comparator, up-down counter and 9-bit d.a.c. form a digital delta modulator, with the up-down counter and d.a.c. fulfilling the same function as the integrator in the feedback path of the delta modulator shown in Fig. 9. The up-down counter effectively converts the one-bit p.c.m. signal into a 9-bit p.c.m. signal at the same sampling rate (20 MHz). This p.c.m. signal is then passed through a digital low-pass filter and re-sampled at 32 kHz. It was hoped, when investigations into this technique began, that it would be possible to construct an a.d.c. having at least 14-bit resolution. However, instrumental problems restricted resolution to little better than 13-bit,[5] and the delta modulation-to-p.c.m. technique has so far proved to be more complicated to implement than the dual-slope ramp counter converter (see next Section).

3.3 The Ramp Counter Converter: a Technique applicable to A.D.Cs and D.A.Cs

The ramp counter converter[6] is a technique which can be used both for analogue-to-digital conversion and for digital-to-analogue conversion.

A block diagram of a ramp counter a.d.c. is shown in Fig. 11. In this type of a.d.c., the input voltage

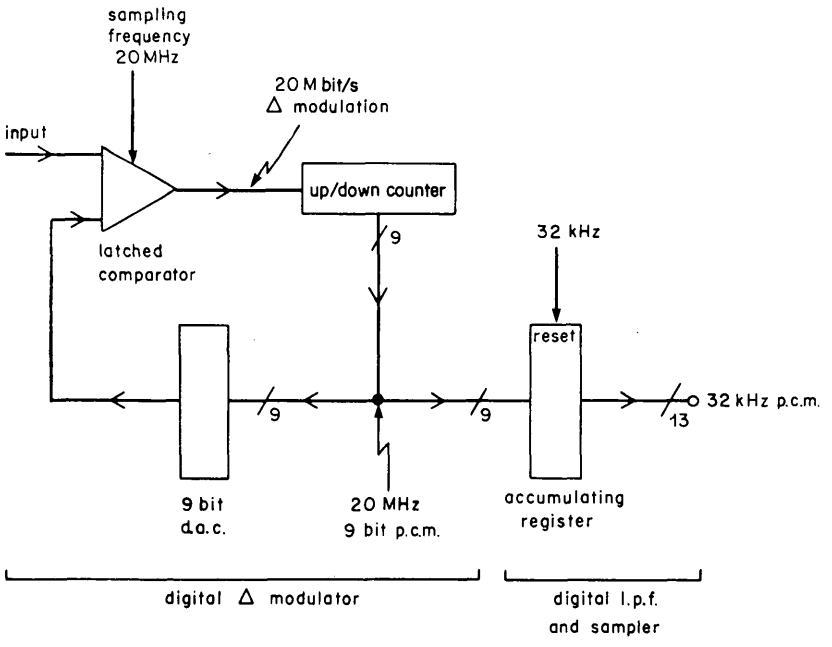


Fig. 10. Digital delta-modulator with low-pass filter and resampler.

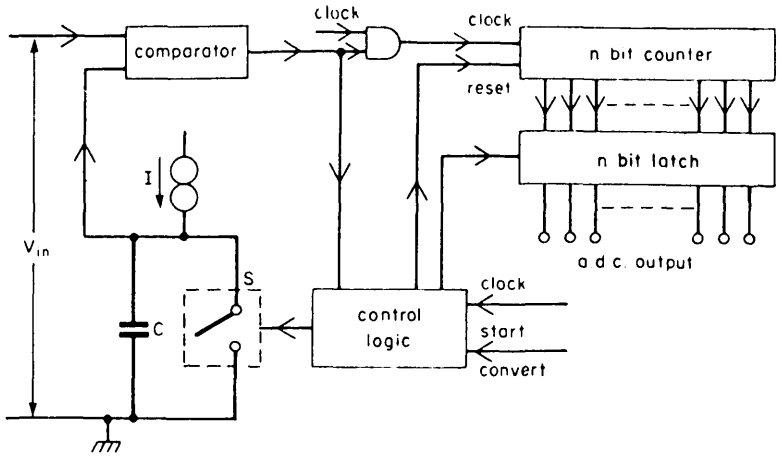


Fig. 11. Ramp counter a.d.c.

is converted to a time interval which is then measured to give a digital output, using the following sequence of operations. Initially, the counter is set to zero and the switch S is closed. Conversion starts when switch S is opened and the counter is enabled. The counter counts clock pulses as the capacitor charges linearly, from the constant current source, until the potential difference across the capacitor reaches the input voltage; the comparator then changes state and halts the counter. The control logic then instructs the output latch to accept the number held in the counter, switch S is closed to discharge the capacitor and the counter is reset to zero ready for the next conversion. It is clear that the time taken for the capacitor to charge to the level of the input signal voltage (V_{in}) is directly proportional to V_{in}, and in turn the final output of the counter is proportional to the time interval, and hence to V_{in}.

This type of convertor must be preceded by a sample-and-hold circuit. Without a sample-and-hold circuit, sampling would occur at irregular intervals, even if conversion were started regularly, and the noise performance of the convertor would suffer.

The ramp counter d.a.c. operates in the reverse manner to the a.d.c. and uses very similar circuitry. The input digital code is loaded into a down counter, and upon receiving the start conversion command the counter commences counting towards zero. At the same time, a constant-current source is connected to the ramp capacitor. When the counter reaches zero, the constant-current source is switched off, and the voltage across the ramp capacitor is transferred to a sample-and-hold circuit at the output of the d.a.c. After discharging the capacitor, the d.a.c. is ready for the next conversion.

Although the ramp counter converter offers very low differential non-linearity, the need for very high counting speeds presents problems. A 13-bit sound codec operating at a sampling rate of 32 kHz would require a counter clock at a minimum rate of 270 MHz. The comparator also presents problems, as it must have a high gain to give the necessary resolution and must be able to halt the counter within a time period which does not vary by more than a fraction of one clock pulse, if a good noise performance is to be obtained.

A variant of the ramp counter converter has been developed within the BBC for 13-bit sound coding and decoding and is in use with the 13-channel p.c.m. distribution system. This converter is the dual-slope ramp type (sometimes referred to as the 'change-gear' converter).† In the BBC's dual-slope ramp a.d.c., a fast-rising ramp voltage is compared with the input signal, and the time taken for it to overtake the input voltage (V_{in}) is taken as an approximate measure of V_{in}. This value is used to set the most significant bits. The ramp voltage then drops a small fixed amount before rising more slowly to determine V_{in} more accurately and set the least significant bits. The sequence of operations is illustrated in Fig. 12.

Generation of the dual-slope ramp voltage for an a.d.c is a relatively straightforward matter, using the arrangement shown in the simplified schematic diagram of Fig. 13. Before conversion, S1 is closed and so the capacitor C is charged to $-V$ (which corresponds to the negative limit of the coding range). At the start of conversion, S1 is opened and S2 closed. Initially the voltage across the capacitor rises linearly with time at a rate given by $dV/dt = 64I/C$. The time taken for the voltage across the capacitor plus the voltage across R to reach the sampled-and-held audio input voltage is recorded by a 7-stage counter. The 7-bit number obtained from this counter represents the 7 most significant bits of the conversion. At this point the comparator changes state, switch S2 is opened and the capacitor charging current reduces by a factor 64 : 1. The voltage across R drops so that the comparator changes back to the initial state, and the voltage across the capacitor rises at a slower rate given by $dV/dt = I/C$. When the voltage applied to the comparator by the ramp circuit reaches the sampled-and-held input voltage, the comparator changes state once again.

† The terms 'dual ramp' and 'dual-slope ramp' have been used to describe a number of conversion techniques developed from the basic ramp counter converter, and some confusion can arise between the different types as a result. The alternative name 'change-gear' is therefore often used to describe the BBC's dual-slope ramp converters, although this does not describe the operation of the converter as satisfactorily as 'dual-slope ramp'.

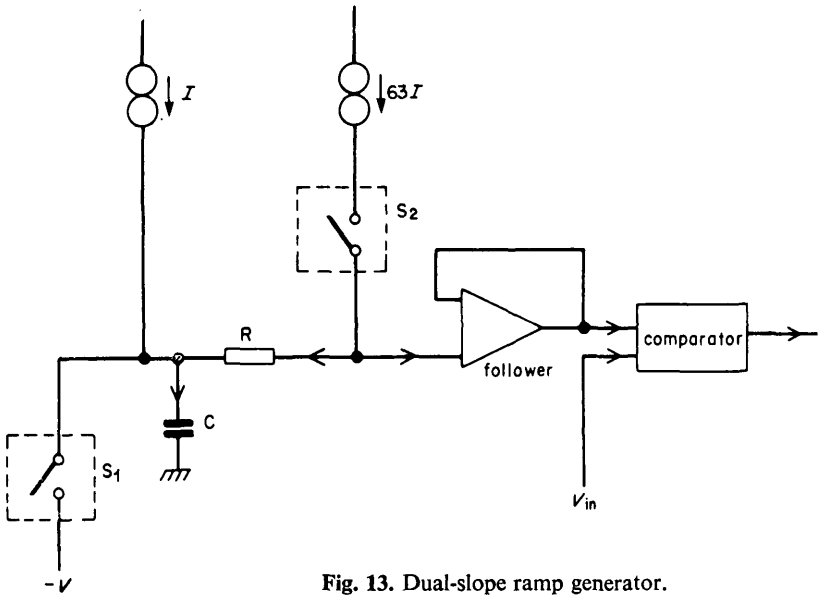


Fig. 13. Dual-slope ramp generator.

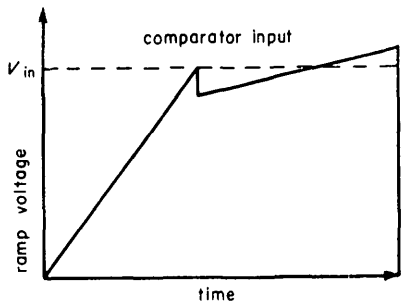


Fig. 12. Operation of dual-slope ramp a.d.c.

The duration of the slow ramp is measured by a 6-stage binary counter to give the least significant bits of the conversion.

The dual-slope ramp d.a.c. operates in exactly the reverse manner. The 7 most significant bits determine the period for which a capacitor is charged by a current of magnitude $64I$, and the 6 least significant bits determine the period of charging by a current of magnitude I.

The great advantage of the dual-slope ramp converter is that counting speeds are reduced significantly. For the 13-bit converters, the counters can use a clock frequency in the region of 12 MHz instead of 270 MHz, giving reduced cost and heat dissipation in the counting logic and easing the problems of keeping high-speed digital waveforms out of the analogue circuits. The principal disadvantage with this type of converter is the difficulty of ensuring that the capacitor charging currents remain in the ratio 64 : 1. For a 13-bit counter, an error of 1·56% in the ratio results in a discontinuity equivalent to one least significant bit.

4 Future Developments in A.D.Cs and D.A.Cs for Sound-programme Use

As explained in the introduction to this paper, the BBC's future requirements will be for a.d.cs and d.a.cs with at least 14-bit resolution. Any developments in the field of a.d.cs and d.a.cs undertaken by the BBC are likely to involve the already well-tried dual-slope ramp converter technique. A successful 14-bit codec has been made using this principle, but further development would be necessary before the production of significant quantities of these could be undertaken. One or two commercial codecs using ladder-network d.a.c. and successive-approximation a.d.c. techniques may be suitable for sound-programme coding and decoding applications, and might be able to offer resolutions of up to 16 bits/sample for this purpose. Some examples of these tested by the BBC have given encouraging results, but most commercial equipment is either too slow or suffers from errors such as those described in Section 2. The equipment which has proved satisfactory has required extensive modification for use in BBC applications.

For the present, therefore, p.c.m. sound equipment under development within the BBC will use the existing 13-bit dual-slope ramp type of a.d.c. and d.a.c., even though the use of higher resolution codecs is envisaged with the new generation of NICAM (near instantaneous companding audio multiplex) equipment. Provision will be made for the new equipment to accept 14-bit a.d.cs and d.a.cs, which will be designed as 'plug-in' replacements for the 13-bit units, when they become available.

5 Acknowledgment

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