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Reconfigurable Sound Wave Filter bank with Low Power 16-channel bank core with Adaptive Band for Hearing Aids

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Abstract— **Hearing impaired people have their own hearing losscharacteristics and listening preferences. Therefore hearing aid system should become more natural, humanized and personalized, which requires the filter bank in hearing aids provides flexible sound wave so that patients are likely to use the most suitable scheme for their own hearing compensation strategy. In this paper, a reconfigurable sound wave filter bank is proposed. We describe a 16-channel critical-like spaced, highstop band attenuation ($\geqslant_{60}$ dB, 109th $\times$ 16-order), micro power (247.5 μW@1.1 V, 0.96 MHz), small integrated circuit (IC) area (1.62 mm$_2$@0.35-μm CMOS) finite impulse response filter bank core for power-critical hearing aids. We achieve the low-power and small IC area attributes by our proposed common pre-Computational unit to generate a set of pre-calculated intermediate values that is shared by all 16 channels. We also take advantage of the consecutive zeros in the coefficients of the filter channels, allowing the multiplexers there in to be simplified**

Keywords— **Filter bank, finite-impulse response (FIR) digitalfilters, hearing aids, low power, nonuniform bandwidth.**

I.   Introduction

HEARING aids (hearing instruments) are well accepted in the medical community as high-efficacy assistiveportable biomedical devices to improve the speech intelligibility of hearing impaired users. The primary challenges of these devices include noise reduction (higher signal-to-noise ratio signals in noisy environments) [1], higher acoustical gain before the onset of acoustic feedback [2], low-distortion high-efficiency output amplifiers (Class-D) [3], small integrated circuit (IC) area, and low-power dissipation [4]. In the case of the latter two,for aesthetic and portability reasons, these hearing aids are powered remotely from a low-energy capacity ($\sim$100mA h) low voltage (1.1–1.4 V) miniature-size battery. Consequently, much of these challenges pertain to the Development of more intelligent algorithms and to the degree of sophistication of these algorithms that can be realized without excessive power dissipation and IC area overhead. Two of the major issues in digital hearing aid design are high flexibility and low power consumption. High flexibility accounts for a more accurate fitting that results in increased hearing clarity for the wearer. Lower power consumption prolongs battery lifetime. There have been active researches to achieve both high flexibility and low power consumption at once. A more elaborate approach is to divide the frequency spectrum into many bands [5] [6]. So, we have used up to 16 bands. While these implementations do allow for a fine-grained fitting, for a future advanced hearing aid, we specify the need for a linear phase (constant group delay) filter bank as opposed to the prevalent nonlinear phase infinite-impulse response (IIR) filter bank in current-art hearing aids. We deem the linear phase response necessary for an improved acoustic

noise cancellation algorithm and for the potential of better preserving the phase cues for binaural (as opposed to bilateral) hearing when a pair of hearing aids are simultaneously worn. The major drawback in a linear phase realization is the need for the order of the filter bank to be higher (hence increased overheads) over a filter bank without a linear phase for the same magnitude response. A further attribute that we impose is higher stop band attenuation ($\geqslant 60$ dB) for the filter channels than current-art hearing aids (typically 50 dB). A higher stop band has potential for increased gain before the onset of acoustic feedback and greater magnitude response programmability.

To reduce the power dissipation of the filter bank for hearing aids, low computational complexity interpolated finite-impulse response (IFIR) filter banks [7], [9] have been proposed. However, the bandwidths of these filter banks are usually fixed (spaced uniformly), hence limiting the magnitude response programmability for hearing aids and poor frequency selectivity, particularly at low frequencies. Another approach to reduce the power is to reduce the power due to multiplications as multiplications are the main arithmetic operations in the filter bank. This reported approach includes multipliers with reduced spurious switching [8], multiplier-less and/or reduced hardware complexity techniques including canonical-signed-digit [9], powers-of-two [10], [11], common sub-expression elimination [12], etc. Although the latter techniques [9]–[12] are appeared.

The main purpose for accurate fitting of hearing aids is to enhance the patients' ability to comprehend spoken language. Most other sounds such as environmental noise can be perceived with a far less accurate compensation. This presents an opportunity to decrease power consumption by reducing the complexity of the DSP when the patient is not listening to speech. By using a voice activity detection circuit with low computational complexity in conjunction with clock gating techniques, the number of active filter elements can be reduced further to just one when no speech is detected in the incoming sound stream.
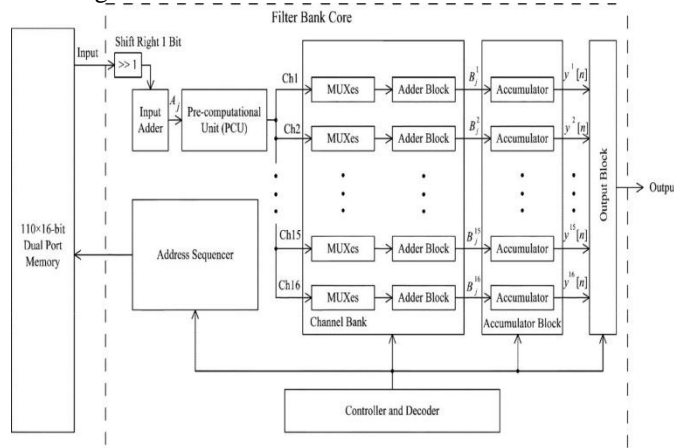

Fig. 1. Block diagram of the proposed 16-channel filter bank.

In this brief, we propose a critical-like spaced 16-channel linear-phase FIR filter bank core that features micro power [247.5

μW (excluding the memory)@1.1 V, 0.96 MHz using a 0.35-μm CMOS process] operation, high stop band attenuation ($\geqslant 60$dB per channel), and small IC area (1.62 mm$_2$). We achieve the low-power attributes by the design of a proposed simple pre-computational unit [(PCU), see Fig. 3, shown later] that can be shared by all channels and output of the PCU is multiplexed and added in a predetermined sequence to obtain the multiplication outputs. The multiplication operations are hence not realized by the usual dedicated power-hungry multi-pliers, and hence power reduction. In addition to the proposed architecture, we further reduce the power dissipation of the filter bank by adopting the technique of reducing the effective word length of the coefficients of the filter channels (where there are consecutive zeros) without compromising performance. We show that our design is very competitive against reported designs, yet obtaining the added desirable linear phase and high stop band attributes not featured in current-art devices. When compared to a conventional filter bank core (16 separate FIR filters with usual array multipliers [11]) of the same filter order, our filter bank is estimated to dissipate 47% lower power dissipation and to feature 37% smaller IC area. With the common pre-computational unit, a set of intermediate values could be shared by all the channels to achieve low power and small area. In [11], the FIR-based design of the 1/3 octave filter bank was proposed. The multi-rate architecture saved both the power and chip size of hearing aids.

I. 10-ms 18-band Quasi-ANSI S1.11 1/3 octave filter bank was proposed in [11]. The inter-band interference was reduced by a prescription-fitting algorithm.

Filter banks mentioned above only provides one kind of sound decomposition scheme. However, the features of hearing loss denoted by audiograms are different from person to person. It is meaningful to provide various sound decompositions to meet the demands of different patients, which implies that the filter bank needs to be reconfigurable. Here "reconfigurable" means that different sub bands distributions could be obtained according to the control parameters without changing the filter-bank's structure.

II. FUNDAMENTALS OF THE IDEA

Before the structure of the proposed filter bank is presented, the design of cosine modulated filter bank and the nonlinear transformation will be described.

A. Cosine-Modulated Uniform Filter bank

A cosine modulated filter bank is defined as modulated filter bank is defined as, where is a low pass FIR prototype filter with length of the modulation factor and a magnitude control factor of the index of the sub band.

The Transform transfer

$$h^{(i)}(n) = c_i \cdot h_L(n) \cdot \cos\left(\frac{\cdot \pi}{M} n\right) \qquad (1)$$

$$H^{(i)}(z) = \sum h^{(i)}(n) z^{-n}$$

$$= \sum c_i \cdot h_L(n) \cdot \cos \frac{\pi}{M} n \cdot z^{-n} \qquad (2)$$
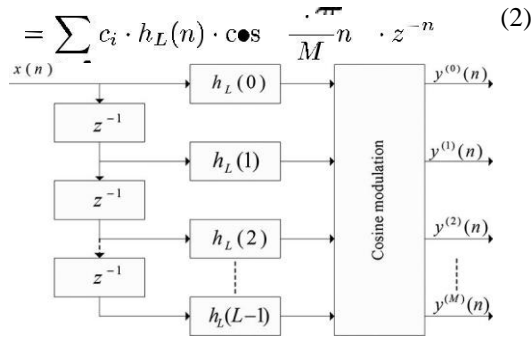

Fig. 2.The structure of the cosine-modulated filter bank.

The magnitude response of the cosine-modulated filter bank is shown in Fig. 1, where ω and ω_s are the pass band edge and stop band edge of the low-pass prototype filter, respectively. It is suggested in the figure that to make the sum of the magnitude responses of all the sub bands equal to unity, (3) should be satisfied. The structure of the cosine-modulated filter bank expressed as

$$\omega_p + \omega_s = \frac{\pi}{M} \qquad (3)$$

B.   The Nonlinear Transformation

In order to transform the uniform filter bank to a non-uniform Filter bank, the original coordinate axis is mapped to a new Co-ordinate axis by a nonlinear transformation (4).

$$z^{-1} = G(Z^{-1}) = \frac{Z^{-1} - \alpha}{1 - \alpha^* \cdot Z^{-1}} \cdot \frac{Z^{-1} - \alpha^*}{1 - \alpha \cdot Z^{-1}}$$

$$= \frac{z^{-2} + d_1 \cdot z^{-1} + d_2}{d_2 \cdot Z^{-2} + d_1 \cdot Z^{-1} + 1} \qquad (4)$$

where z and Z are the z-transform symbols in the original space and the transformed space, respectively. $G(Z_{-1})$ is the cascade of two all-pass filters. Assuming that θ is the frequency point in the original space and ω is the mapped frequency point of θ.

III. Fɪʀ Fɪʟᴛᴇʀ Bᴀɴᴋ Sᴘᴇᴄɪꜰɪᴄᴀᴛɪᴏɴꜱ ᴀɴᴅ Dᴇꜱɪɢɴ

Fig. 3 depicts the magnitude response of 16 channels of the filter bank; each channel is a 109th-order (110 taps) FIR filter sampled at 16 kHz. We adopt the linear-phase-structured FIR (LPFIR) filter and use its symmetrical property to reduce the number of multiplications by half (replaced by simple additions) compared to usual structures such as the transposed or transversal direct form structures. The expression for 109th-order LPFIR filter is

$$y^i[n] = \sum_{j=0}^{54} h^i[j] \cdot \{x[n-j] + x[n-109+j]\} \qquad (1)$$

Where h_i is the coefficient for $j = 0$ to 54 in channel

$,y^i[n]$ is the output of channel i at time n, and $x[n\_j]$ is the input at time n-j.

From (1), we observe that the inputs and their sequence to all channels ($i = 1$ to 16) are identical (before performing the respective multiplications). We exploit this observation by proposing to pre-calculate a set of intermediate signals by means of a PCU, and thereafter reuse these intermediate signals for all channels to generate the multiplication outputs (see Fig. 1). It is interesting to note that a recent reported computation sharing programmable FIR filter [12]also employed a somewhat similar PCU. However, this reported approach is for a high speed transposed direct form FIR filter with a low filter order and is hardware inefficient for realizing filters with high stop band attenuation—its hardware (shift units and adders) increases proportionally with the order of the filter. Furthermore, the reported PCU was also not designed to be shared by the different channels of a filter bank. Our proposed design, on the other hand, does not suffer from these drawbacks—our design easily accommodates high-order filters and the PCU is shared by all channels and is independent of the order of the filters. These desirable attributes ultimately lead to a low-power dissipation and small IC area design.

Fig. 2 depicts the architecture of our proposed filter bank. The filter bank consists of a 110×16-bit dual port RAM and the filter bank core comprising an input adder, a PCU, an address sequencer, a controller and decoder, a channel bank, an accumulator block, and an output block. The PCU effectively provides scaled values (by means of hardwire shifts and adders/ subtractors) of intermediate nodes, $A j$, shown at output of the input adder in Fig. 1. The outputs of the PCU are multiplexed, shifted, and added (by means of multiplexers, hardwire shifts, and adders) in the channel bank and finally accumulated to obtain the outputs of the filter bank. In this proposed architecture, multiplication operations by the usual power-hungry multipliers are completely avoided to reduce power dissipation.

Prior to delineating the filter bank depicted in Fig. 1, we will first describe the PCU and subsequently the operation Of Channel $i = 1$.we depict the proposed PCU that generates the eight possible multiplication products of
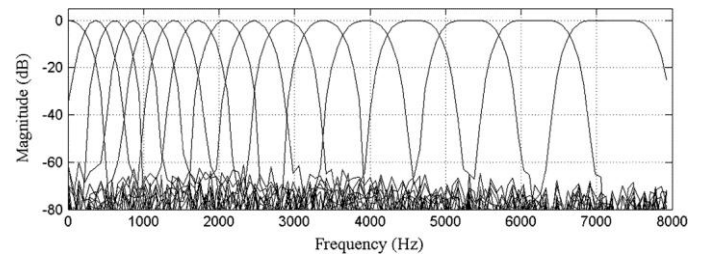

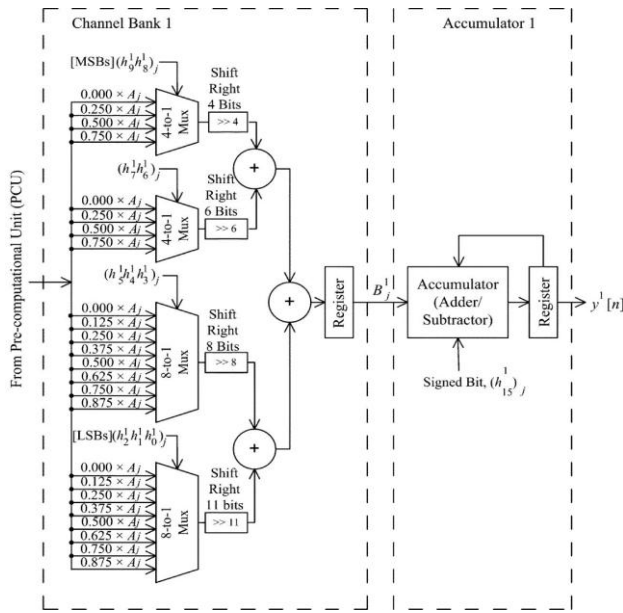Fig. 3.Magnitude response of the 16-channel filter bank.

Fig. 4. Channel bank and accumulator for channel 1.

The computation for the remaining channels, Channel 2 to Channel 16, is similar to that described for Channel 1 except for the effective word length of the coefficients and the value of the coefficients therein. We note that the input adder to obtain A_j and the PCU (refer Fig.1) are identical for all channels. We share these functional blocks between all channels, thereby substantially reducing the hardware complexity of the filter bank. We will quantify the advantages of this proposed approach in Section IV later.

The filter bank requires 60 clock cycles to compute each input sample: 55 clock cycles are used for processing 55 pairs of input data (110 taps) and the remaining 5 clock cycles are used to initialize and reset the filter bank. For 16-kHz sampling frequency, the system clock of our filter bank is low (0.96 MHz, this low clock rate is slightly lower than most current-art hearing aids).

In our filter bank, we take advantage where there are consecutive zeros in the 16-bit coefficients of a particular channel. For example, consider the magnitude bits of the coefficients of Channel 1, $000\text{-}00xx\text{-}xxxx\text{-}xxxx_2$, where x is either 1 or 0. The first five MSBs are removed because the resultant product from a multiplication with consecutive zeros is always 0.

TABLE I
EFFECTIVE WORDLENGTH (EXCLUDING THE SIGNED BIT)
OF COEFFICIENTS FOR DIFFERENT CHANNELS

Table I tabulates the effective word length (excluding the signed bit) of the coefficients of the different channels in our filter bank. Arising from this simple technique, the average word length of the coefficients in the filter bank is reduced by ~ 4 bits, that are the average effective word length is ~ 11 bits.

In hardware terms, this translates to $\sim 20\%$ fewer multiplexers and $\sim 25\%$ fewer adders in the channel bank.
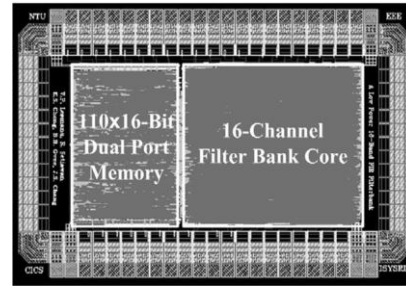
IV. DESIGN PROCESS

Fig. 5 Layout of the 16-channel filter bank

We depict the layout of our filter bank in Fig. 5 and our simulations are based on the extracted parameters

TABLE II
BREAKDOWN OF NUMBER OF TRANSISTORS, IC
AREA, AND POWER DISSIPATION OF THE
DIFFERENT BLOCKS @ 1.1 V, 0.96 MHZ

Sub-Modules	Transistors	Area (mm²)	Power (μW)
Channel Bank	58528	1.008	87.3
Accumulator Block	33692	0.389	70.7
PCU	4220	0.048	66.9
Controller & Decoder	10636	0.110	14.5
Address Sequencer	2244	0.028	2.1
Other	2516	0.037	6.0
Total	111836	1.620	247.5

From this layout. The design is based a commercial 0.35-μm-dual-poly-four-metal CMOS process and standard digital library cells were employed.

We tabulate in Table II the breakdown of the number of transistors, area, and power dissipation of the various blocks of the filter bank core. As expected, the blocks that do most of the computations, namely the channel bank, accumulator block, and PCU, dissipate most of the power and occupy the largest IC area. Of specific interest, the single PCU that is shared by all

16 channels dissipates $\sim 27\%$ of the total power but occupies only $\sim 3\%$ of the total area (or $\sim 4\%$ of the total number of transistors). We attribute its relatively large power dissipation to the large capacitive load due to the large fan-out.

To appreciate the significance of sharing the PCU, we design the same filter bank core without sharing the PCU. Should

16 PCUs be physically realized instead of one being shared, the area of the filter bank core would be 2.3 mm$_2$, an increase of 30%. This filter bank core also dissipates 435.5 μW, a 43% in-crease in power. Put simply, the advantages

gained by sharing the same PCU for all channels are significant.

For completeness, the area and power dissipation for the Dual-port RAM is respectively $\sim 0.6\,mm_2$ and 94 $\mu W @1.1$ V, 0.96 MHz. The power dissipation for this memory is relatively high because it is synthesized using flip-flops. The power dissipation of the memory based on the standard 8-transistor dual-port RAM cells would be considerably smaller.

At this juncture, it is instructive to compare our design against reported low-power filter bank designs for hearing aid applications. At this outset, we remark that a comparison of this nature will be somewhat contentious because of the very varied parameters.

We tabulate in Table IV a comparison and make the following comments. First, IFIR filter banks [6] (the pass band bandwidths for each channel are constrained by the prototype filters due to its wavelet-based structure and its bandwidth is ~ 1000 Hz)
The advantage of the proposed filter bank lies in two aspects. One is its flexibility that comes from the careful design of a reconfigurable nonlinear transformation. It provides multiple choices of sound wave decomposition schemes, which makes it capable of meeting the different requirements of different kinds of hearing losses. The other one is that compared with other reconfigurable filter banks, it has smaller delay, which is crucial in practical applications. However, due to the usage of non- linear transformation, the phase response of the whole system is no longer strictly linear. Fortunately, the requirement of linear phase in audio filtering is not as high as that in areas such as image filtering because human is not sensitive to the phase distortion [10].

V. Conclusion

This paper proposed a reconfigurable non-uniform filter bank for hearing aid. The reconfigurable filter bank is based on cosine-modulated filter bank and non-linear transformation. By adjusting the control parameters, four different types of sub band allocations with the same structure are available to supply various sound compensation schemes. Design examples showed that the proposed filter bank has better matching results and smaller group delay than recent approaches. A 16-channel critical band-like spaced micro power (247.5 $\mu W@1.1$ V, 0.96 MHz) small IC area (1.62 mm$_2$ @0.35- μm CMOS) FIR filter bank core for hearing aid applications. We obtained the micro power and small IC area attributes by sharing the proposed PCU between all 16 channels and we take advantage of consecutive zeros in the coefficients of the filter channels. We have verified our filter bank on the basis of computer simulations from an actual layout. We have shown that our design is very competitive against reported designs, and with the added features of higher

stop band attenuation and linear phase frequency response. When compared to a standarddesign of the same specifications, our design dissipates 47% lower power and features 37% smaller IC area.

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