

INSTITUTO TECNOLÓGICO DE COSTA RICA
COMPUTER ENGINEERING ACADEMIC AREA

PROYECTO DE DISEÑO EN INGENIERÍA EN COMPUTADORES



Project Plan

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1 Name of the project

Design of Application Specific Instruction Set Processors (ASIPs) for Approximate Computing

2 Name of the institution

Chair for Embedded System (CES), Karlsruhe Institute of Technology (KIT), Germany, and Laboratorio Sistemas Embebidos y Electrónica Digital (SEED-Lab) del Instituto Tecnológico de Costa Rica

3 Confidentiality requirements

Due to the academic nature of the project, there are no confidentiality requirements, however, there will not be published results during the development of the project but until the end of the work.

4 Problem description

Diseñar ASIPs aproximados para un conjunto de aplicaciones tolerantes a errores.

Design Compiler and Prime Time, Synopsys

ModelSim, Mentor Graphics

ISE, Xilinx + tarjeta Virtex-IV/V

ASIPMeister

CoSy compiler

5 Objectives

5.1 General objectives

To explore the design of Application-Specific Instruction Set Processors (ASIP) to be used in error tolerant applications.

5.2 Specific objectives

The project has the following specific objectives:

1. To select 3 error tolerant applications to be evaluated.
2. To develop at least 3 instances of approximated hardware for tolerant error sections for each of the selected applications.
3. To develop ASIPs configurations using specific approximated instruction.
4. To evaluate, with the use of approximated instructions, a set of applications in terms of execution time, area and power consumption vs the error achieved for the approximated ASIP.

6 Project stakeholders

Since this is an investigation project, there are only a few stakeholders, which are described below:

- Jorge Castro: He is the supervisor of the project, has the general idea about the project itself and guides the course of it. He wants to create new knowledge with the use of ASIPs, so that this area grows and future processes of creating approximated applications become more automated.
- Sajjad Hussain: He works with Jorge Castro on the general guidance of the project, helps with any issue on the server in Germany so that the process of using the software platform (ASIPMeister, Dlxsim and other tools) remains smooth and clear. He has the same interest as Jorge Castro with the project.
- Jeferson González: He is the supervisor in ITCR, helps with any resource assignation of whether space or resources (like the hardware platform) as the person in charge of the SEED laboratory.

7 Solution description

8 Deliverables and criteria of acceptance

The expected deliverables are the following:

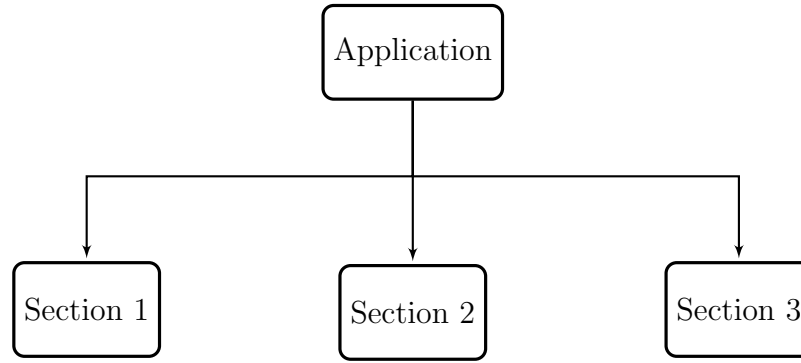


Figure 1: Structure of the Market

Table 1: Deliverables with the corresponding criteria of acceptance

Name	Description	Criteria of acceptance
Requirement 1.1	Instances of approximated hardware	[criterio]
Requirement 2.1	Configuration of approximated ASIPs	[criterio]
Requirement 3.1	Data of execution time, area and power	[criterio]
Requirement 3.2	Comparison and analysis of the obtained results	[criterio]

9 Risky analysis

10 Activities and effort budget

The table 3 takes in consideration a total of 216 engineering hours.

Table 2: Risk analysis

Risk	Probability of occurrence	Impact (hours)	Risk exposure (hours)
Illness or any special medical condition	0.5	8	4
General server errors (missing files, permissions restrictions, etc)	0.6	24	14.4
Delays when acquiring the hardware equipment	0.25	8	2

Table 3: Activities and effort budget

ID	Activity	Engineering hours	Risk reserve (hours)	Total (hours)
001	Get to know the software platform	24	2	26

Table 4: Schedule for the whole project

	Week															
Activity	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Reading the corresponding literature about the project and understanding the general idea of ASIPs																
Execution of the laboratory script to get to know the software tools like ASIPMeister, Dlxsim, etc																

11 Schedule

References