

Advanced Workshop on FPGA-based Systems-On-Chip for Scientific Instrumentation and Reconfigurable Computing



"Laboratory: GPIO IP Cores in PL"

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Objectives

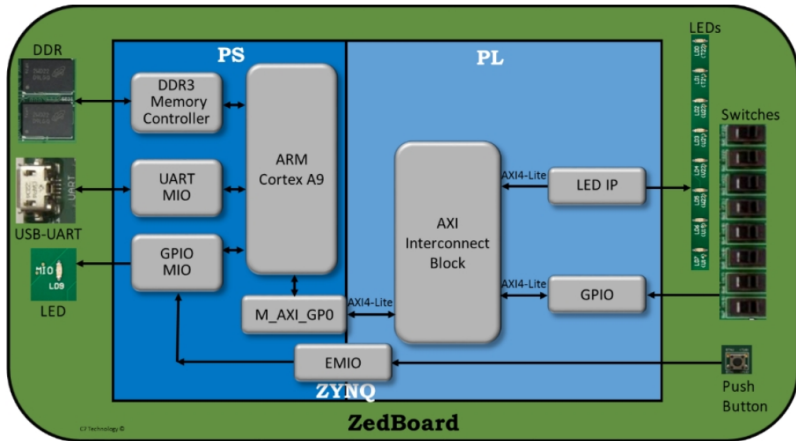
After completing this lab, you will be able to:

- Configure the GP Master port
- Add Xilinx standard IP in the Programmable Logic (PL) section
- Use and route the GPIO signal of the PS into the PL by using EMIO
- Configure some of the 'C' compiler settings in the SDK environment
- Read external inputs and outputs using a 'C' application
- Configure the FPGA from the SDK software
- Test in hardware the design

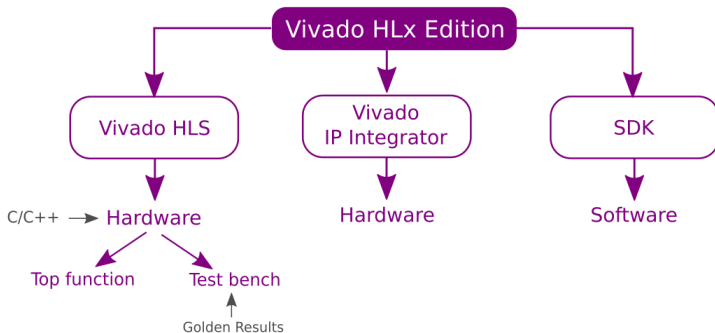
Procedure

You will create a top-level project using Vivado, create the processor system using the IP Integrator, add two instances of the GPIO IP, validate the design, generate the bitstream, export the design to the SDK, create an application in the SDK and test the design in hardware (ZedBoard).

Design Description



Vivado HLx Edition



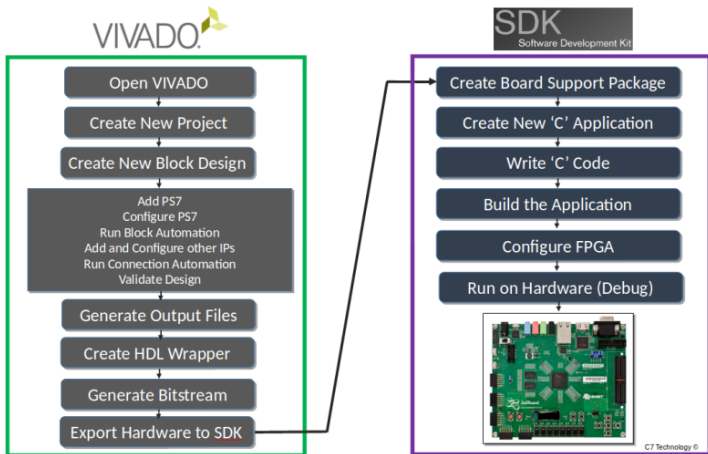
VIVADO[®]
HLx Editions

VIVADO[®]

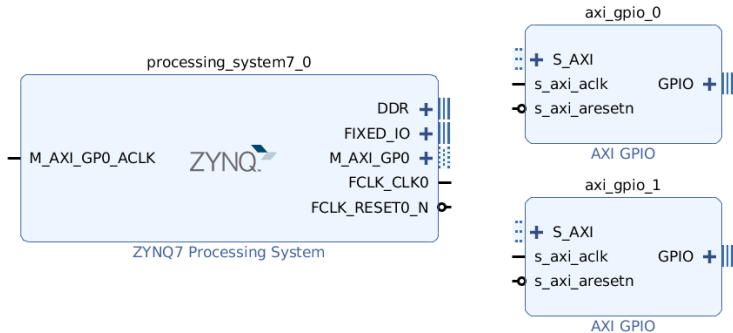


SDK
Software Development Kit

Vivado Design Flow

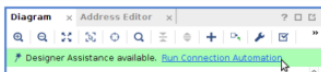
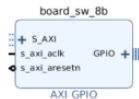
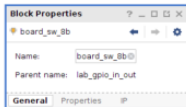


General Steps

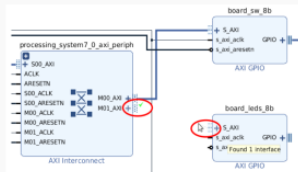


General Steps

SWITCHES

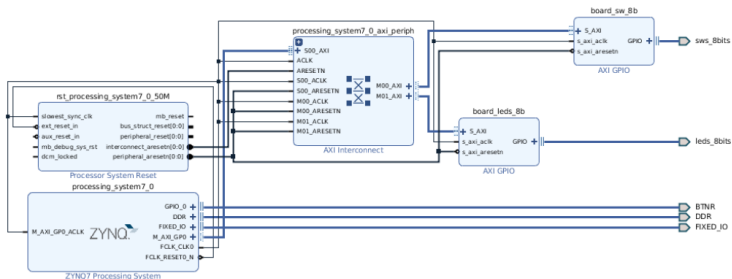


LEDS



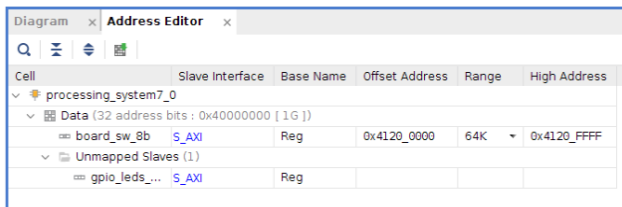
General Steps

Block Diagram



General Steps

Address Editor



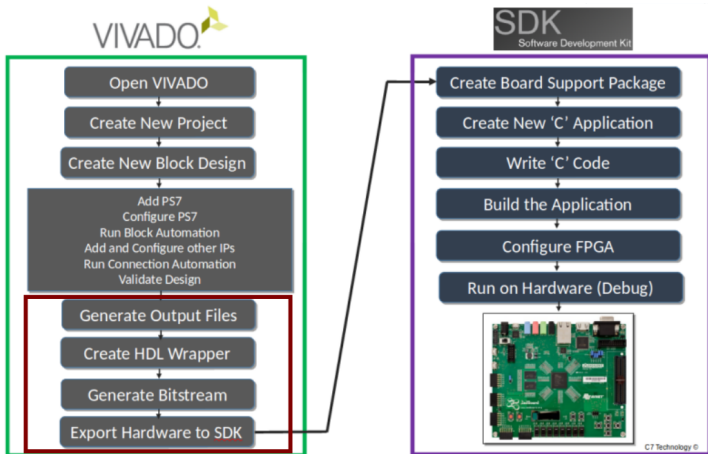
Cell	Slave Interface	Base Name	Offset Address	Range	High Address
processing_system7_0					
Data (32 address bits : 0x40000000 [1 G])					
board_sw_8b	S_AXI	Reg	0x4120_0000	64K	0x4120_FFFF
Unmapped Slaves (1)					
gpio_leds_...	S_AXI	Reg			

General Steps

I/O Ports

I/O Ports									
Name	Dir...	Board Part...	Boar...	Ne...	Package ...	Fixed	Bank	I/O Std	^1
sws_8bits_16670 (8)	IN					<input checked="" type="checkbox"/>	(Multiple)	LVCN0525*	▼
Scalar ports (0)									
sws_8bits_trn_i (8)	IN					<input checked="" type="checkbox"/>	(Multiple)	LVCN0525*	▼
sws_8bits_trn_i[7]	IN	sws_8bits_...			M15 ▼	<input checked="" type="checkbox"/>	34	LVCN0525*	▼
sws_8bits_trn_i[6]	IN	sws_8bits_...			H17 ▼	<input checked="" type="checkbox"/>	35	LVCN0525*	▼
sws_8bits_trn_i[5]	IN	sws_8bits_...			H18 ▼	<input checked="" type="checkbox"/>	35	LVCN0525*	▼
sws_8bits_trn_i[4]	IN	sws_8bits_...			H19 ▼	<input checked="" type="checkbox"/>	35	LVCN0525*	▼
sws_8bits_trn_i[3]	IN	sws_8bits_...			F21 ▼	<input checked="" type="checkbox"/>	35	LVCN0525*	▼
sws_8bits_trn_i[2]	IN	sws_8bits_...			H22 ▼	<input checked="" type="checkbox"/>	35	LVCN0525*	▼
sws_8bits_trn_i[1]	IN	sws_8bits_...			G22 ▼	<input checked="" type="checkbox"/>	35	LVCN0525*	▼
sws_8bits_trn_i[0]	IN	sws_8bits_...			F22 ▼	<input checked="" type="checkbox"/>	35	LVCN0525*	▼
GPIO_57396 (8)	OUT					<input type="checkbox"/>		LVCN0533*	▼
Scalar ports (0)									
led_8bits_trn_o (8)	OUT					<input type="checkbox"/>		LVCN0533*	▼
led_8bits_trn_o[7]	OUT	leds_8bits...			▼	<input type="checkbox"/>		LVCN0533*	▼
led_8bits_trn_o[6]	OUT	leds_8bits...			▼	<input type="checkbox"/>		LVCN0533*	▼
led_8bits_trn_o[5]	OUT	leds_8bits...			▼	<input type="checkbox"/>		LVCN0533*	▼
led_8bits_trn_o[4]	OUT	leds_8bits...			▼	<input type="checkbox"/>		LVCN0533*	▼
led_8bits_trn_o[3]	OUT	leds_8bits...			▼	<input type="checkbox"/>		LVCN0533*	▼
led_8bits_trn_o[2]	OUT	leds_8bits...			▼	<input type="checkbox"/>		LVCN0533*	▼
led_8bits_trn_o[1]	OUT	leds_8bits...			▼	<input type="checkbox"/>		LVCN0533*	▼
led_8bits_trn_o[0]	OUT	leds_8bits...			▼	<input type="checkbox"/>		LVCN0533*	▼

General Steps



Software Development Kit (SDK)

