Notes

Implementation of RISC-V in SME

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Introduction

Add motivation behind whole project

Why RISK-V?, why RISCK-V in physics?, why SME?

Chapter 2

Logic Design

This chapter aims to introduce the reader to the basics of logic design, which will be imperative to the understanding the subsequent chapters. The general structure of this chapter will be based on Appendix A in [2].

We will begin in section 2.1 by introducing the fundamental algebra and the physical building blocks, used to implement the algebra, such as the OR gate.

Hereafter we will be using these building blocks to design and create the core components used in the RISC-V architecture such as the decoder and multiplexer in section 2.2.

2.1 Boolean algebra

The fundamental tool used in logic design is a branch of mathematical logic called Boolean algebra. Compared to elementary algebra, where we deal with variables which represents some real or complex number, in Boolean algebra the variables are viewed as statements or propositions which is either *true* or *false*.

In addition to the variables in elementary algebra we also had a means of manipulating them. These manipulations are called operations which operates on the variables (operands) where the basic operators of algebra consists of $+$, $-$, $\times$ and $\div$.

In Boolean algebra we have a distinction between operators which work on one operand and the ones that work on to two operands. These are called unary and binary operators respectively. We would go through a description of these in the following section.

2.1.1 Unary operators

With a single binary operand p we have 2 possible input *true* and $false$. All output combinations are summarized in table 2.1. Each numbered column here represents an unnamed operator. We will go ahead and describe one of these in the following. The rest can referred to in appendix A.

make ven diagrams to show the operator function

p	1	2	3	4
$true$	$true$	$true$	$false$	$false$
$false$	$true$	$false$	$true$	$false$

Table 2.1: Logic table of possible unary operators. Each numbered column represents an unnamed operator.

Logical complement

For our first basic Boolean operator we have the logical complement operator, which is represented by NOT, !, $\neg$ or $\bar{x}$ in various literature and commonly referred to as the negation operator.

The negation operator inverts an operand such that $\neg true = false$ and $\neg false = true$. Using a table we can neatly represent the complete function of the negation operator. These tables are called *logic tables*.

A logic table has been created for the negation operator as can be seen in table 2.2. The first column represents our proposition and all its possible arguments $true$ and $false$. The second column is then the negated proposition.

p	$\neg p$
$true$	$false$
$false$	$true$

Table 2.2: Logic table of the negation operator where the proposition p, which is either true or false, can be found in the first column. In the second column we find $\neg p$, which is read as NOT p, and its return values.

Summary

We can now go ahead and fill the numbered columns table 2.1 with the corresponding operators which we have defined throughout this section and appendix A. The filled table can be found in table 2.3.

rewrite this section.

p	$T(p)$	$I(p)$	$\neg p$	$F(p)$
$true$	$true$	$true$	$false$	$false$
$false$	$true$	$false$	$true$	$false$

Table 2.3: Logic table of possible unary operators where p is our proposition. Column 2-5 shows the output of the corresponding operator.

2.1.2 Binary operators and disjunctive normal form

With two binary operands, p and q, there exist four possible combinations between their respectable values namely $(true, true)$, $(true, false)$, $(false, true)$, $(false, false)$.

Compared to the previous section we now have 4 possible input values for our yet unnamed operators $X(p, q)$. There exist 16 unique sets of outputs and therefore 16 possible operators. An example of a set of outputs could be

$$X(p, q) = \{true, false, false, false\} \tag{2.1}$$

where $(p, q) = \{(true, true), (true, false), (false, true), (false, false)\}$ is the set of possible inputs.

All output sets are summarized in table 2.4 where each numbered column represents an unnamed operator.

We will in this section start by defining the basic operators from which we will derive the rest. For brevity we will only go through the 3 most commonly used operators, the rest can be referred to in appendix B.

The choice of basic operators is arbitrary but I have chosen the operators for which it is the easiest to derive all other operators, since there exists a method to convert any truth table into a Boolean expression using these which we will get into later.

p	q	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
t	t	t	t	t	t	f	t	f	f	t	t	f	t	f	f	f	f
t	f	t	t	t	f	t	t	t	f	f	f	t	f	t	f	f	f
f	t	t	t	f	t	t	f	t	t	f	t	f	f	f	t	f	f
f	f	t	f	t	t	t	f	f	t	t	f	t	f	f	f	t	f

Table 2.4: Logic table of possible binary operators where $t = true$ and $f = false$. Each numbered column represents an unnamed operator.

Logical conjunction

The logical conjunction operator is represented by $\wedge$ in mathematics; AND, &, && in computer science and a $\cdot$ in electronic engineering and commonly referred to as the AND operator or the logical product. The AND operator only results in a true value if both of the operands are true.

Using table 2.4 we see that the set of outputs which corresponds to this definition is column 12 and is summarized in table 2.5.

Here we have the propositions p and q in the first two columns and all possible permutations between them in the following rows. The last column then shows the resulting value after doing the AND operation between p and q.

p	q	$p \wedge q$
$true$	$true$	$true$
$true$	$false$	$false$
$false$	$true$	$false$
$false$	$false$	$false$

Table 2.5: Logic table of the AND operator where p is the first proposition and q is the second. All possible permutations are then specified in each row for each proposition. The third column then shows the resulting value of the AND operation between p and q.

Logical disjunction

The logical disjunction operator is represented by $\vee$ in mathematics; OR, |, || in computer science and a + in electronic engineering and commonly referred to as the OR operator or the logical sum. The OR operator results in a true value if one or more of the operands are true.

Using table 2.4 we see that the set of outputs which corresponds to this definition is column 2 and is summarized in table 2.6.

Here we have the propositions p and q in the first two columns and all possible permutations between them in the following rows. The last column then shows the resulting value after doing the OR operation between p and q.

p	q	$p \vee q$
$true$	$true$	$true$
$true$	$false$	$true$
$false$	$true$	$true$
$false$	$false$	$false$

Table 2.6: Logic table of the OR operator where p is the first proposition and q is the second. All possible permutations are then specified in each row for each proposition. The third column then shows the resulting value of the OR operation between p and q.

We choose AND, OR and NOT to form our basic or primitive operators from which we will derive all remaining operators.

Exclusive disjunction and disjunctive normal form

The exclusive disjunction is represented by $\veebar$ in mathematics or XOR, ^ in computer science and commonly referred to as the XOR or exclusive OR operator. The XOR operator results in a true value only if the operands differ.

Using table 2.4 we see that the set of outputs which corresponds to this definition is column 7 and is summarized in table 2.7.

Here we have the propositions p and q in the first two columns and all possible permuta-

tions between them in the following rows. The last column then shows the resulting value after doing the XOR operation between p and q.

p	q	$p \veebar q$
$true$	$true$	$false$
$true$	$false$	$true$
$false$	$true$	$true$
$false$	$false$	$false$

Table 2.7: Logic table of the XOR operator where p is the first proposition and q is the second. All possible permutations are then specified in each row for each proposition. The third column then shows the resulting value of the XOR operation between p and q.

We can define this operator in disjunctive normal form, DNF for short, using our basic operators AND, OR and NOT. A logic equation (see section 2.1.3) is said to be in DNF, when it consists of disjunctions between one or more conjunctions, where each of the propositions can be complemented.

To do write our operator in DNF, we first identify all true output in 2.7 namely row 3 and 4. We then take a look at the corresponding input values

$$(p, q) = (true, false) \quad \text{and} \quad (p, q) = (false, true) \tag{2.2}$$

and applying the NOT operator on all the false values. We now have the two tuples

$$(p, \neg q) = (true, \neg false) \quad \text{and} \quad (\neg p, q) = (\neg false, true). \tag{2.3}$$

Hereafter we apply the AND operator between the values in each tuple of input such that

$$p \wedge \neg q = true \wedge \neg false \quad \text{and} \quad \neg p \wedge q = false \wedge \neg true. \tag{2.4}$$

Lastly we apply the OR operators between each tuple and we have the final expression for XOR in terms of the basic operators

$$p \veebar q = (p \wedge \neg q) \vee (\neg p \wedge q). \tag{2.5}$$

The procedure is summarized as follows

1. Find all output values, which are true.
2. Negate all false input for corresponding true output value.
3. Apply AND operator between each value in each input tuple.
4. Lastly apply OR operator between each input tuple.

Using this procedure any logic table can be expressed as a Boolean expression and will be used extensively throughout this thesis.

Summary

We can now go ahead and fill the numbered columns table 2.4 with the corresponding operators which we have defined throughout this section. The filled table can be found in table 2.8.

rewrite this section.

p	q	$\top$	$\vee$	$\leftarrow$	$\rightarrow$	$\uparrow$	$P(p,q)$	$\veebar$	$\neg P(p,q)$	$\leftrightarrow$	$Q(p,q)$	$\neg Q(p,q)$	$\wedge$	$\not\rightarrow$	$\not\leftarrow$	$\downarrow$	$\bot$
t	t	t	t	t	t	f	t	f	f	t	t	f	t	f	f	f	f
t	f	t	t	t	f	t	t	t	f	f	f	t	f	t	f	f	f
f	t	t	t	f	t	t	f	t	t	f	t	f	f	f	t	f	f
f	f	t	f	t	t	t	f	f	t	t	f	t	f	f	f	t	f

Table 2.8: Logic table of binary operators where $t = true$ and $f = false$.

2.1.3 Boolean equations

In the last section we saw that it was possible to describe any logic table in terms of the AND, OR and Negation operators. An example of this could be the following

$$p \veebar q = (p \wedge \neg q) \vee (\neg p \wedge q) \tag{2.6}$$

where p and q was our propositions. Expression 2.6 is an example of a *Boolean equation*.

Like ordinary algebra, Boolean equations satisfy many of the same basic laws of algebra as summarized in table 2.9. Here we see that the laws are exactly equivalent to the version we see with ordinary addition and multiplication, hence the names logical sum $\vee$ and logical product $\wedge$.

Using these laws we can drastically simplify complex expressions which we will use later to greatly reduce the complexity of logic units.

Say we have

$$C = A \cdot \bar{B} \cdot \bar{S} + A \cdot B \cdot \bar{S} + \bar{A} \cdot B \cdot S + A \cdot B \cdot S \tag{2.7}$$

where A, B, C and S are Boolean variables. Notice that $\cdot = \wedge$ and $+ = \vee$, we use this notation since it is much easier to discern the individual terms. Now we can use the distributivity law we found in table 2.9 to pull $A \cdot \bar{S}$ and $B \cdot S$ outside the parentheses

$$C = (\bar{B} + B) \cdot A \cdot \bar{S} + (\bar{A} + A) \cdot B \cdot S. \tag{2.8}$$

Lastly we use the complement law in table 2.10 ($\bar{B} + B = 1$ and $\bar{A} + A = 1$) and the identity law in table 2.9 ($1 \cdot A \cdot \bar{S} = A \cdot \bar{S}$ and $1 \cdot B \cdot S = B \cdot S$) to simplify such that we have

$$C = A \cdot \bar{S} + B \cdot S. \tag{2.9}$$

Notice that we went from using 11 operations in (2.7) to 3 in (2.9) by using the Boolean laws to manipulate the equations, this reduces the complexity of an eventual implementation of the logic equation. Incidentally (2.7) is an example of a multiplexer which we will get into later.

Law	Law of $\vee$	law of $\wedge$
Commutativity	$p \vee q = q \vee p$	$p \wedge q = q \wedge p$
Associativity	$p \vee (q \vee r) = (p \vee q) \vee r$	$p \wedge (q \wedge r) = (p \wedge q) \wedge r$
Distributivity	$p \wedge (q \vee r) = (p \wedge q) \vee (p \wedge r)$	
Identity	$p \vee 0 = p$	$p \wedge 1 = p$
Zero law		$p \wedge 0 = 0$

Table 2.9: Basic Boolean laws. These laws satisfy both Boolean and ordinary algebra.

Law	Law of $\vee$	law of $\wedge$
Distributivity		$p \vee (q \wedge r) = (p \vee q) \wedge (p \vee r)$
One law	$p \vee 1 = 1$	
Idempotence law	$p \vee p = p$	$p \wedge p = p$
Absorption law	$x \vee (x \wedge y) = x$	$x \wedge (x \vee y) = x$
Complement law	$p \vee \neg p = 1$	$p \wedge \neg p = 0$
De Morgan Laws	$\neg p \vee \neg q = \neg(p \wedge q)$	$\neg p \wedge \neg q = \neg(p \vee q)$

Table 2.10: Basic Boolean laws. These laws do not have an equivalent in ordinary algebra.

2.1.4 Gates

In this and following sections the physical abstractions to the propositions *true* and $false$ will be represented by a voltage either being high or low. When the voltage is high we say that the signal is *asserted* and represented by 1 and when low is *deasserted* and represented by 0.

We will use 3 fundamental physical components, *gates*, to implement logic tables or Boolean equations and each of these is represented by a symbol which we will go through in the following.

It should be noted that multiple input are possible with the AND and OR gates since they are both commutative and associative. There will though always be 1 output which is the result of all the subsequent input.

AND Gate

The AND gate is the physical implementation of logic table 2.5 we defined earlier. It is illustrated by the symbol found in figure 2.1.

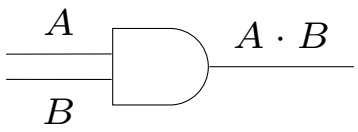


Figure 2.1: Illustration of the AND gate where A and B are the input and $A \cdot B$ is the output.

OR Gate

The OR gate is the physical implementation of logic table 2.6 we defined earlier. It is illustrated by the symbol found in figure 2.2.

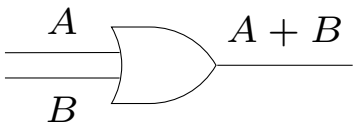


Figure 2.2: Illustration of the OR gate where A and B are the input and $A + B$ is the output.

NOT Gate

The NOT gate or inverter is the physical implementation of logic table 2.2 we defined earlier. It is illustrated by the symbol found in figure 2.3. Usually the inverter is not drawn explicitly, but rather a "bubble" is drawn at the input or output of the respective gate, as shown in figure 2.4.

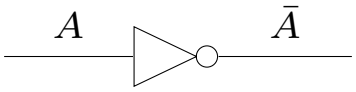


Figure 2.3: Illustration of the NOT gate where A and B are the input and $A + B$ is the output.

maybe talk about that nor and nand gates are universal

2.2 Combinational logic

When we design logic units which contain no memory i.e always return the same output given same input, we deal with *combinational logic*. In this section we will go through the essential combinational logic units that will be used throughout this thesis.

(a) (b)

Figure 2.4: (a) illustrates the inverter explicitly drawn before the input to the AND gate. (b) shows the inverter illustrated as a bubble before the input to the AND gate.

2.2.1 Decoder

The first combinational logic unit we will take a look at will be the *decoder*. Its function is to select one of multiple outputs to assert. This selection is determined by the inputs.

Say that we have 3 inputs i.e 3 bits of information. There are 8 possible configurations of these 3 bits ($2^3 = 8$) and for each configuration we assign one output to be asserted.

In table 2.11 we have for each configuration asserted one output. Notice that we have used the binary representation of a decimal number to determine which output should be asserted for given input configuration. For example the binary representation for the decimal number 5 is 101, so when the input is $In2 = 1$, $In1 = 0$ and $In0 = 1$ output 5 is asserted.

It should be noted that the choice of which output that should get asserted for given input is arbitrary and up to the logic designer to decide, though each input configuration must only assert one unique output.

We had 3 input in the previous example, but we can generalize the decoder such that for n input, where $n > 0$, we have 2^n output. Only one output is asserted per input configuration.

Input			**Output**							
In2	In1	In0	Out7	Out6	Out5	Out4	Out3	Out2	Out1	Out0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

Table 2.11: Logic Table of a 3 input decoder where the binary representation of the input determines which output gets asserted. For example when In2=1, In1=0, In0=1 output 5 will get asserted as the binary representation for 5 is 101.

2.2.2 Multiplexer

When we will later deal with larger systems consisting of multiple logic units, we will need a way to select from which unit we want the output to go further up the chain. This select

unit is known as a *multiplexer* or *mux*. Its function is to select one of multiple input to output unchanged.

In table 2.12 we have constructed a multiplexer with three input one of which is the control signal S. If the control signal is asserted $S = 1$ the output will have the value of B and if deasserted $S = 0$ it will output the value of A.

In this example we only have two input, but the multiplexer can be made such that it can select between arbitrary many input though this requires an increase in control signals. For n control signals we are able to select between 2^n input, where $n > 0$.

A	**B**	**S**	**C**
0	0	0	0
0	1	0	0
1	0	0	1
1	1	0	1
0	0	1	0
0	1	1	1
1	0	1	0
1	1	1	1

Table 2.12: Logic Table of a multiplexer.

2.2.3 Two-level logic

We saw in a previous section that it was possible to express any logic table into a logic equation expressed as a sum of one or more products, also known as *disjunctive normal form* or *Sum of Products*. As we will see shortly this type of logic expression can be implemented using only two levels of logic, one layer consisting only of AND gates and one only of OR Gates, where negations are only applied to individual variables.

In this and next section we will see an example how one would implement various logic units, such as the multiplexer, going from logic table to the sum of products logic equation and lastly generating a gate-level implementation.

Going ahead we will implement the two input multiplexer starting by writing the logic table found in 2.12 in sum of products form. Using the approach mentioned in 2.1.2 we end up with the logic equation for the multiplexer

$$C = A \cdot \bar{B} \cdot \bar{S} + A \cdot B \cdot \bar{S} + \bar{A} \cdot B \cdot S + A \cdot B \cdot S. \tag{2.10}$$

We already saw how one could drastically simplify this expression in section 2.1.3, such that we end up with

$$C = A \cdot \bar{S} + B \cdot S. \tag{2.11}$$

Now we have the simplified two-level representation for the two input multiplexer, in next section we will se how this is used to generate the gate-level implementation.

2.2.4 Programmable logic array

A common two-level logic device used to implement logic equations is the *programmable logic array* or PLA for short. The PLA consists of two lines of input, one unaltered and one complemented (negated input), which are then connected to a plane of AND gates. The connections between the inputs and AND plane of course depends on the to be implemented logic equation. Hereafter the outputs of the AND plane connects to the OR plane and again the connections depends on the logic equation.

Using this logic we can go ahead and implement 2.11. Looking at the equation we see that we need to perform two AND operations and one OR operation. We therefore need two AND gates and one OR gate. Since the PLA has lines for both input and inverted input we only need to connect the correct lines to the corresponding gates. This is done in figure 2.5a where the black dots shows which lines are connected to which gate. When designing larger logic circuits it is more common to omit drawing all gates explicitly, which is illustrated in 2.5b.

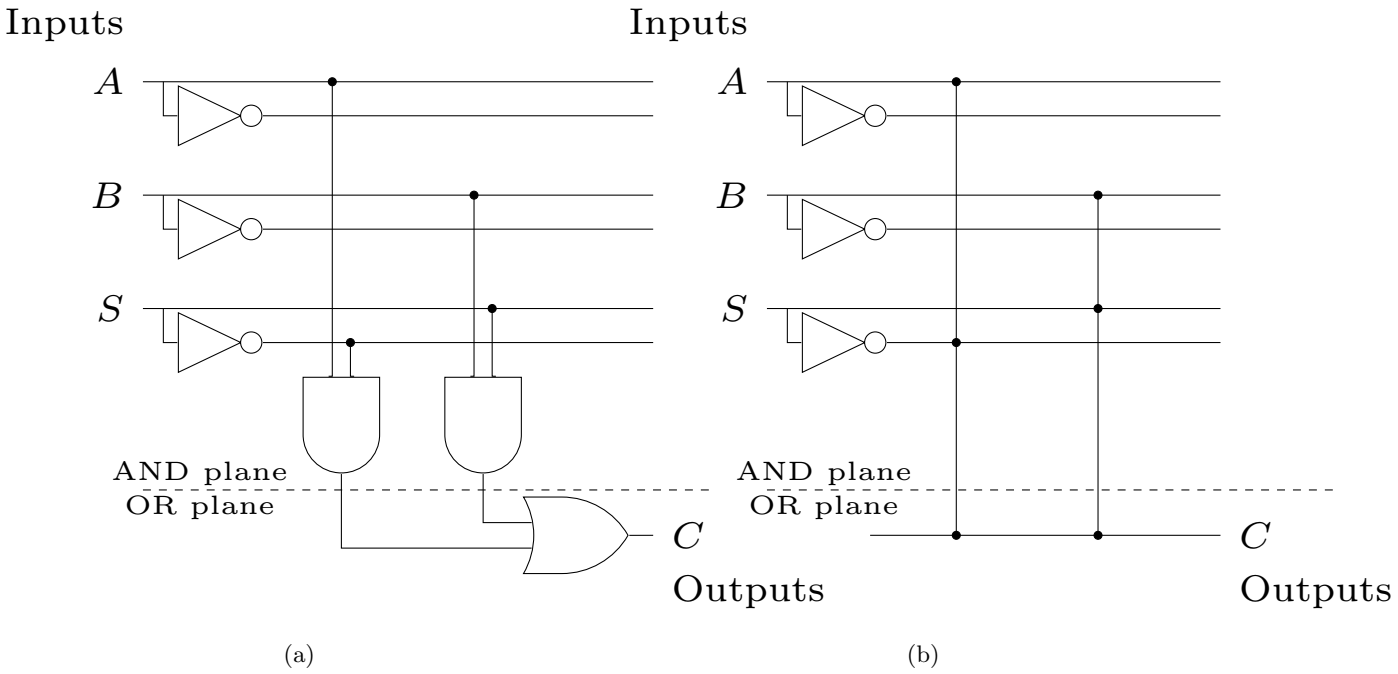


Figure 2.5: Both of these circuits shows the PLA implementation of the logic equation we saw in 2.11. (a) Illustrates the multiplexer with explicitly drawn gates where the black dots indicates a connection. (b) Illustrates the multiplexer with implicitly drawn gates where each vertical line in the AND plane represents a connection to an AND gate and each horizontal line in the OR plane represents a connection to an OR gate. As before the black dots shows which lines are connected.

Chapter 3

Synchronous Message Exchange

In the previous chapter we went through the theory behind logic design, all the way from the introduction of Boolean algebra to gate-level implementation of logic units. We will in this chapter use those ideas to implement logic units in synchronous message exchange (SME). This will serve as a means to introduce SME to the reader and further cement former logic design ideas.

Starting out we will go through a short introduction behind the inspiration for SME, Communicating Sequential Processes. Hereafter we will go through the theory and syntax of SME with an emphasis on real examples, as i believe this is the most efficient manner of introducing SME to the reader.

3.1 Communicating Sequential Processes

Rewrite this section

add examples of a process and channels

When working with multiprocessor workloads one will quickly realize the inconvenience of memory sharing. The non-determinism of having multiple processes reading and writing the same memory often results in unexpected behavior.

A classic example of non-determinism would be the act of printing out the numbers one through ten, to your console using more than one thread. If the aforementioned code is executed multiple times, you will notice that the order of numbers would vary between the runs. This is due to the scheduler of the operating system, which one does not have control over. That can create race conditions (meaning the behavior in your code is dependent on the timing of different threads), which can cause unpredictable behavior and therefore bugs, which is undesirable.

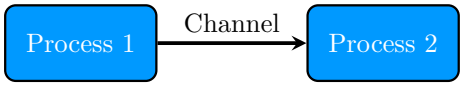
Various attempts has been made to solve this problem, such as the introduction of mutexes or locks. Though it does not solve our problem completely as these ”solutions” introduces deadlocks, which is a state, where multiple processes are waiting for each other and the program stalls indefinitely. These deadlocks might not happen every run and thus intro-

duces another layer of difficulty, as error reproducibility is essential for code debugging and therefore makes it hard to make reliable software.

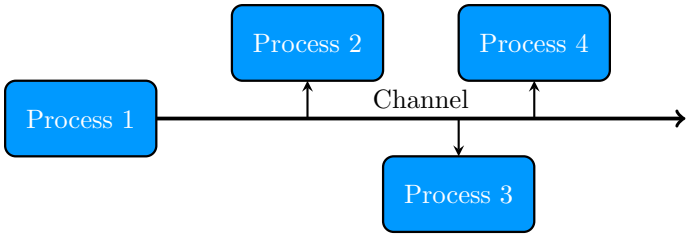
Communicating Sequential Processes (CSP) is an algebra first proposed by Hoare [1] to solve exactly these issues. CSP is build on two very basic primitives one is the process (which should not be confused with operating system processes). A process could be an ordered sequence of operations. These processes do not share any memory, therefore one process cannot access a specific value in another process (which solves the problems we had with shared memory).

The other primitive is channels, which is the way the processes communicate with each other. You can pass whatever you want through these channels, but once you pass the value, the process lose access to it. There are a lot of ways the processes and channels can be arranged. The most simple one can be found in figure 3.1a, which illustrates process 1 passing a value onto a channel which process 2 takes as input. Some different configurations can be found in figures 3.1b-3.1d.

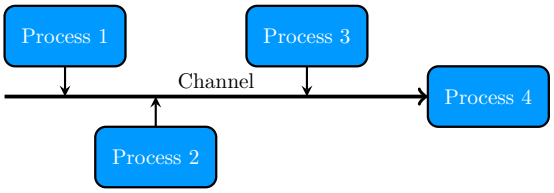
Using these primitives as ones programming paradigm one can design multiprocess workloads without the shared memory problems mentioned earlier. The asynchronous nature of CSP will though be a problem for hardware models, as we will see shortly and is the fundamental inspiration behind synchronous message exchange.



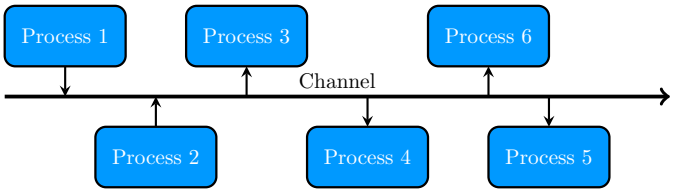
(a) CSP one to one



(b) CSP one to many



(c) CSP many to one



(d) CSP many to many

3.2 Synchronous Message Exchange

The idea of using CSP for hardware modeling was first introduced in Rehr et al. [3] and later further developed in [4], where two students successfully implemented a vector processor using PyCSP (a CSP library for python). They however found a number of shortcomings of using PyCSP for hardware modeling. The need for global synchronicity, when simulating hardware models using CSP, meant that additional channels were needed to simulate clock progress and emulation of latches among others. This caused an explosion of required channels and an unnecessary increase in complexity.

ask where the idea to use csp for hardware came from

They did however find that building isolated processes and then connecting them via channels proved to be a powerful approach for building larger hardware models. As in the unit testing method one can develop and test individual processes to then connecting them together and form larger hardware models.

With this in mind a more suitable message-passing framework for hardware modeling was developed, with the following requirements:

- Globally synchronous
- Broadcasting channels
- Shared nothing
- Implicit latches

all these observations laid the foundation behind synchronous message exchange (SME), Vinter and Skovhede [6]. Since then the SME framework has been implemented in the .Net framework, Skovhede and Vinter [5], which is the version of SME that will be used throughout this thesis.

We will not dwell further into the theory behind SME in this thesis. Instead we will be developing actual units in SME, that will be needed when we later implement the RISC-V architecture. The SME syntax will be introduced as we go through the examples and is intended to be a from-scratch introduction for the uninitiated reader.

3.2.1 SME setup and structure

We will in this section go through the code structure I have decided to use for the development of all logic units. Much thought has been given to this and from previous experience doing code projects I would say it is good practice to think about the general structure of ones project for ease of development and future extensions.

A modular design is essential as many logic units is going to be needed when implementing the RISC-V architecture. This also allows for easy debugging and testing, as individual units

can be addressed before integrating them into a larger system. Each logic unit will also be separated into two files. One which contains all the buses and one which contains the function of the unit. The thought behind this is to help compartmentalize bus declarations from unit function and hopefully ease development.

In the following it is a prerequisite that .Net Core SDK[1] is installed on their respective systems to be able to run the code. All following code examples can be found by clicking here or if reading printed version the full link can be found in this footnote[2].

In the following it should be noted that the equivalent to a channel in CSP, is a bus in SME. Buses however, are able to contain multiple signals/channels.

Project structure example

We are going to build an AND gate for this example and will be the only section were the complete code is shown, as this section is meant to serve as a "quick start guide" for readers beginning their journey into SME. Subsequent sections will only show relevant parts of the code.

For this quick example we are going to start a project in a folder called .../ANDGate/, which is where all shown files are going to be placed. To do this we are going to open up a terminal window and navigate to the desired folder destination (for example the Desktop) and invoke the command:

```
$ dotnet new console -n ANDGate
```

where "ANDGate" can be changed to a name of choice.

Next navigate into the folder

```
$ cd ANDGate
```

and add the necessary SME libraries

```
$ dotnet add package SME --version=0.4.0-beta
$ dotnet add package SME.GraphViz --version=0.4.0-beta
$ dotnet add package SME.Tracer --version=0.4.0-beta
$ dotnet add package SME.VHDL --version=0.4.0-beta
```

There should now exist 3 items inside the ANDGate folder: Program.cs, ANDGate.csproj and a folder called obj. If all went well we should now be able to begin with our project.

I always find drawing a quick flowchart before implementing code gives a nice overview ones project. So in the spirit of this I've drawn out a quick sketch of the project in Figure 3.2, which shows the two processes we are going to create, namely the SME simulator and the AND gate process.

[1] The SDK can be found here https://dotnet.microsoft.com/download

[2] https://github.com/DanielRamyar/Master_Thesis/tree/master/SME_Implementations

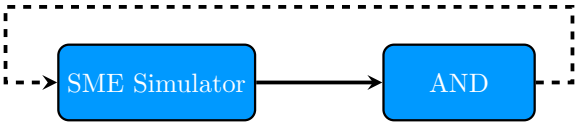


Figure 3.2: Flowchart of AND gate SME project. Here the rectangles represent individual processes, which lies in a file of its own. The solid arrow represents a bus and dashed arrow a bus going to a clocked process.

Opening up the Program.cs file, we are going to add a couple of lines, as shown in Listing 3.1. The Program.cs contains the Main() method of the project and is the entry point of any C# program. To use the SME library we import it with the "using SME" command as shown in the second line.

Within the Main() method, the first function we meet is the using function, this is just to ensure the resources is properly cleaned up after the simulation.

Hereafter we see the simulation object, which as the name implies, is responsible for the simulation of the logic unit. We then pass the simulated input to the ANDgate object, which will then perform the AND operation (it is not necessary to pass the simulation object itself to the ANDGate, but is shown here to not cause confusion about how the simulation passes input values to the AND process). We will see how these objects are defined shortly.

Lastly we can configure the simulator object, which uses fluent syntax. In this case we configured it to build a CSV file, which shows what each bus contained at every clock cycle. We build a graph, which outputs a .dot file that shows how all the processes are connected and we transpile the code to VHDL. It should be noted that Run() should always be the last method called.

The file which contains the Main() will ways be named project.cs in this thesis, but the naming is irrelevant.

```
1  using System;
2  using SME;
3
4  namespace ANDGate {
5      class Program {
6          static void Main(string[] args) {
7              using(var sim = new Simulation()) {
8
9                  var simulator = new ANDGateSimulator();
10                 var ANDcalculator = new ANDGate(simulator.input);
11
12                 sim
13                     .BuildCSVFile()
14                     .BuildGraph()
15                     .BuildVHDL()
16                     .Run();
17             }
18         }
19     }
```

```
20 }
```

Listing 3.1: The Program.cs file, which contains the Main() method for the project.

We are going to need a way to test our AND gate, this is what the simulation file is for and is shown in Listing 3.2. Remember to name your namespace the same as in the project file. The first two definitions inside the simulation process creates or loads the two buses for the test. Notice that the gate output is labeled as an input bus and vice versa for the gate input. This is due to the simulation is a process in and of itself and therefore needs to output the test values to a bus, which the ANDGate process takes in as input.

Now everything within the Run() method is what is going to be simulated and each time we want a new clock cycle to occur, we use the line *await ClockAsync()*. In a simulation process any .Net library is allowed and is not going to get transpiled to a VHDL file. Therefore we can print the output of the AND gate to console to see whether or not it works correctly. We do this by transmitting data via the input bus, which contains two signals, in1 and in2. We then set the two signals to false wait a clock cycle and print the output. Since this is a fairly small system we can test for all input combinations and look at the outputs to see if the gate is behaving correctly.

```
1  using System;
2  using SME;
3
4  namespace ANDGate {
5      public class ANDGateSimulator : SimulationProcess {
6          [InputBus]
7          public readonly GateOutput output = Scope.CreateOrLoadBus<GateOutput>();
8
9          [OutputBus]
10         public readonly GateInputs input = Scope.CreateOrLoadBus<GateInputs>();
11
12         public async override System.Threading.Tasks.Task Run() {
13             Console.WriteLine("Starting test!\n");
14             await ClockAsync();
15
16             input.in_1 = false;
17             input.in_2 = false;
18
19             await ClockAsync();
20             Console.WriteLine($"Gate input: {input.in_1} (Input 1) - {input.in_2} (Input
                   2)\n");
21             Console.WriteLine($"AND gate output: {output.out_AND}");
22             ...
23             Console.WriteLine("Done testing!");
24         }
25     }
26 }
```

Listing 3.2: The simulator file, which specifies how the simulation is run. Most lines in the run method are concatenated brievity.

Hereafter we are going to make our bus declarations in a new file called buses.cs. Looking at Listing 3.3, we see that the bus declarations are made using the interface command, which inherits its fields and methods from the IBus interface. The name for the bus is free of choice and in this case are called GateInputs and GateOuputs respectively.

A bus can contain multiple signals of various types. Since the AND gate evaluates binary values, the bool type has been chosen for the input and output signals. You may have noticed that all the signals have the InitialValue attribute. What this does is that once the bus is created it will contain an initial value. If this is not done one have to be careful not to read the bus before any value has been given to it, as this will crash the program.

Hereafter we have the TopLevelInputBus and TopLevelOuputBus attributes, they tell SME which buses goes in and out of the hardware implementation. Remember that this attribute is only given to buses which interfacing with some outside process, in this case the simulation process. Internal buses should not be given this attribute. By a internal bus we mean a bus which is connecting processes inside the hardware implementation (see Figure 3.5 here the internal buses goes from the NOT gates to the AND gates)

finish this section

```
1  using System;
2  using SME;
3
4  namespace ANDGate {
5      [TopLevelInputBus]
6      public interface GateInputs : IBus {
7          [InitialValue]
8          bool in_1 {get; set;}
9          [InitialValue]
10         bool in_2 {get; set;}
11     }
12
13     [TopLevelOutputBus]
14     public interface GateOutput : IBus {
15         [InitialValue]
16         bool out_AND {get; set;}
17     }
18 }
```

Listing 3.3: The file where all bus declarations are made.

Lastly we are going to define our AND gate in a process class. We create a file called ANDGate.cs, where our process is going to lie. We see how the process is defined in Listing 3.4. In line 5 we define the class ANDGate and since the AND gate is only going to execute once per cycle, we are going to inherit from the SimpleProcess class.

We are then loading our output bus in lines 6-7 and declaring our input bus in lines 9-10. Then I have added a constructor, which checks whether or not the object passed from the simulator object (remember that we passed the simulator inputs in the project file) contains any values.

Finally we have the OnTick method, which contains the logic that has to be performed. In line 16 we perform the logical AND operation between the two input signals and then passing it on to the output. The Ontick method makes sure that the code within runs exactly once per cycle.

```
1  using System;
2  using SME;
3
4  namespace ANDGate {
5      public class ANDGate : SimpleProcess {
6          [OutputBus]
7          public readonly GateOutput output = Scope.CreateOrLoadBus<GateOutput>();
8
9          [InputBus]
10         private readonly GateInputs m_input;
11         public ANDGate(GateInputs input) {
12             m_input = input ?? throw new ArgumentNullException(nameof(input));
13         }
14
15         protected override void OnTick() {
16             output.out_AND = m_input.in_1 && m_input.in_2;
17         }
18     }
19 }
```

Listing 3.4: This is where we define the function of the AND gate process.

Finally one run the project by returning to the terminal. In the directory where the project is placed one simply writes following command

```
1  $ dotnet run
```

this will output 3 files to a folder named output placed in the same directory as the project. These files consist of network.dot, trace.csv and a VHDL folder. The network.dot file is a graphical representation of our model, which we have shown in Figure 3.3. Next we have the trace.csv file, which shows what each signal in all buses contained at each clock cycle. This is a very helpful tool when debugging, as one can quickly identify problems if wrong values are spotted throughout the simulation.

Lastly we the transpiled VHDL files in the VHDL folder, which we can verify using any VHDL simulator (GHDL is recommended). The folder contains a makefile, which automates this process, so you simply navigate to the VHDL folder in your terminal and run the command

```
1          $ dotnet make
```

assuming that you have already installed GHDL on your system.

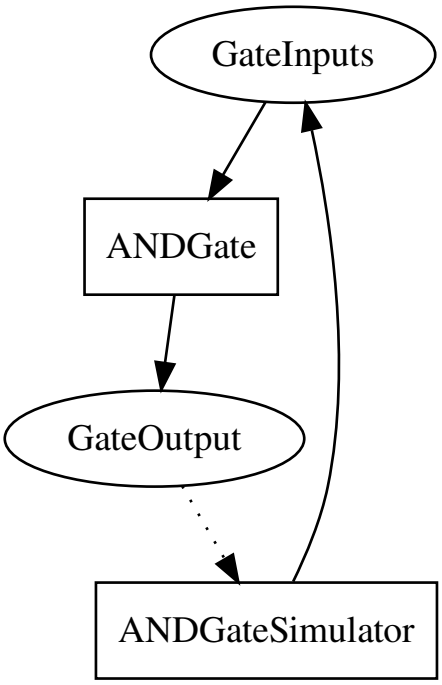


Figure 3.3: Graphical representation of the AND gate generated by the outputted network.dot file. Here rectangles represent processes and ellipses buses. The arrows show the direction of the data flow, where a dotted line indicates data flow to a clocked process, which means that the process is activated on a rising clock edge.

3.2.2 The Decoder

In this section we will start by implementing the 2-bit decoder (see 2.2.1). First we set up the logic table, as shown in Table 3.1. We then derive the logic equation from the table:

$$output = \overline{In1} \cdot \overline{In0} + \overline{In1} \cdot In0 + In1 \cdot \overline{In0} + In1 \cdot In0 \tag{3.1}$$

We notice from Eq. 3.1 that we need two NOT gates, four AND gates and four outputs. Since we only have 1 minterm per output no OR gates are necessary. We can then create a circuit diagram of the decoder, as shown in Figure 3.4 and use it as our design guide when we implement it in SME.

Input		**Output**			
In1	In0	Out3	Out2	Out1	Out0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Table 3.1: Logic Table of a 2 input decoder, where the binary representation of the input determines which output gets asserted. For example when In1=1, In0=0 output 1 will get asserted as the binary representation for 2 is 10.

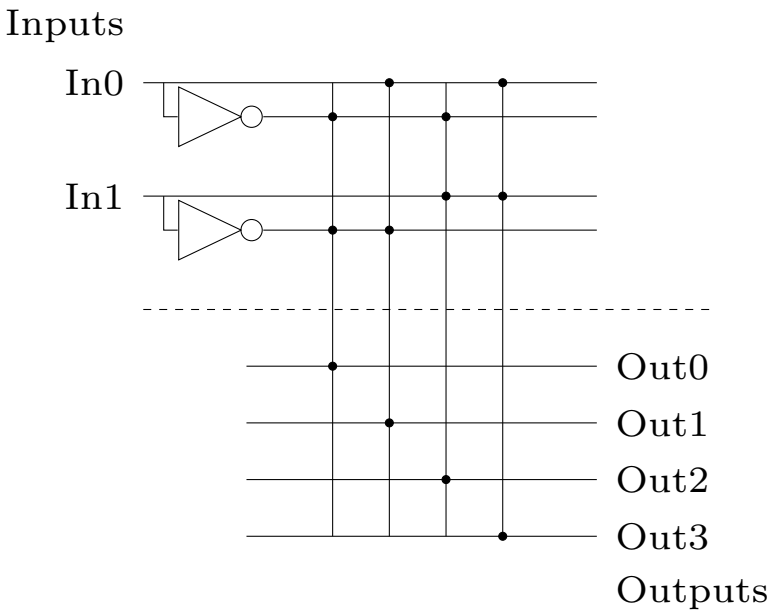


Figure 3.4: Flowchart of AND gate SME project. Here the rectangles represent individual processes, which lies in a file of its own. The solid arrow represents a bus and dashed arrow a bus going to a clocked process.

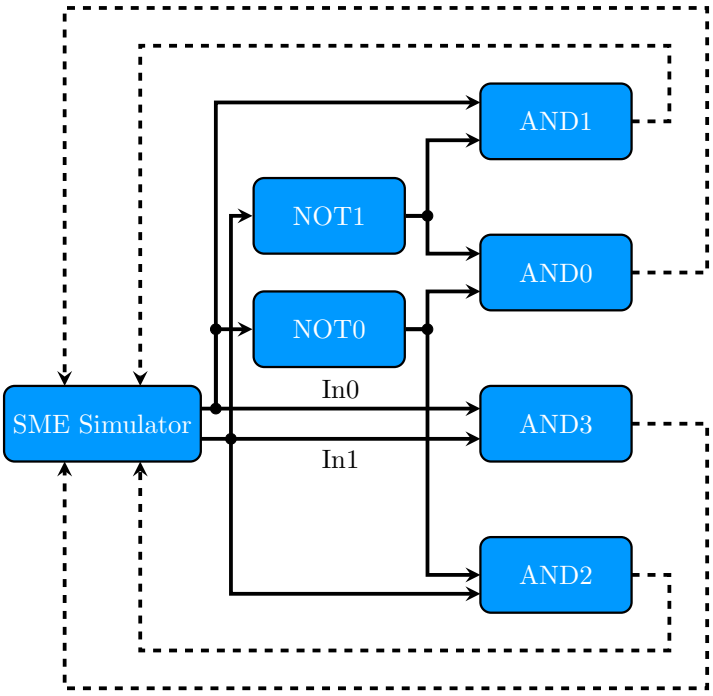


Figure 3.5: Flowchart of decoder SME project. Here the rectangles represent individual processes. The solid arrow represents a bus and the dashed arrow a bus going to a clocked process. Solid dots show extension of the same bus and any crossing lines are not connected

Chapter 4

Introduction to RISC-V instructions

This chapter aims to introduce the reader to the basics of machine language. Based on chapter 2 in [2]

Chapter sections are subject to change in name and order

4.1 RISC-V Assembly

4.2 Operands

4.2.1 Register

4.2.2 Memory Format

4.2.3 Const vs imm

4.3 Numeral system of a computer

4.3.1 base 2

4.3.2 signed unsigned

4.4 Instruction representation in binary

4.5 Operators

Chapter 5

The RISC-V processor

This chapter aims to introduce the reader to the basics of machine language. Based on chapter 4 in [2]

Chapter sections are subject to change in name and order

5.1 Single Cycle RISC-V Units

make a better title

5.1.1 Program Counter

5.1.2 Instruction Memory

5.1.3 incrementor?

figure out a name for this subsection

5.1.4 Register

5.1.5 Arithmetic Logic Unit (ALU)

5.1.6 Immediate generator

5.1.7 Data Memory

Need to figure out more sections to explain whole datapath

5.2 Designing the Control

5.3 Single Cycle RISC-V datapath

5.4 Improving the datapath

figure out better naming for sections

5.4.1 RV64I Base Instructions Support

5.4.2 Supporting R-Format

5.4.3 Supporting I-Format

5.4.4 Supporting S-Format

5.4.5 Supporting B-Format

5.4.6 Supporting U-Format

5.4.7 Supporting J-Format

5.5 Debugging the instructions

5.5.1 Writing assembly to test instructions

5.5.2 Writing simple C code to run on RISC-V

Chapter 6

Conclusion and future work

Appendix A

Unary Operators

Logical identity

Hereafter we have the logical identity operator which we will represent as the function $I(x)$. The logical identity operator takes an argument and returns it as is.

A logic table for the identity operator has been created and can be found in table A.1. In the first column we find our preposition p and its arguments. In the second column we find the return values of the identity operator with the prepositions as the argument $I(p)$.

p	$I(p)$
$true$	$true$
$false$	$false$

Table A.1: Logic table of the identity operator where the proposition p, which is either true or false, can be found in the first column. In the second column we find $I(p)$, which is the identity operator with p as its argument, and its return values.

Logical true

Next we have logical true which we will represent as the function $T(x)$. Logical true takes an argument and always returns true.

A logic table for the true operator has been created and can be found in table A.2. In the first column we find our preposition p and its arguments. In the second column we find the return values of the true operator with the prepositions as the argument $T(p)$.

p	$T(p)$
$true$	$true$
$false$	$true$

Table A.2: Logic table of the true operator where the proposition p, which is either true or false, can be found in the first column. In the second column we find $T(p)$, which is the true operator with p as its argument, and its return values.

Logical false

Lastly we have logical false which we will represent as the function $F(x)$. Logical false takes an argument and always return false.

A logic table for the false operator has been created and can be found in table A.3. In the first column we find our preposition p and its arguments. In the second column we find the return values of the false operator with the prepositions as the argument $F(p)$.

p	$F(p)$
$true$	$false$
$false$	$false$

Table A.3: Logic table of the false operator where the proposition p, which is either true or false, can be found in the first column. In the second column we find $F(p)$, which is the false operator with p as its argument, and its return values.

Appendix B

Binary Operators

Joint denial

Joint denial is represented by $\downarrow$ in mathematics or NOR in computer science and commonly referred to as the NOR operator. The NOR operator results in a true value only if both operands are false.

Using table 2.4 we see that the set of outputs which corresponds to this definition is column 15 and is summarized in table B.1.

Here we have the propositions p and q in the first two columns and all possible permutations between them in the following rows. The last column then shows the resulting value after doing the NOR operation between p and q.

p	q	$p \downarrow q$
$true$	$true$	$false$
$true$	$false$	$false$
$false$	$true$	$false$
$false$	$false$	$true$

Table B.1: Logic table of the NOR operator where p is the first proposition and q is the second. All possible permutations are then specified in each row for each proposition. The third column then shows the resulting value of the NOR operation between p and q.

In disjunctive normal form the NOR operator can be expressed in the following form

$$p \downarrow q = (\neg p \wedge \neg q) \tag{B.1}$$

using the procedure mentioned in chapter 2.1.

Alternative denial

Alternative denial is represented by $\uparrow$ in mathematics or NAND in computer science and commonly referred to as the NAND operator. The NAND operator results in a true value

only if one or more of the operands are false.

Using table 2.4 we see that the set of outputs which corresponds to this definition is column 5 and is summarized in table B.2.

Here we have the propositions p and q in the first two columns and all possible permutations between them in the following rows. The last column then shows the resulting value after doing the NAND operation between p and q.

p	q	$p \uparrow q$
$true$	$true$	$false$
$true$	$false$	$true$
$false$	$true$	$true$
$false$	$false$	$true$

Table B.2: Logic table of the NAND operator where p is the first proposition and q is the second. All possible permutations are then specified in each row for each proposition. The third column then shows the resulting value of the NAND operation between p and q.

In disjunctive normal form the NAND operator can be expressed in the following form

$$p \uparrow q = (p \wedge \neg q) \vee (\neg p \wedge q) \vee (\neg p \wedge \neg q) \tag{B.2}$$

using the procedure mentioned in chapter 2.1.

Logical biconditional

The logical biconditional is represented by $\leftrightarrow$ in mathematics or XNOR in computer science and commonly referred to as the exclusive NOR operator. The XNOR operator results in a true value only if both operands are either true or false.

Using table 2.4 we see that the set of outputs which corresponds to this definition is column 9 and is summarized in table B.3.

Here we have the propositions p and q in the first two columns and all possible permutations between them in the following rows. The last column then shows the resulting value after doing the XNOR operation between p and q.

p	q	$p \leftrightarrow q$
$true$	$true$	$true$
$true$	$false$	$false$
$false$	$true$	$false$
$false$	$false$	$true$

Table B.3: Logic table of the XNOR operator where p is the first proposition and q is the second. All possible permutations are then specified in each row for each proposition. The third column then shows the resulting value of the XNOR operation between p and q.

In disjunctive normal form the XNOR operator can be expressed in the following form

$$p \leftrightarrow q = (p \wedge q) \vee (\neg p \wedge \neg q) \tag{B.3}$$

using the procedure mentioned in chapter 2.1.

Tautology

The tautology operator is represented by $\top$ in mathematics which always returns a true value.

Using table 2.4 we see that the set of outputs which corresponds to this definition is column 1 and is summarized in table B.4.

Here we have the propositions p and q in the first two columns and all possible permutations between them in the following rows. The last column then shows the resulting value after doing the tautology operation between p and q.

p	q	$p \top q$
$true$	$true$	$true$
$true$	$false$	$true$
$false$	$true$	$true$
$false$	$false$	$true$

Table B.4: Logic table of the tautology operator where p is the first proposition and q is the second. All possible permutations are then specified in each row for each proposition. The third column then shows the resulting value of the tautology operation between p and q.

In disjunctive normal form the tautology operator can be expressed in the following form

$$p \top q = (p \wedge q) \vee (p \wedge \neg q) \vee (\neg p \wedge q) \vee (\neg p \wedge \neg q) \tag{B.4}$$

using the procedure mentioned in chapter 2.1.

Contradiction

The contradiction operator is represented by $\perp$ in mathematics which always returns a false value.

Using table 2.4 we see that the set of outputs which corresponds to this definition is column 16 and is summarized in table B.5.

Here we have the propositions p and q in the first two columns and all possible permutations between them in the following rows. The last column then shows the resulting value after doing the contradiction operator between p and q.

In disjunctive normal form the contradiction operator can be expressed in the following

p	q	$p \perp q$
$true$	$true$	$false$
$true$	$false$	$false$
$false$	$true$	$false$
$false$	$false$	$false$

Table B.5: Logic table of the contradiction operator where p is the first proposition and q is the second. All possible permutations are then specified in each row for each proposition. The third column then shows the resulting value of the contradiction operation between p and q.

form

$$p \perp q = p \wedge \neg p \tag{B.5}$$

Proposition P

We will define the operator Proposition P which results in a true value only if the first operand p is true.

Using table 2.4 we see that the set of outputs which corresponds to this definition is column 6 and is summarized in table B.6.

Here we have the propositions p and q in the first two columns and all possible permutations between them in the following rows. The last column then shows the resulting value after doing the proposition P between p and q.

p	q	$P(p,q)$
$true$	$true$	$true$
$true$	$false$	$true$
$false$	$true$	$false$
$false$	$false$	$false$

Table B.6: Logic table of the proposition P operator where p is the first proposition and q is the second. All possible permutations are then specified in each row for each proposition. The third column then shows the resulting value of the proposition P operation between p and q.

In disjunctive normal form the proposition P can be expressed in the following form

$$P(p,q) = (p \wedge q) \vee (p \wedge \neg q) \tag{B.6}$$

using the procedure mentioned in chapter 2.1.

Proposition Q

We will define the operator Proposition Q which results in a true value only if the second operand q is true.

Using table 2.4 we see that the set of outputs which corresponds to this definition is column 10 and is summarized in table B.7.

Here we have the propositions p and q in the first two columns and all possible permutations between them in the following rows. The last column then shows the resulting value after doing the proposition Q between p and q.

p	q	$Q(p,q)$
$true$	$true$	$true$
$true$	$false$	$false$
$false$	$true$	$true$
$false$	$false$	$false$

Table B.7: Logic table of the proposition P operator where p is the first proposition and q is the second. All possible permutations are then specified in each row for each proposition. The third column then shows the resulting value of the proposition P operation between p and q.

In disjunctive normal form the proposition Q can be expressed in the following form

$$P(p,q) = (p \wedge q) \vee (\neg p \wedge q) \tag{B.7}$$

using the procedure mentioned in chapter 2.1.

Negated P

We will define the operator negated P which results in a true value only if the first operand p is false.

Using table 2.4 we see that the set of outputs which corresponds to this definition is column 8 and is summarized in table B.8.

Here we have the propositions p and q in the first two columns and all possible permutations between them in the following rows. The last column then shows the resulting value after doing the negated P between p and q.

p	q	$\neg P(p,q)$
$true$	$true$	$false$
$true$	$false$	$false$
$false$	$true$	$true$
$false$	$false$	$true$

Table B.8: Logic table of the negated P operator where p is the first proposition and q is the second. All possible permutations are then specified in each row for each proposition. The third column then shows the resulting value of the negated P operation between p and q.

In disjunctive normal form the negated P can be expressed in the following form

$$\neg P(p,q) = (\neg p \wedge q) \vee (\neg p \wedge \neg q) \tag{B.8}$$

using the procedure mentioned in chapter 2.1.

Negated Q

We will define the operator negated Q which results in a true value only if the second operand q is false.

Using table 2.4 we see that the set of outputs which corresponds to this definition is column 11 and is summarized in table B.9.

Here we have the propositions p and q in the first two columns and all possible permutations between them in the following rows. The last column then shows the resulting value after doing the negated Q between p and q.

p	q	$\neg Q(p,q)$
$true$	$true$	$false$
$true$	$false$	$true$
$false$	$true$	$false$
$false$	$false$	$true$

Table B.9: Logic table of the negated Q operator where p is the first proposition and q is the second. All possible permutations are then specified in each row for each proposition. The third column then shows the resulting value of the negated operation between p and q.

In disjunctive normal form the negated Q can be expressed in the following form

$$\neg Q(p,q) = (p \wedge \neg q) \vee (\neg p \wedge \neg q) \tag{B.9}$$

using the procedure mentioned in chapter 2.1.

Material implication

Material implication is represented by $\rightarrow$ in mathematics. The material implication operator results in a false value only if the first operand p is true and second operand q is false.

Using table 2.4 we see that the set of outputs which corresponds to this definition is column 4 and is summarized in table B.10.

Here we have the propositions p and q in the first two columns and all possible permutations between them in the following rows. The last column then shows the resulting value after doing the material implication operation between p and q.

In disjunctive normal form the material implication operator can be expressed in the following form

$$p \rightarrow q = (p \wedge q) \vee (\neg p \wedge q) \vee (\neg p \wedge \neg q) \tag{B.10}$$

using the procedure mentioned in chapter 2.1.

p	q	$p \rightarrow q$
$true$	$true$	$true$
$true$	$false$	$false$
$false$	$true$	$true$
$false$	$false$	$true$

Table B.10: Logic table of the material implication operator where p is the first proposition and q is the second. All possible permutations are then specified in each row for each proposition. The third column then shows the resulting value of the material implication operation between p and q.

Converse implication

Converse implication is represented by $\leftarrow$ in mathematics. The converse implication operator results in a false value only if the first operand p is true and the second q is true.

Using table 2.4 we see that the set of outputs which corresponds to this definition is column 3 and is summarized in table B.11.

Here we have the propositions p and q in the first two columns and all possible permutations between them in the following rows. The last column then shows the resulting value after doing the converse implication operation between p and q.

p	q	$p \leftarrow q$
$true$	$true$	$true$
$true$	$false$	$true$
$false$	$true$	$false$
$false$	$false$	$true$

Table B.11: Logic table of the converse implication operator where p is the first proposition and q is the second. All possible permutations are then specified in each row for each proposition. The third column then shows the resulting value of the converse implication operation between p and q.

In disjunctive normal form the converse implication operator can be expressed in the following form

$$p \leftarrow q = (p \wedge q) \vee (p \wedge \neg q) \vee (\neg p \wedge \neg q) \tag{B.11}$$

using the procedure mentioned in chapter 2.1.

Material nonimplication

Material nonimplication is represented by $\not\rightarrow$ in mathematics. The material nonimplication operator results in a true value only if the first operand p is true and the second operand q is false.

Using table 2.4 we see that the set of outputs which corresponds to this definition is column 13 and is summarized in table B.12.

Here we have the propositions p and q in the first two columns and all possible permutations between them in the following rows. The last column then shows the resulting value after doing the material nonimplication operation between p and q.

p	q	$p \not\rightarrow q$
$true$	$true$	$false$
$true$	$false$	$true$
$false$	$true$	$false$
$false$	$false$	$false$

Table B.12: Logic table of the material nonimplication operator where p is the first proposition and q is the second. All possible permutations are then specified in each row for each proposition. The third column then shows the resulting value of the material nonimplication operation between p and q.

In disjunctive normal form the material nonimplication operator can be expressed in the following form

$$p \rightarrow q = p \wedge \neg q \tag{B.12}$$

using the procedure mentioned in chapter 2.1.

Converse nonimplication

Converse nonimplication is represented by $\not\leftarrow$ in mathematics. The converse nonimplication operator results in a true value only if the first operand p is false and the second operand q is true.

Using table 2.4 we see that the set of outputs which corresponds to this definition is column 14 and is summarized in table B.13.

Here we have the propositions p and q in the first two columns and all possible permutations between them in the following rows. The last column then shows the resulting value after doing the converse nonimplication operation between p and q.

p	q	$p \not\leftarrow q$
$true$	$true$	$false$
$true$	$false$	$false$
$false$	$true$	$true$
$false$	$false$	$false$

Table B.13: Logic table of the converse nonimplication operator where p is the first proposition and q is the second. All possible permutations are then specified in each row for each proposition. The third column then shows the resulting value of the converse nonimplication operation between p and q.

In disjunctive normal form the converse nonimplication operator can be expressed in the following form

$$p \leftarrow q = \neg p \wedge q \tag{B.13}$$

using the procedure mentioned in chapter 2.1.

Risc V Reference Card

Instruction Formats

31 25	24 20	19 15	14 12	11 7	6 0	
funct7	rs2	rs1	funct3	rd	opcode	R-type
imm[11:0]		rs1	funct3	rd	opcode	I-type
imm[11:6]	imm[5:0]	rs1	funct3	rd	opcode	I-type*
imm[11:5]	rs2	rs1	funct3	imm[4:0]	opcode	S-type
imm[12|10:5]	rs2	rs1	funct3	imm[4:1|11]	opcode	B-type
imm[31:12]				rd	opcode	U-type
imm[20|10:1|11|19:12]				rd	opcode	J-type

* This is a special case of the RV64I I-type format used by slli, srli and srai instructions where the lower 6 bits in the immediate are used to determine the shift amount (shamt). If slliw, srliw and sraiw are used it should generate an error if imm[6] $\neq 0$

RV64I Base Instructions

Name	Fmt	Opcode	Funct3	Funct7/ imm[11:5]	Assembly	Description (in C)
Add	R	0110011	000	0000000	add rd, rs1, rs2	rd = rs1 + rs2
Subtract	R	0110011	000	0100000	sub rd, rs1, rs2	rd = rs1 − rs2
AND	R	0110011	111	0000000	and rd, rs1, rs2	rd = rs1 & rs2
OR	R	0110011	110	0000000	or rd, rs1, rs2	rd = rs1 | rs2
XOR	R	0110011	100	0000000	xor rd, rs1, rs2	rd = rs1 ^ rs2
Shift Left Logical	R	0110011	001	0000000	sll rd, rs1, rs2	rd = rs1 ≪ rs2
Set Less Than	R	0110011	010	0000000	slt rd, rs1, rs2	rd = (rs1 < rs2)?1:0
Set Less Than (U)*	R	0110011	011	0000000	sltu rd, rs1, rs2	rd = (rs1 < rs2)?1:0
Shift Right Logical	R	0110011	101	0000000	srl rd, rs1, rs2	rd = rs1 ≫ rs2
Shift Right Arithmetic†	R	0110011	101	0100000	sra rd, rs1, rs2	rd = rs1 ≫ rs2
Add Word	R	0111011	000	0000000	addw rd, rs1, rs2	rd = rs1 + rs2
Subtract Word	R	0111011	000	0100000	subw rd, rs1, rs2	rd = rs1 − rs2
Shift Left Logical Word	R	0111011	001	0000000	sllw rd, rs1, rs2	rd = rs1 ≪ rs2
Shift Right Logical Word	R	0111011	101	0000000	srlw rd, rs1, rs2	rd = rs1 ≫ rs2
Shift Right Arithmetic Word†	R	0111011	101	0100000	sraw rd, rs1, rs2	rd = rs1 ≫ rs2
Add Immediate	I	0010011	000		addi rd, rs1, imm	rd = rs1 + imm
AND Immediate	I	0010011	111		and rd, rs1, imm	rd = rs1 & imm
OR Immediate	I	0010011	110		or rd, rs1, imm	rd = rs1 | imm
XOR Immediate	I	0010011	100		xor rd, rs1, imm	rd = rs1 ^ imm
Shift Left Logical Immediate	I	0010011	001	0000000	slli rd, rs1, shamt	rd = rs1 ≪ shamt
Shift Right Logical Immediate	I	0010011	101	0000000	srli rd, rs1, shamt	rd = rs1 ≫ shamt
Shift Right Arithmetic Immediate†	I	0010011	101	0100000	srai rd, rs1, shamt	rd = rs1 ≫ shamt
Set Less Than Immediate	I	0010011	010		slti rd, rs1, imm	rd = (rs1 < imm)?1:0
Set Less Than Immediate (U)*	I	0010011	011		sltiu rd, rs1, imm	rd = (rs1 < imm)?1:0
Add Immediate Word	I	0011011	000		addiw rd, rs1, imm	rd = rs1 + imm
Shift Left Logical Immediate Word	I	0011011	001	0000000	slliw rd, rs1, shamt	rd = rs1 ≪ shamt
Shift Right Logical Immediate Word	I	0011011	101	0000000	srliw rd, rs1, shamt	rd = rs1 ≫ shamt
Shift Right Arithmetic Imm Word†	I	0011011	101	0100000	sraiw rd, rs1, shamt	rd = rs1 ≫ shamt
Load Byte	I	0000011	000		lb rd, rs1, imm	rd = M[rs1+imm][0:7]
Load Half	I	0000011	001		lh rd, rs1, imm	rd = M[rs1+imm][0:15]
Load Word	I	0000011	010		lw rd, rs1, imm	rd = M[rs1+imm][0:31]
Load Doubleword	I	0000011	011		ld rd, rs1, imm	rd = M[rs1+imm][0:63]
Load Byte (U)*	I	0000011	100		lbu rd, rs1, imm	rd = M[rs1+imm][0:7]
Load Half (U)*	I	0000011	101		lhu rd, rs1, imm	rd = M[rs1+imm][0:15]
Load Word (U)*	I	0000011	110		lwu rd, rs1, imm	rd = M[rs1+imm][0:31]
Store Byte	S	0100011	000		sb rs1, rs2, imm	M[rs1+imm][0:7] = rs2[0:7]
Store Half	S	0100011	001		sh rs1, rs2, imm	M[rs1+imm][0:15] = rs2[0:15]
Store Word	S	0100011	010		sw rs1, rs2, imm	M[rs1+imm][0:31] = rs2[0:31]
Store Doubleword	S	0100011	011		sd rs1, rs2, imm	M[rs1+imm][0:63] = rs2[0:63]
Branch If Equal	B	1100011	000		beq rs1, rs2, imm	if(rs1 == rs2) PC += imm
Branch Not Equal	B	1100011	001		bne rs1, rs2, imm	if(rs1 != rs2) PC += imm
Branch Less Than	B	1100011	100		blt rs1, rs2, imm	if(rs1 < rs2) PC += imm
Branch Greater Than Or Equal	B	1100011	101		bge rs1, rs2, imm	if(rs1 ≥ rs2) PC += imm
Branch Less Than (U)*	B	1100011	110		bltu rs1, rs2, imm	if(rs1 < rs2) PC += imm
Branch Greater Than Or Equal (U)*	B	1100011	111		bgeu rs1, rs2, imm	if(rs1 ≥ rs2) PC += imm
Load Upper Immediate	U	0110111			lui rd, imm	rd = imm ≪ 12
Add Upper Immediate To PC	U	0010111			auipc rd, imm	rd = PC + (imm ≪ 12)
Jump And Link	J	1101111			jal rd, imm	rd = PC + 4; PC += imm
Jump And Link Register	I	1100111	000		jalr rd, rs1, imm	rd = PC + 4; PC = rs1 + imm

*Assumes values are unsigned integers and zero extends † Fills in with sign bit during right shift and msb (most significant bit) extends

RV64M Standard Extension Instructions

Name	Fmt	Opcode	Funct3	Funct7	Assembly	Description (in C)
Multiply	R	0110011	000	0000001	mul rd, rs1, rs2	rd = (rs1 · rs2)[63:0]
Multiply Upper Half	R	0110011	001	0000001	mulh rd, rs1, rs2	rd = (rs1 · rs2)[127:64]
Multiply Upper Half Sign/Unsigned†	R	0110011	010	0000001	mulhsu rd, rs1, rs2	rd = (rs1 · rs2)[127:64]
Multiply Upper Half (U)*	R	0110011	011	0000001	mulhu rd, rs1, rs2	rd = (rs1 · rs2)[127:64]
Divide	R	0110011	100	0000001	div rd, rs1, rs2	rd = rs1 / rs2
Divide (U)*	R	0110011	101	0000001	divu rd, rs1, rs2	rd = rs1 / rs2
Remainder	R	0110011	110	0000001	rem rd, rs1, rs2	rd = rs1 % rs2
Remainder (U)*	R	0110011	111	0000001	remu rd, rs1, rs2	rd = rs1 % rs2
Multiply Word	R	0111011	000	0000001	mulw rd, rs1, rs2	rd = (rs1 · rs2)[63:0]
Divide Word	R	0111011	100	0000001	divw rd, rs1, rs2	rd = rs1 / rs2
Divide Word (U)*	R	0111011	101	0000001	divuw rd, rs1, rs2	rd = rs1 / rs2
Remainder Word	R	0111011	110	0000001	remw rd, rs1, rs2	rd = rs1 % rs2
Remainder Word (U)*	R	0111011	111	0000001	remuw rd, rs1, rs2	rd = rs1 % rs2

*Assumes values are unsigned integers and zero extends † Multiply with one operand signed and the other unsigned

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