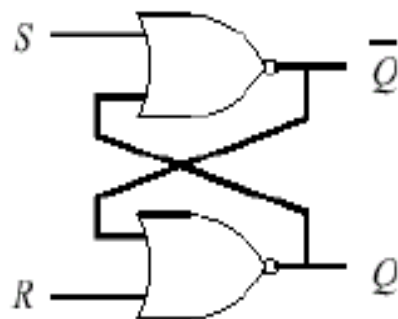
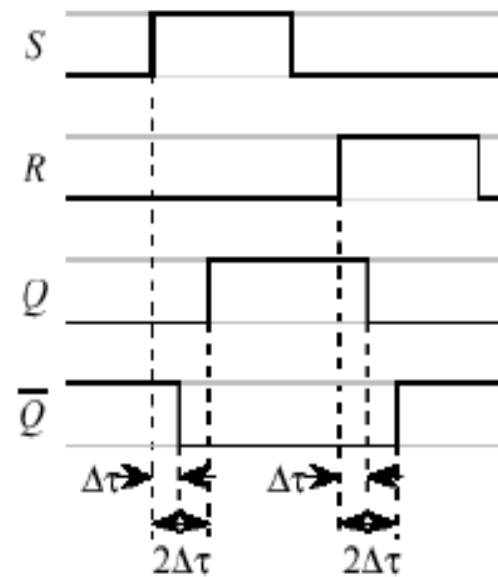


# Latch tipo S-R



$Q_i$	$S_i$	$R_i$	$Q_{i+1}$
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	(disallowed)
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	(disallowed)



Timing Behavior

# Latch RS

(a) Tabela característica

Entradas correntes	Estado corrente	Próximo estado
SR	$Q_n$	$Q_{n+1}$
00	0	0
00	1	1
01	0	0
01	1	0
10	0	1
10	1	1
11	0	—
11	1	—

(b) Tabela característica simplificada

S	R	$Q_{n+1}$
0	0	$Q_n$
0	1	0
1	0	1
1	1	—

(c) Resposta para uma série de entradas

$t$	0	1	2	3	4	5	6	7	8	9
S	1	0	0	0	0	0	0	0	1	0
R	0	0	0	1	0	0	1	0	0	0
$Q_{n+1}$	1	1	1	0	0	0	0	0	1	1

# O Latch RS: resumo do funcionamento

R	S	Q	Q'	ação
1	0	0	1	vai para o estado reset
0	0	0	1	mantém o estado reset (= mantém estado anterior)
0	1	1	0	vai para o estado set
0	0	1	0	mantém o estado set (= mantém estado anterior)
1	1	0	0	estado proibido

**tabela de transição  
de estados**

R	S	$Q_{t+1}$	comentário
0	0	$Q_t$	mantém estado anterior
0	1	1	estado set
1	0	0	estado reset
1	1	-	proibido

## Diagrama de estados

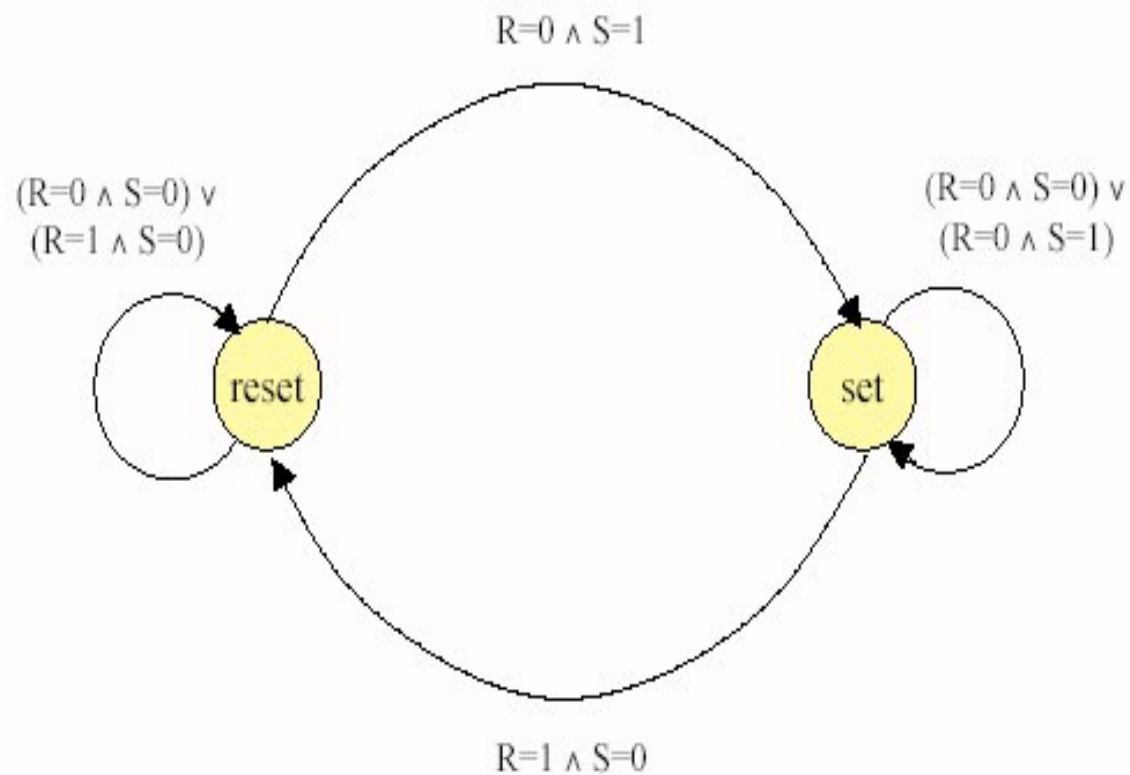


tabela de transição  
de estados

R	S	$Q_{t+1}$
0	0	$Q_t$
0	1	1
1	0	0
1	1	-

# O Latch RS Controlado

símbolo

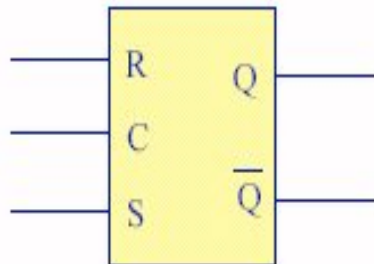
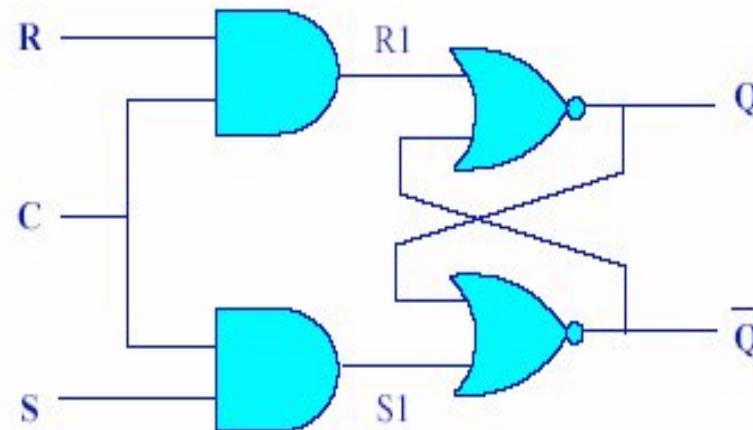


tabela de transição  
de estados

circuito com portas nor e and



C	R	S	$Q_{t+1}$	comentário
0	X	X	$Q_t$	mantém estado anterior
1	0	0	$Q_t$	mantém estado anterior
1	0	1	1	estado set
1	1	0	0	estado reset
1	1	1	-	proibido



# Diagrama de estados

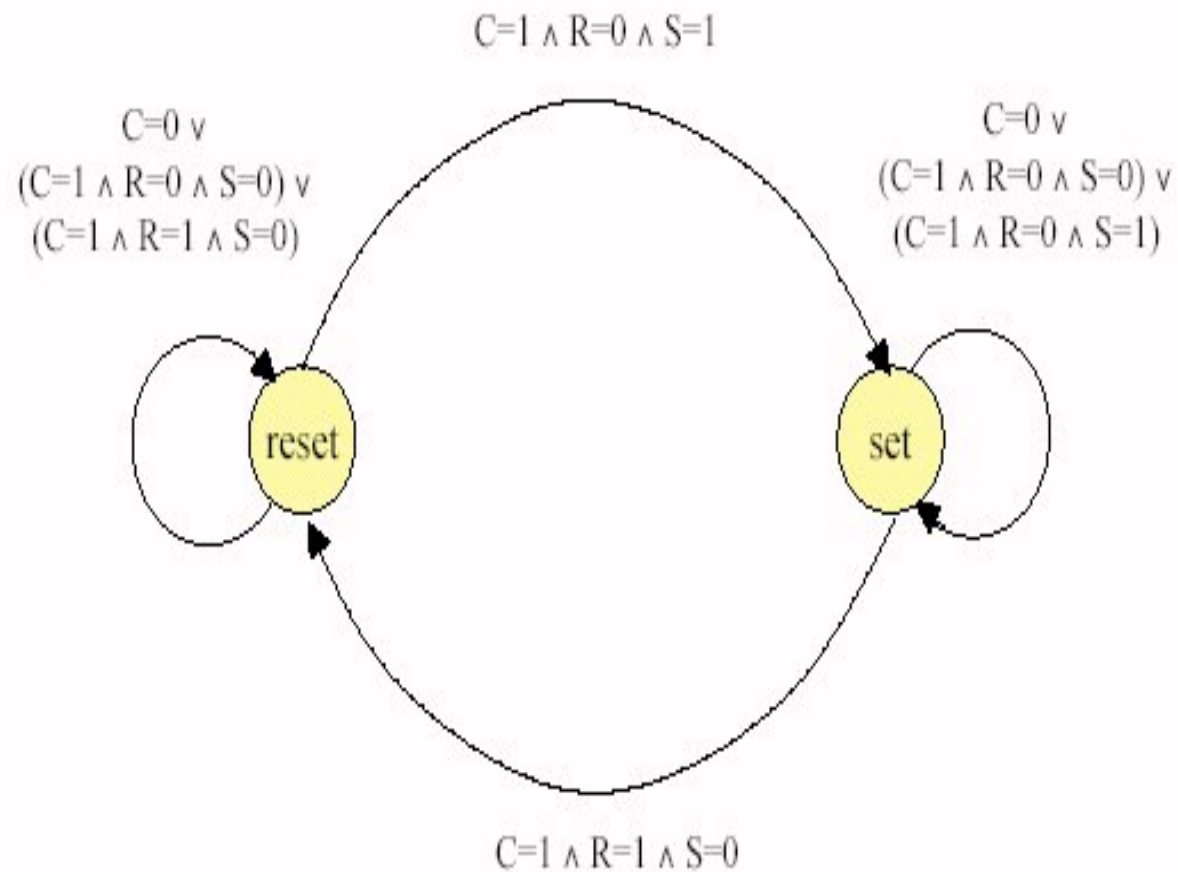


tabela de transição de estados

C	R	S	$Q_{t+1}$
0	X	X	$Q_t$
1	0	0	$Q_t$
1	0	1	1
1	1	0	0
1	1	1	-

## Latch SR usando portas NAND

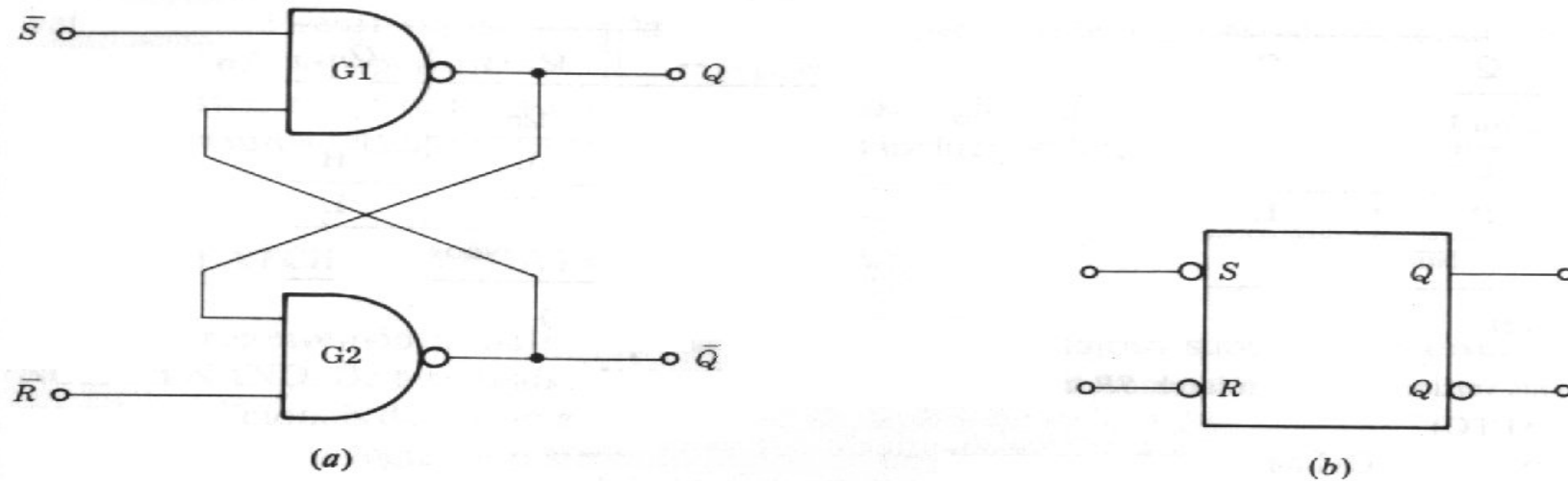


Fig. 4.3-1 Um latch usando portas NAND: (a) diagrama lógico e (b) símbolo lógico.

$\bar{S}$	$\bar{R}$	$Q$	$\bar{Q}$
L	L	Não usada	
L	H	H	L
H	L	L	H
H	H	L ou H	H ou L

(a)

$\bar{S}$	$\bar{R}$	$Q_{n+1}$	$\bar{Q}_{n+1}$
L	L	Não usada	
L	H	H	L
H	L	L	H
H	H	$Q_n$	$\bar{Q}_n$

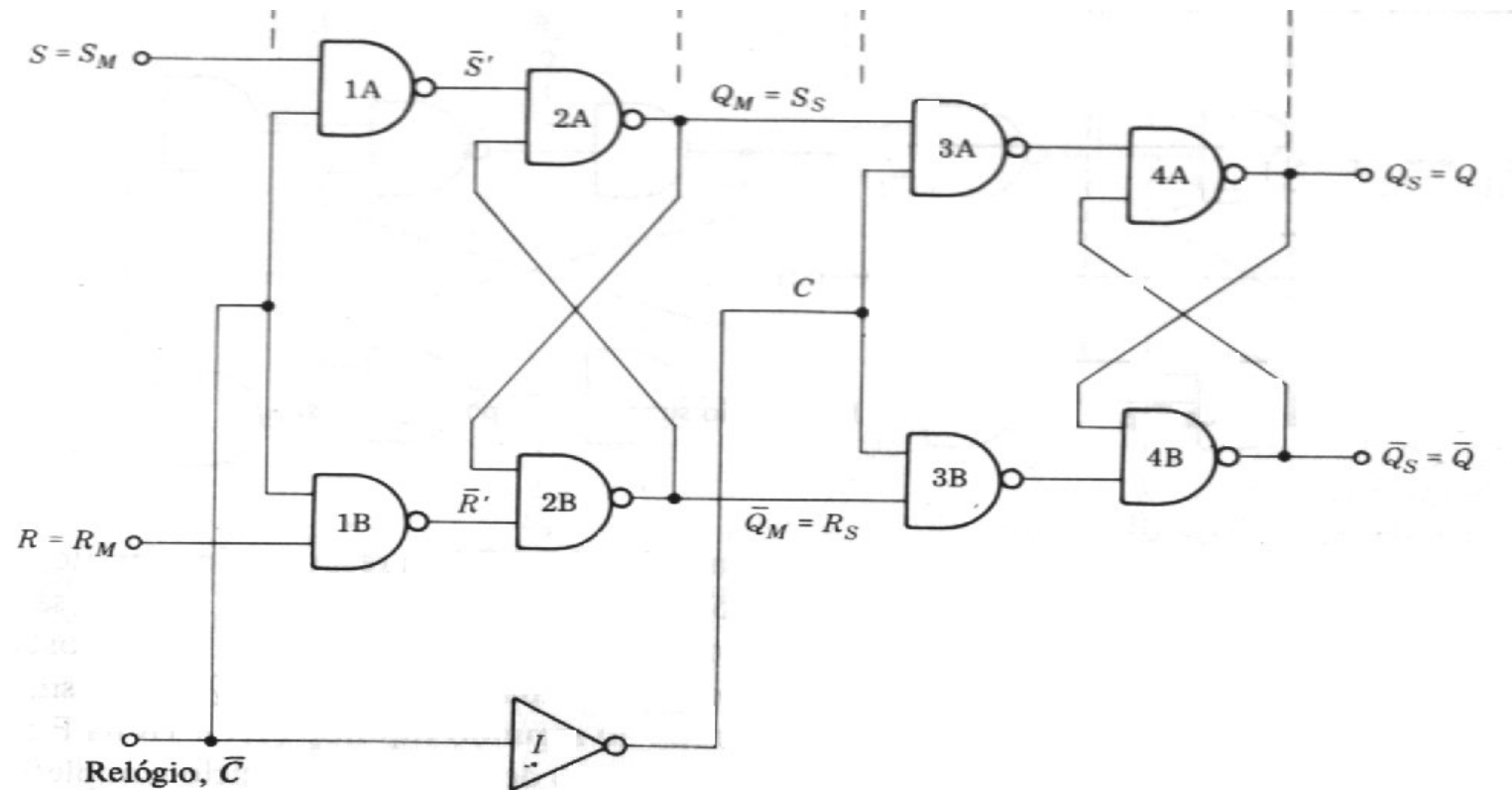
(b)

Fig. 4.3-2 Tabelas verdade para um latch SR com portas NAND.

(H = ALTO)

(L = BAIXO)

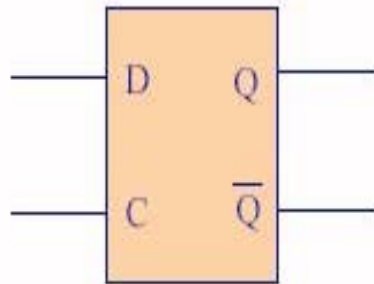
## Flip -flop mestre escravo





# O Latch D

símbolo



circuito a partir do latch RS controlado

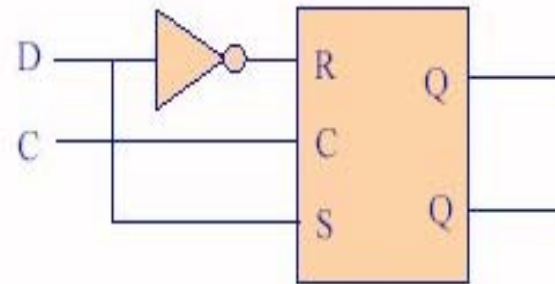
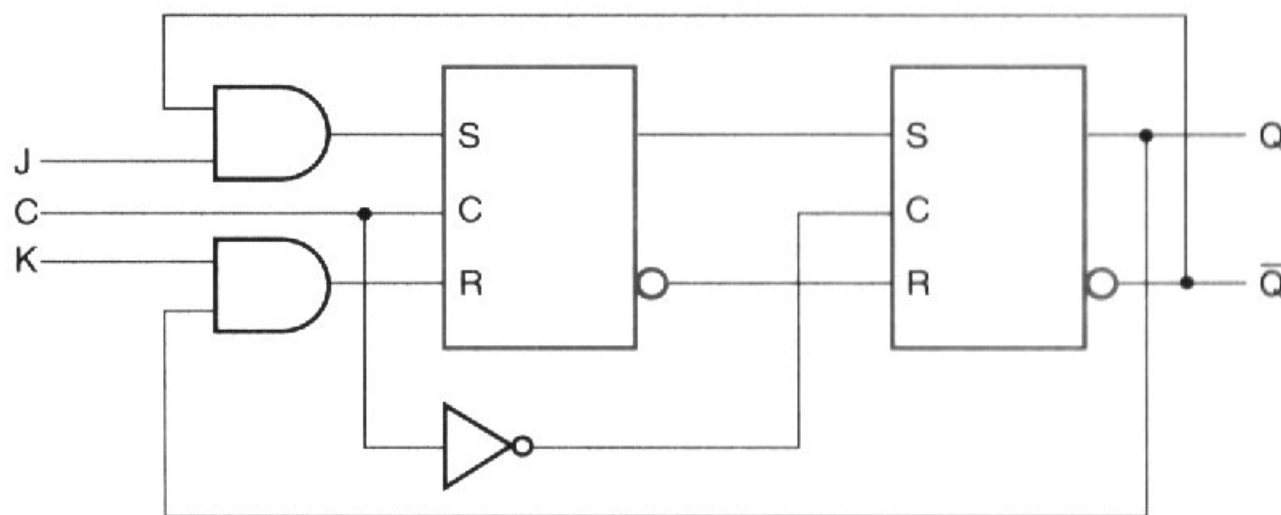


tabela de transição  
de estados

C	D	$Q_{t+1}$	comentário
0	X	$Q_t$	mantém estado anterior
1	0	0	estado reset
1	1	1	estado set

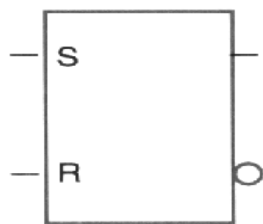


(a)

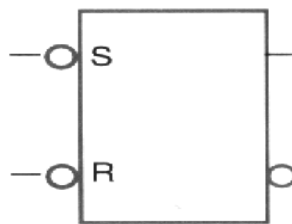
		Next State of Q
J	K	
0	0	Q
0	1	0
1	0	1
1	1	$\bar{Q}$

(b)

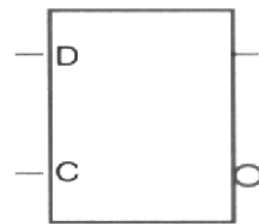
□ **FIGURE 4-12**  
Master-Slave *JK* Flip-Flop



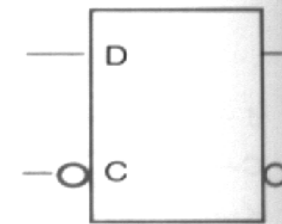
SR



$\overline{S}\overline{R}$

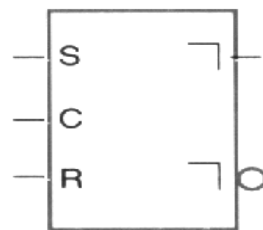


D with 1 Control

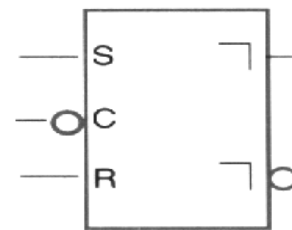


D with 0 Control

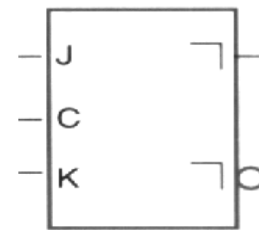
(a) Latches



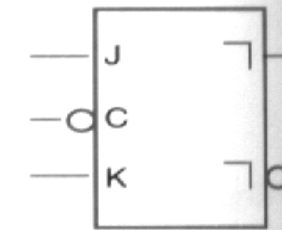
Triggered SR



Triggered SR

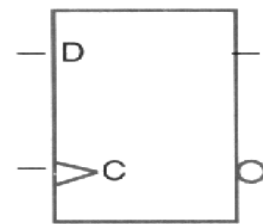


Triggered JK

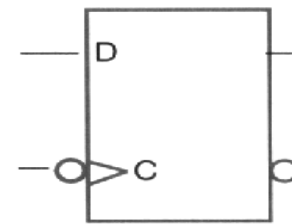


Triggered JK

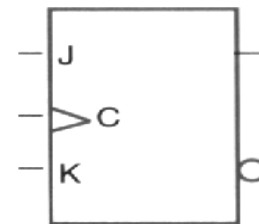
(b) Master-Slave Flip-Flops



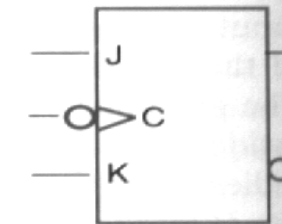
Triggered D



Triggered D



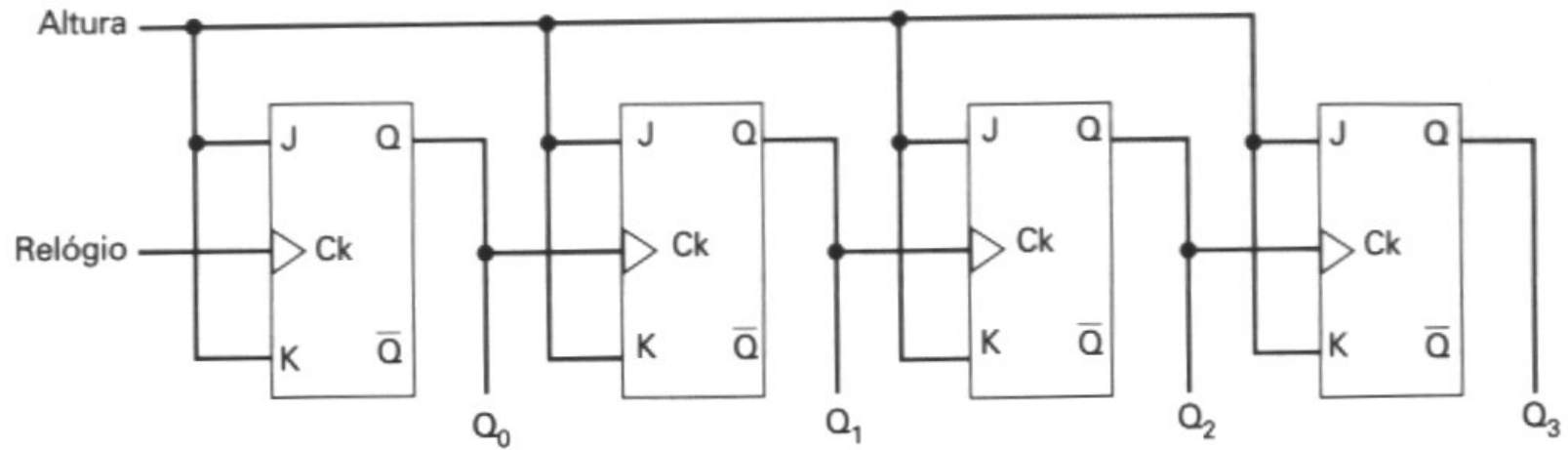
Triggered JK



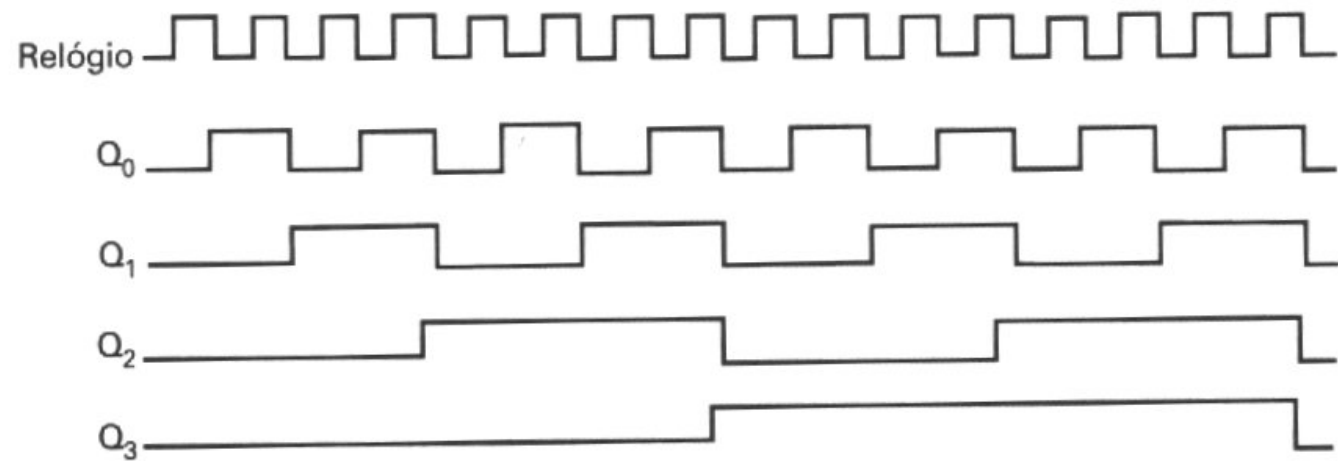
Triggered JK

(c) Edge-Triggered Flip-Flops

# Contador Assíncrono

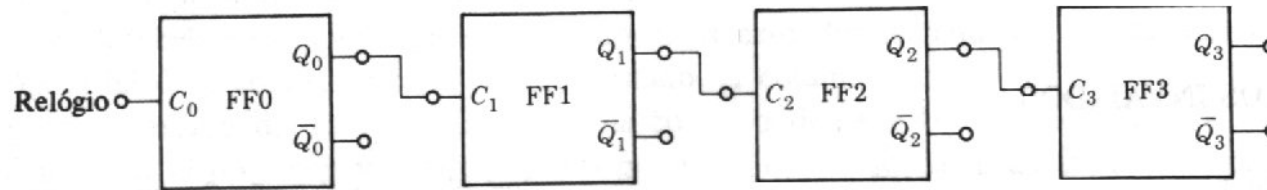


(a) Circuito seqüencial

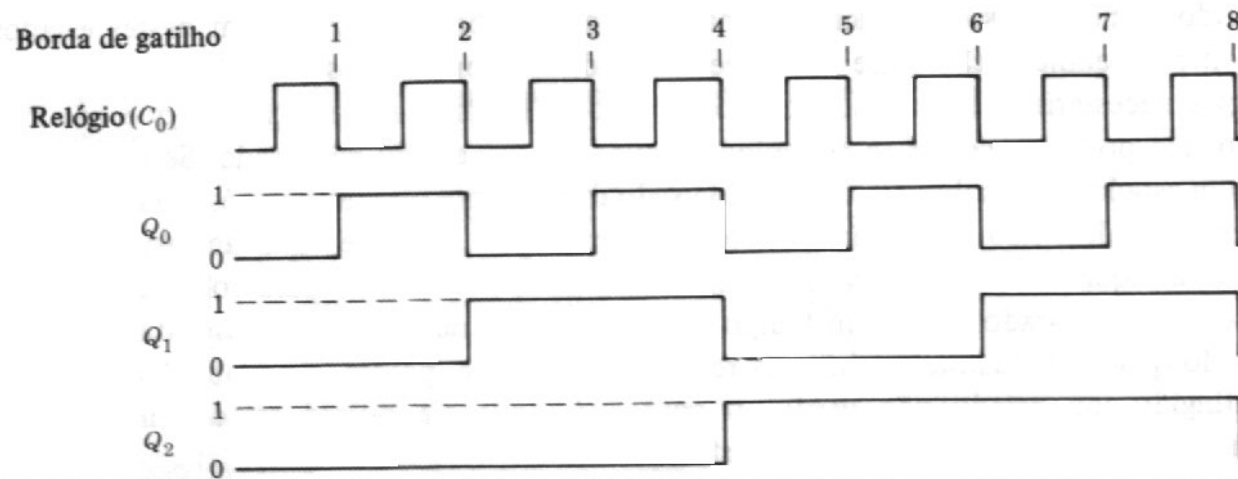


(b) Diagrama de tempo

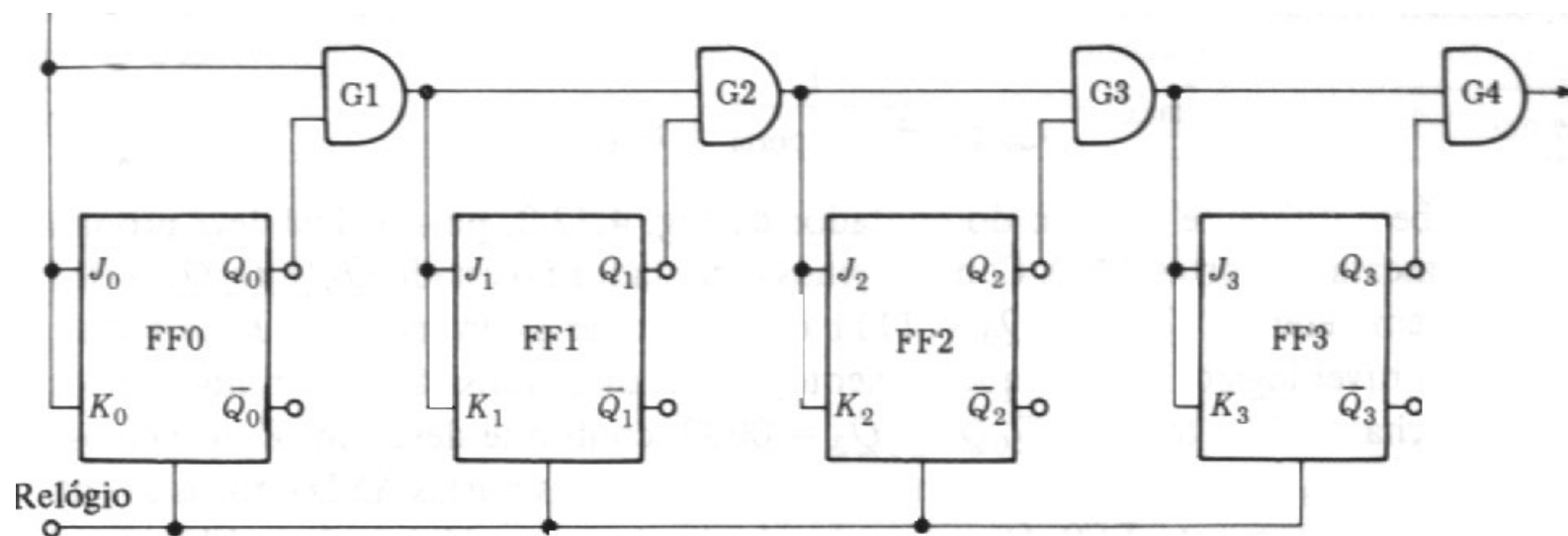
# Contador Assíncrono



(a)

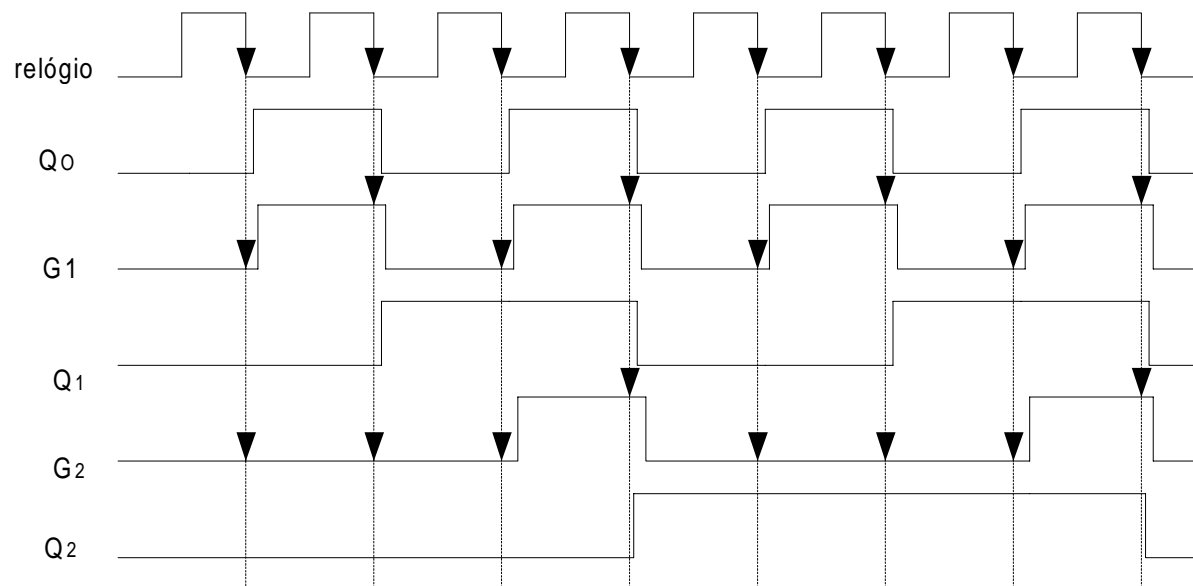


## Contador síncrono

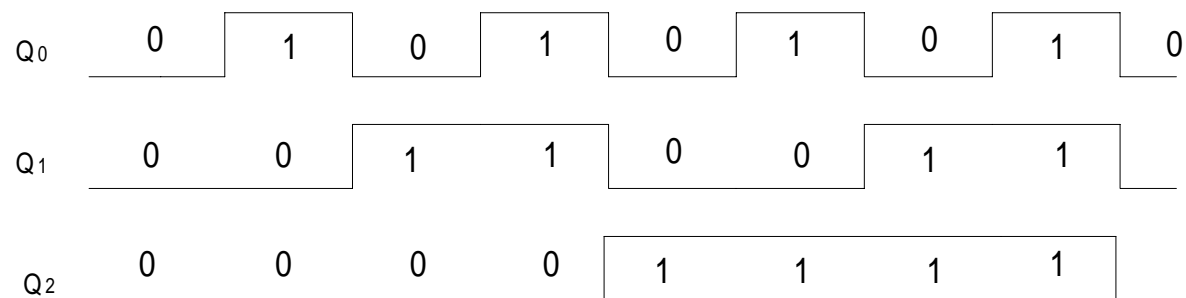




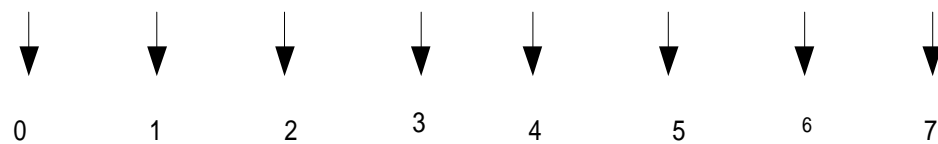
FUNCIONAMENTO DO CONTADOR SÍNCRONO:  
 AMOSTRAGEM FEITA PELA TRANSIÇÃO NEGATIVA,  
 FLIP-FLOP TIPO J-K:  
 $J=0$  e  $K=0 \Rightarrow$  A SAÍDA MANTÉM O VALOR ANTERIOR  
 $J=1$  e  $K=1 \Rightarrow$  A SAÍDA inverte O VALOR ANTERIOR

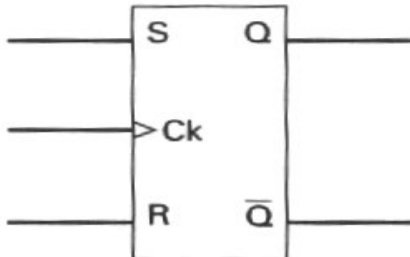
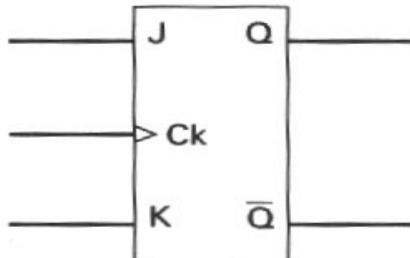
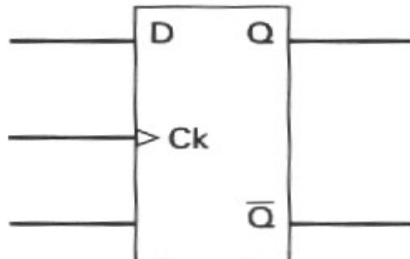


NÚMERO EM BINÁRIO

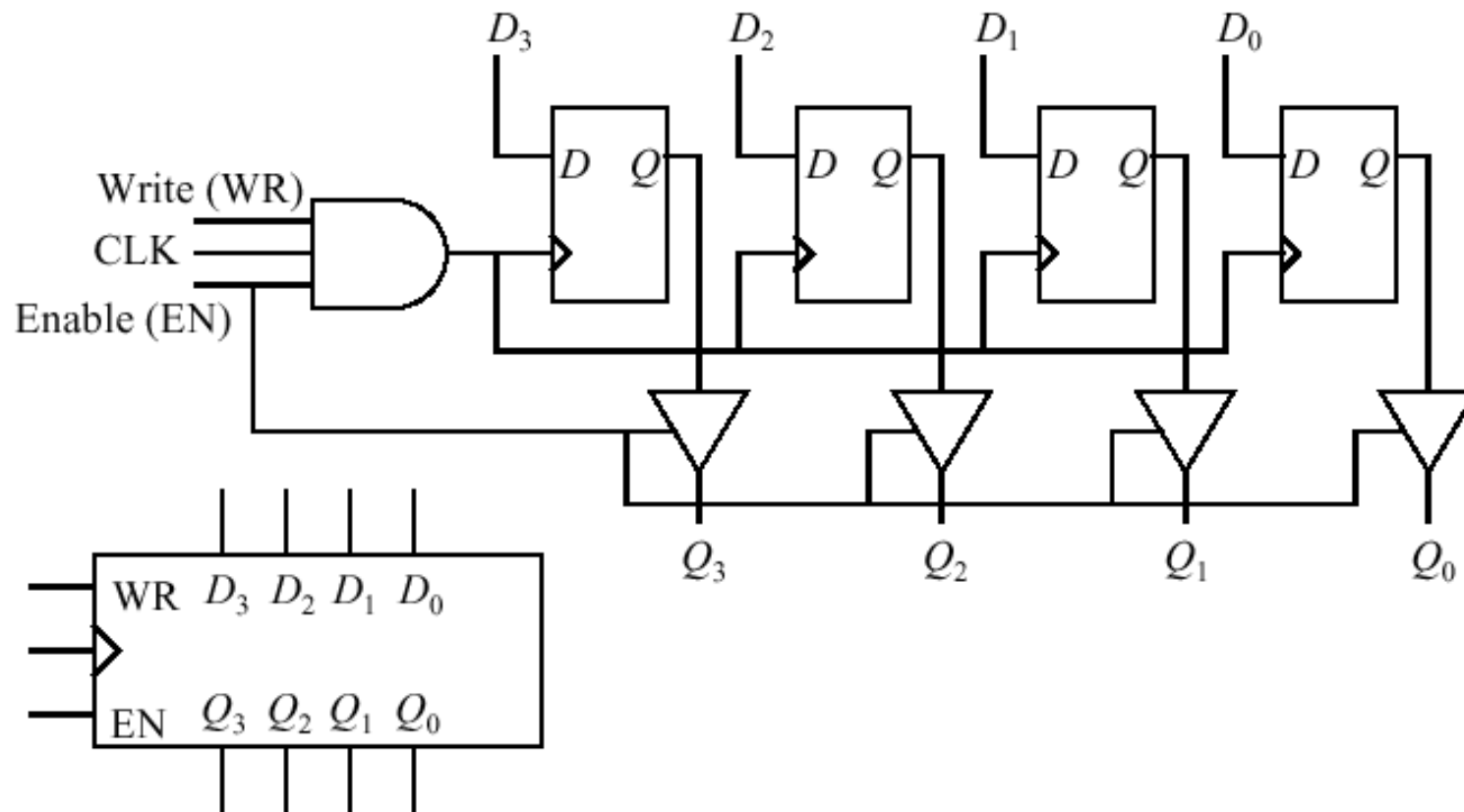


NÚMERO EM DECIMAL

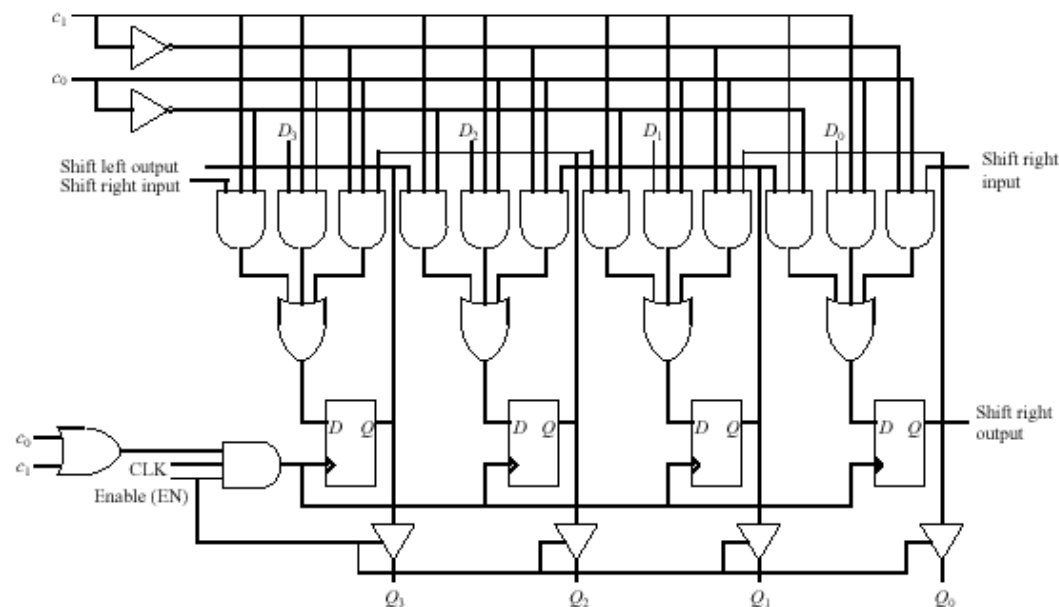


Nome	Símbolo gráfico	Tabela característica															
S-R		<table><tr><th>S</th><th>R</th><th><math>Q_{n+1}</math></th></tr><tr><td>0</td><td>0</td><td><math>Q_n</math></td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>—</td></tr></table>	S	R	$Q_{n+1}$	0	0	$Q_n$	0	1	0	1	0	1	1	1	—
S	R	$Q_{n+1}$															
0	0	$Q_n$															
0	1	0															
1	0	1															
1	1	—															
J-K		<table><tr><th>J</th><th>K</th><th><math>Q_{n+1}</math></th></tr><tr><td>0</td><td>0</td><td><math>Q_n</math></td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td><math>\overline{Q_n}</math></td></tr></table>	J	K	$Q_{n+1}$	0	0	$Q_n$	0	1	0	1	0	1	1	1	$\overline{Q_n}$
J	K	$Q_{n+1}$															
0	0	$Q_n$															
0	1	0															
1	0	1															
1	1	$\overline{Q_n}$															
D		<table><tr><th>D</th><th><math>Q_{n+1}</math></th></tr><tr><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td></tr></table>	D	$Q_{n+1}$	0	0	1	1									
D	$Q_{n+1}$																
0	0																
1	1																

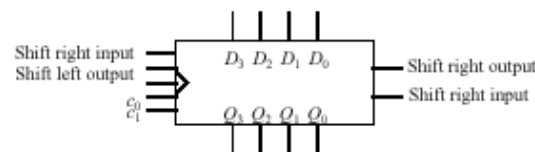
# Registrador de 4 bits



# Registrador de deslocamento com 4 bits



Control		Function
$c_1$	$c_0$	
0	0	No change
0	1	Shift left
1	0	Shift right
1	1	Parallel load



O circuito a ser analisado chama-se REGISTRADOR DE DESLOCAMENTO COM 4 BITS. Este circuito é síncrono com o *clock*, isto é, com a subida do sinal no pino de *clock* do flip-flop a

informação na entrada do *Flip-flop* ( pino D) será copiada para a saída (pino q). Repare que existem “4” possíveis de funções que podem ser executadas no circuito de acordo com entradas de controle c0 e c1:

Com  $C0 = 0$  e  $C1 = 0 \Rightarrow$  nenhuma função selecionada, nem mesmo o sinal de *clock* chegará ao pino de *clock* do *flip flop*.

Com  $C0 = 1$  e  $C1 = 1$  haverá a habilitação da carga paralela, e as demais operações são os deslocamentos para direita e esquerda.

Repare que as entradas de controle  $c0$  e  $c1$  decidirão a função a ser executada, de forma que apenas uma das portas ANDs terá sua saída diferente de zero.

