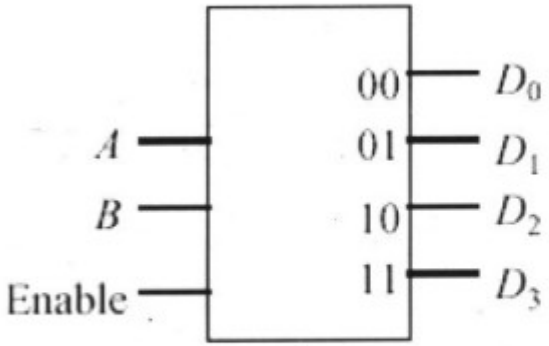
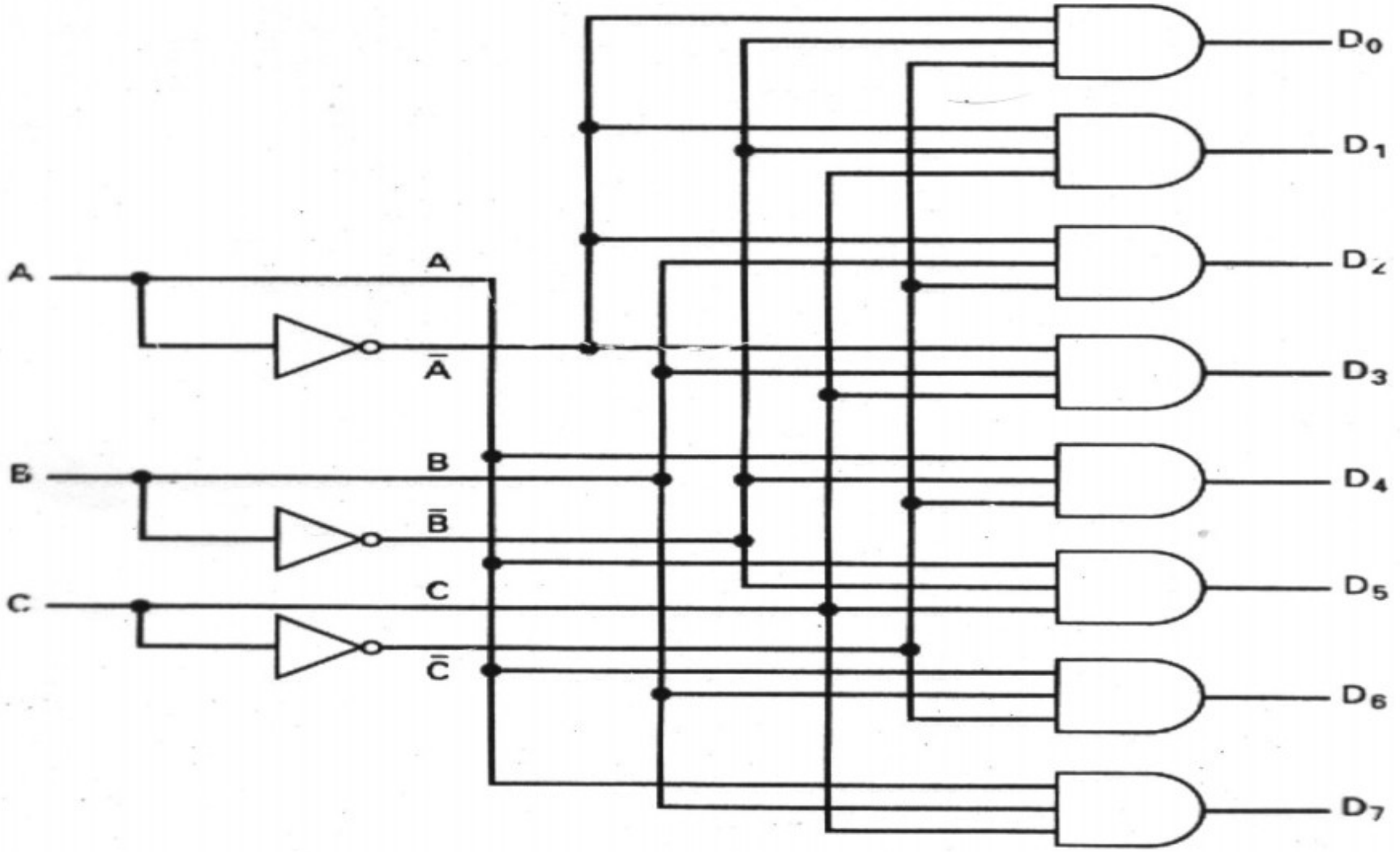
Decodificador



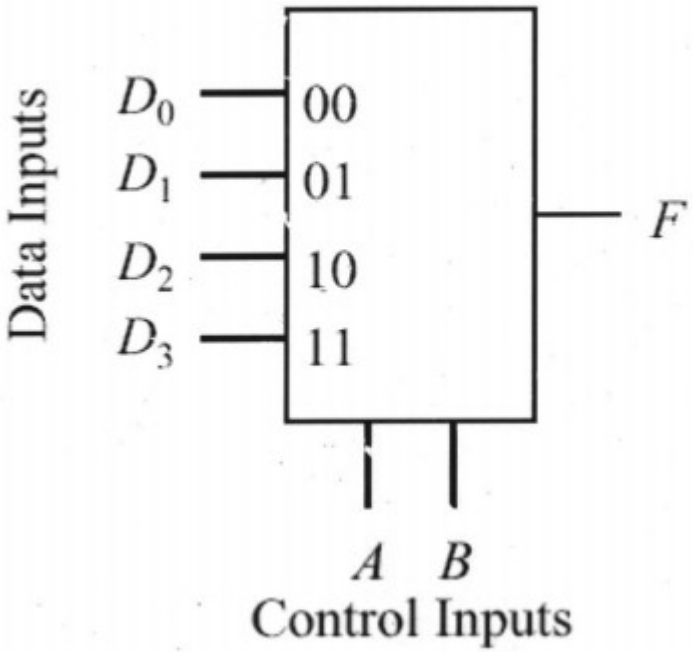
Enable = 1						
A	B	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Enable = 0						
A	B	D_0	D_1	D_2	D_3
0	0	0	0	0	0
0	1	0	0	0	0
1	0	0	0	0	0
1	1	0	0	0	0

$D_0 = \overline{A}\,\overline{B}$ $D_1 = \overline{A}\,B$ $D_2 = A\,\overline{B}$ $D_3 = A\,B$


A
B
C
A
$\bar{A}$
B
$\bar{B}$
C
$\bar{C}$
D_0
D_1
D_2
D_3
D_4
D_5
D_6
D_7

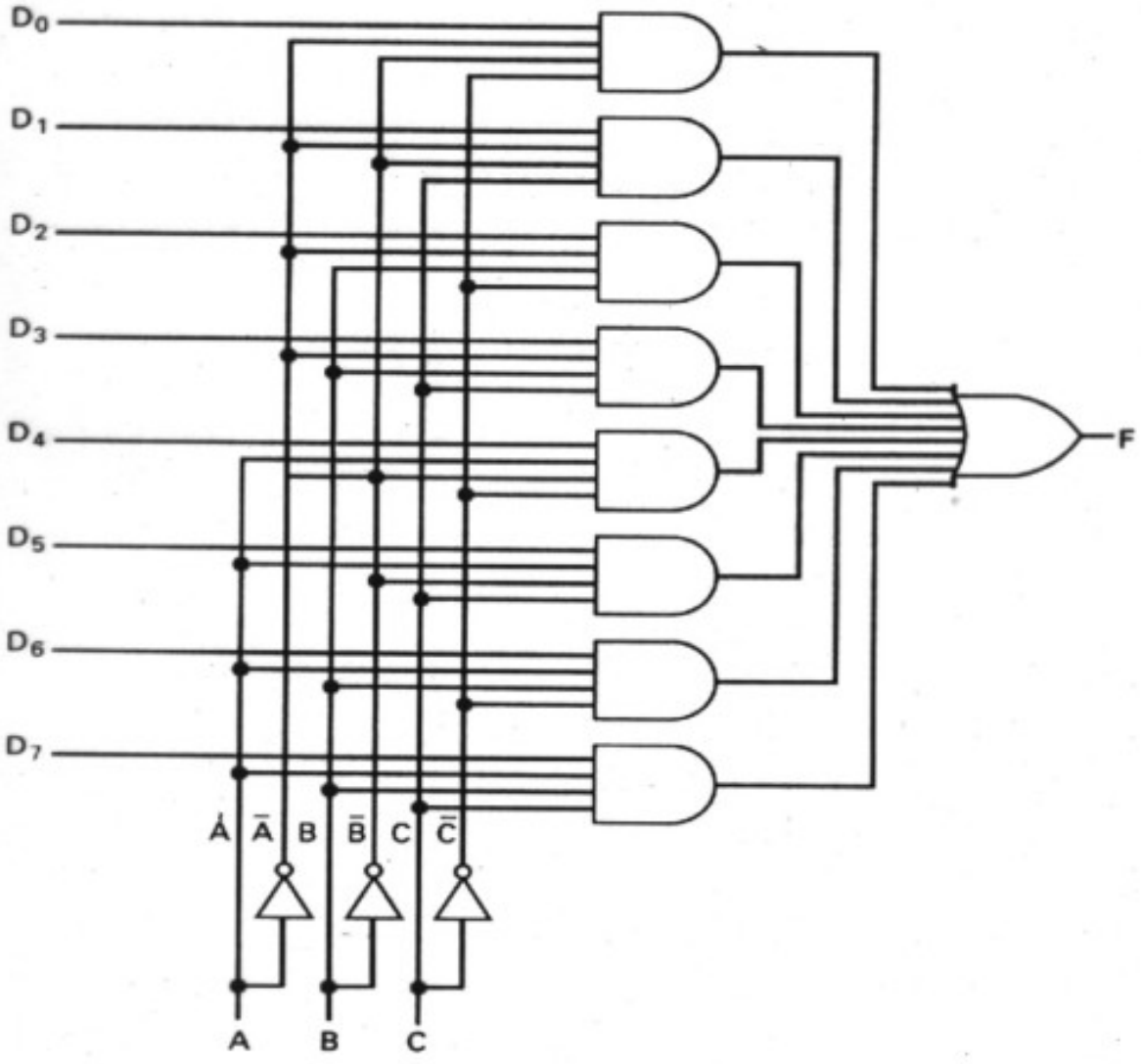
Multiplexador



A	B	F
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

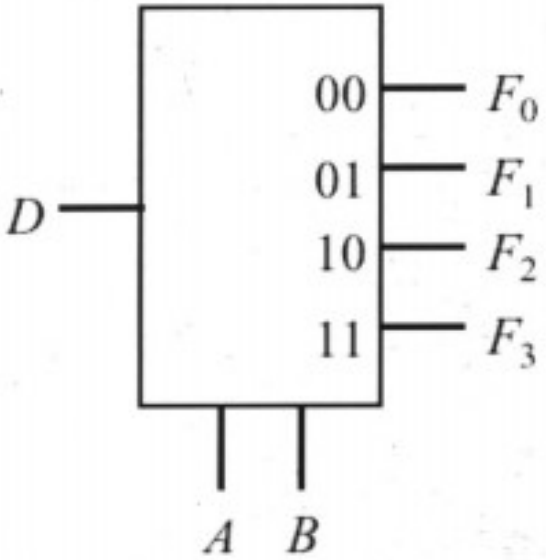
$$F = \overline{A}\,\overline{B}\,D_0 + \overline{A}\,B\,D_1 + A\,\overline{B}\,D_2 + A\,B\,D_3$$

MULTIplexador



MULTIPLEXADOR

De-multiplexador



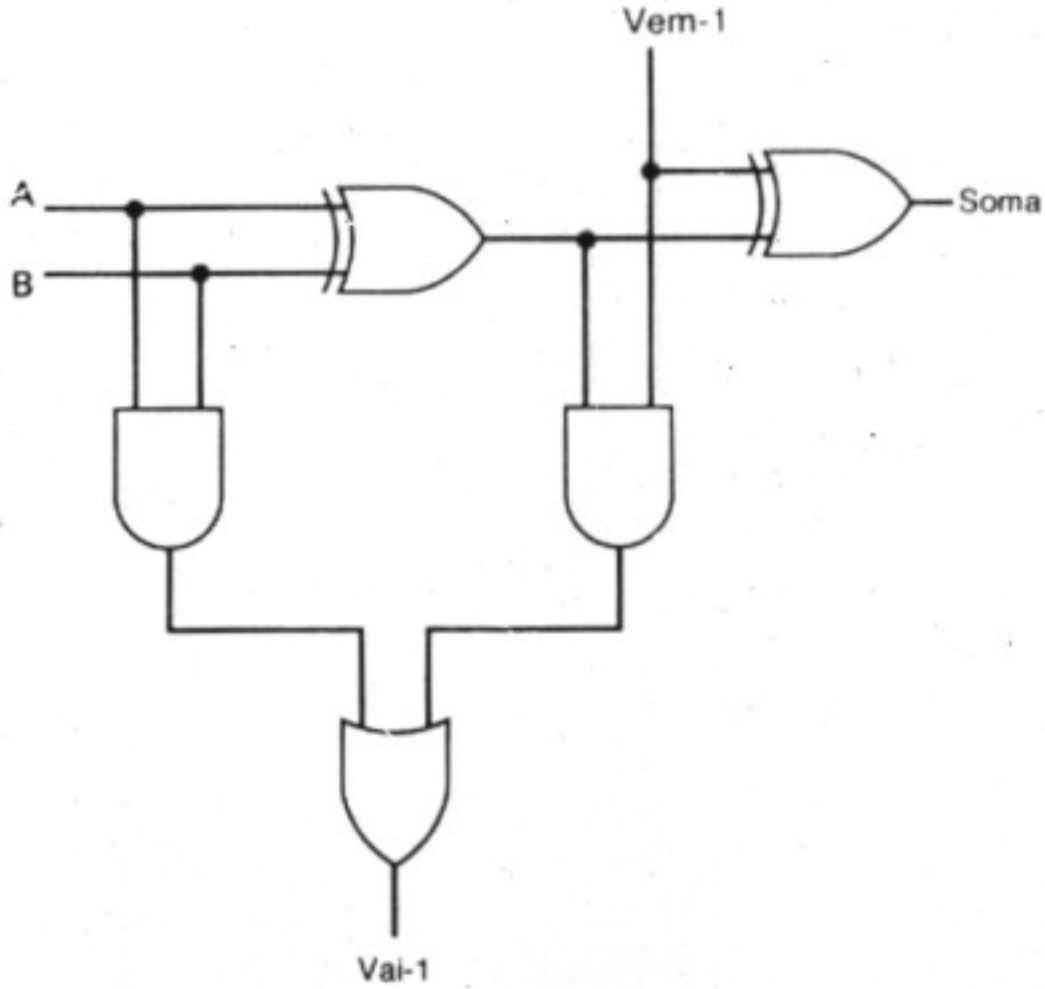
D	A	B	F_0	F_1	F_2	F_3
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	0
0	1	1	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

$F_0 = D\overline{A}\,\overline{B}$ $\quad F_2 = DA\overline{B}$

$F_1 = D\overline{A}B$ $\quad F_3 = DAB$

A	B	Vem-1	Soma	Vai-1
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

(a)



(b)

Fig. 3.19 (a) A tabela verdade para o somador completo. (b) O circuito de um somador completo.

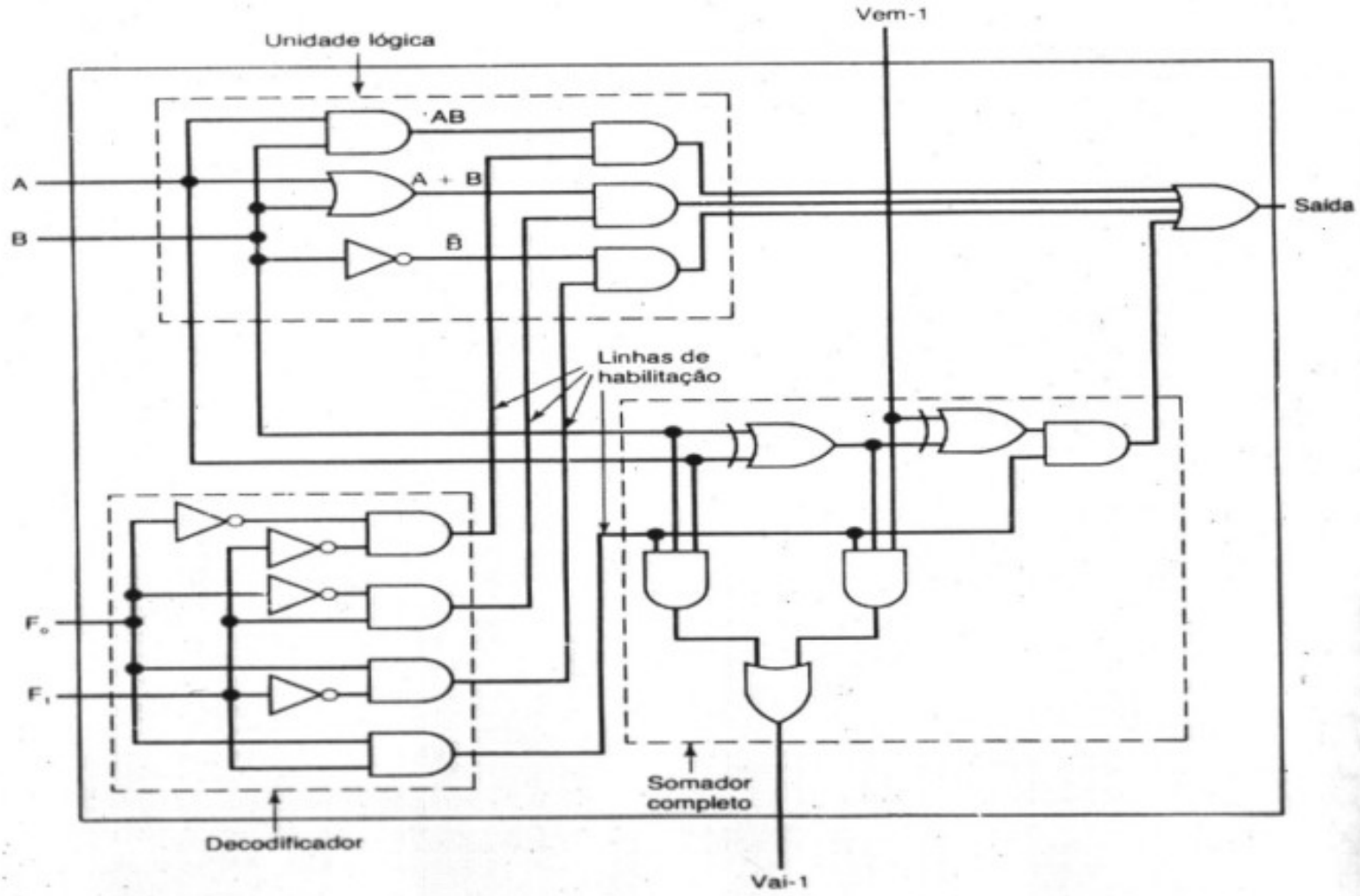


Fig. 3.20 Uma ALU de 1 bit.

Somador Completo de 4 bits com propagação de "vai-um"