# Lab 0: Install and Verify Capabilities of Tools

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# 1 Introduction

## 1.1 Class Information

Course: ECE 206
Lab section: B05
Lecture Instructor: Professor Sharad Malik

# 2 Write-Up

## 2.1 Question 1

*Suppose I have a command line open at a directory named foo. This directory contains a subdirectory named bar. What command or sequence of commands could I issue on your system to find out what files are contained within the subdirectory bar, such that after the command or sequence of commands is executed, foo is the current directory as it was before the commands were executed?*

There are two methods to do this. First, using a *sequence of commands*, it is possible to open the directory **bar** via the *cd* (change directory) command, then view its contents with the *ls* (list) command, and finally return to the parent directory **foo** with *cd*. This would be executed in VSCode as seen below:

```
PS C:\foo > cd .\bar
PS C:\foo\bar > ls
(bar's contents here)
PS C:\foo\bar > cd ..
PS C:\foo >
```

Listing 1: First Method

Alternatively, using a *command* (singular), it is possible to run the *ls* command without leaving **foo** by typing "ls," then pressing *Tab* until the desired directory (in this case **bar**) is reached. This would be executed in VSCode as seen below:

```
PS C:\foo > ls '.\bar\'
(bar's contents here)
PS C:\foo >
```

Listing 2: Second Method

## 2.2 Question 2

*Include a screenshot of the simulated circuit behavior displayed in GTKWave, showing waveforms for all inputs and outputs of circuit under test for the entire duration of the simulation. In particular, counter[3:0] and out should be displayed in the viewer. Additionally, include the waveform for the internal*

*wire d. In the screenshot, place a marker at a location such that the "Signals" pane shows the values of all the signals when the inputs were a = 0, b = 1, c = 1. Is the output of the circuit what you expect?*

After running the simulation and dragging each input and output into the signals tab, the GTKWave simulation window appears as below:

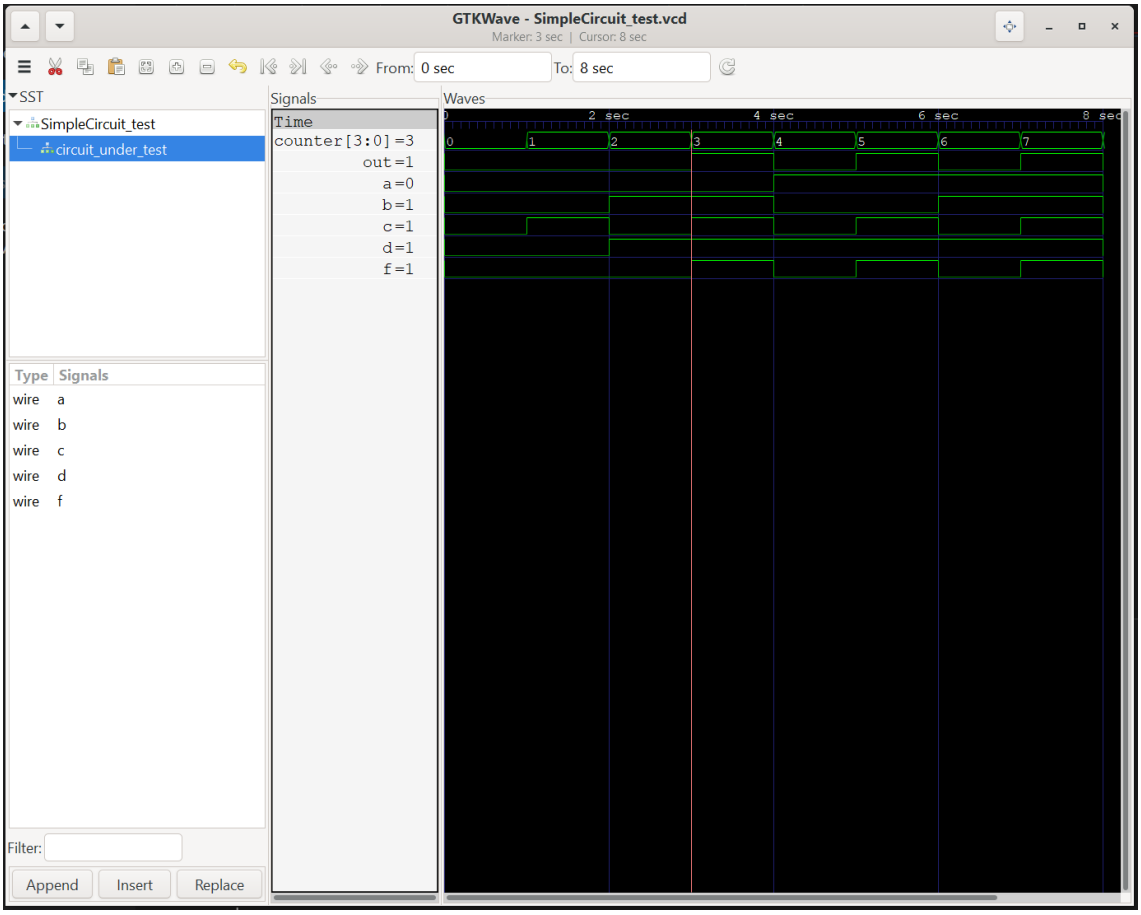


Figure 2.1: Waveforms

As visible from figure 2.1, at 3 seconds, the values in question are listed as:

- a = 0
- b = 1

- c = 1
- out = 1

This behavior is expected. Looking at the provided Verilog code:

```
1  module SimpleCircuit(
2    input a,
3    input b,
4    input c,
5    output f
6  );
7    wire d;
8
9    assign d = a || b;
10   assign f = d && c;
11 endmodule
```

Listing 3: SimpleCircuit.v

Line 9 shows that **d** is the result of an **OR** operation between **a** and **b**. Thus, when $\mathbf{a = 0}$ and $\mathbf{b = 1}$, $\mathbf{d = a\ OR\ b = 1}$.

Subsequently, line 10 shows that **f** is the result of an **AND** operation between **d** and **c**. Thus, when $\mathbf{d = 1}$ and $\mathbf{c = 1}$, $\mathbf{f = d\ AND\ C = 1}$

Since, on line 5, the **output** wire is specified as the **f** wire, it is clear that the **output** should be expected to be 1, which it is in figure 2.1.

## 2.3 Question 3

*How long did the entire simulation run in simulated time?*

As is visible from figure 2.1, near the top right of the window, the simulation ran in a **simulated time of 8 seconds**.

## 2.4 Question 4

*How much time did you spend on this lab assignment, including time spent installing software?*

In total, I spent about **3 hours** on this lab assignment.

*This paper represents my own work in accordance with University regulations.*