Control Signal	Fetch	Decode	ADD1
(rf_w_en) regfile_w_en	0	1	0
(mem_ld) mem_reg_ld	0	0	0
(PC_ld) PC_reg_ld	0	0	0
(PC_cnt) PC_reg_cnt	0	1	0
(IR_ld) IR_ld	1	0	0
(setcc) Set_cc	0	0	0
(dr_w_data) DR_addr	0	0	0
(mem_val_ld) mem_val_ld	0	0	0
(Rf1_addr_0) BaseR, R7, SR1 addr	0	0	0
(Rf2_addr_1) SR, SR2 addr	0	0	0
(instruction) instruction	instruction	0	0
(bit_in) Bit_in	0	0	b[5]
(imm5) imm5	0	0	0
(offset6) offset6	0	0	0
(PCoffset9) PCoffset9	0	0	0
(PCoffset11) PCoffset11	0	0	0
(PC_sel) PC_MUX Signal	0	0	0
(Mem_r_addr_sel) Mem_r_addr MUX Signal	0	0	0
(Mem_w_addr_sel) Mem_w_addr MUX Signal	0	0	0
(rf_w_data_sel) Regfile_w_data MUX Signal	0	0	0
(ALU_A_sel) ALU_A MUX Output Signal	0	0	0
(ALU_B_sel) ALU_B MUX Output Signal	0	0	0
(ALU_op) ALU_sel	0	0	0
(comp_sel) Comp_m0	0	0	0

ADD2	ADD3	AND1	AND2	AND3	BR1
1	1	0	1	1	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
1	1	0	1	1	0
DR	DR	0	DR	DR	0
0	0	0	0	0	0
SR1	SR1	0	SR1	SR1	0
SR2	0	0	SR2	0	0
0	0	0	0	0	0
0	0	b[5]	0	0	0
0	imm5	0	0	imm5	0
0	0	0	0	0	0
0	0	0	0	0	PCoffset9
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
SR1	SR1	0	SR1	SR1	0
SR2	imm5	0	SR2	imm5	0
ADD	ADD	0	AND	AND	0
ALU_out	ALU_out	0	ALU_out	ALU_out	0

BR2	JMP	JS	JSR	JSRR	LD
0	0	1	0	0	1
0	0	0	0	0	0
1	1	0	1	1	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	1
0	0	R7	0	0	DR
0	0	0	0	0	0
0	BaseR	0	0	BaseR	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	b[11]	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	PCoffset9
0	0	0	PCoffset11	0	0
ALU_out	BaseR	0	BaseR	ALU_out	0
0	0	0	0	0	ALU_out
0	0	0	0	0	0
0	0	PC_RF	0	0	mem_out
PC	0	0	0	PC	PC
SEXT(PCoffset9)	0	0	0	SEXT(PCoffset11)	SEXT(PCoffset9)
ADD	0	0	0	ADD	ADD
0	0	0	0	0	Mem_out

LDI1	LDI2	LDR	LEA	NOT	RET (unused)
0	1	1	1	1	0
0	0	0	0	0	0
0	0	0	0	0	1
0	0	0	0	0	0
0	0	0	0	0	0
0	1	1	1	1	0
0	DR	DR	DR	DR	0
1	0	0	0	0	0
0	0	BaseR	0	0	0
0	0	0	0	SR	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	offset6	0	0	0
PCoffset9	0	0	PCoffset9	0	0
0	0	0	0	0	0
0	0	0	0	0	R7
ALU_out	Mem_value	ALU_out	0	0	0
0	0	0	0	0	0
0	mem_out	mem_out	ALU_out	ALU_out	0
PC	0	BaseR	PC	0	0
SEXT(PCoffset9)	0	SEXT(offset6)	SEXT(PCoffset9)	SR	0
ADD	0	ADD	ADD	NOT	0
Mem_out	Mem_out	Mem_out	Mem_out	ALU_out	0

ST	STI1	STI2	STR	HALT
0	0	0	0	0
1	0	1	1	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	1	0	0	0
0	0	0	BaseR	0
SR	0	SR	SR	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	offset6	0
PCoffset9	PCoffset9	0	0	0
0	0	0	0	0
0	0	0	0	0
0	ALU_out	0	0	0
ALU_out	0	Mem_value	ALU_out	0
0	0	0	0	0
PC	PC	0	BaseR	0
SEXT(PCoffset9)	SEXT(PCoffset9)	0	SEXT(offset6)	0
ADD	ADD	0	0	0
1	0	0	1	0