



## Universal Serial Communication Interface – SPI Mode

**NOTE:** This chapter is an excerpt from the *MSP430x5xx and MSP430x6xx Family User's Guide*. The latest version of the full user's guide is available from <http://www.ti.com/lit/pdf/slau208>.

The universal serial communication interface (USCI) supports multiple serial communication modes with one hardware module. This chapter discusses the operation of the synchronous peripheral interface (SPI) mode.

Topic	Page
1.1 Universal Serial Communication Interface (USCI) Overview .....	2
1.2 USCI Introduction – SPI Mode .....	3
1.3 USCI Operation – SPI Mode .....	5
1.4 USCI_A SPI Mode Registers .....	11
1.5 USCI_B SPI Mode Registers .....	19

## 1.1 Universal Serial Communication Interface (USCI) Overview

The universal serial communication interface (USCI) modules support multiple serial communication modes. Different USCI modules support different modes. Each different USCI module is named with a different letter. For example, USCI\_A is different from USCI\_B. If more than one identical USCI module is implemented on one device, those modules are named with incrementing numbers. For example, if one device has two USCI\_A modules, they are named USCI\_A0 and USCI\_A1. See the device-specific data sheet to determine which USCI modules, if any, are implemented on which devices.

USCI\_Ax modules support:

- UART mode
- Pulse shaping for IrDA communications
- Automatic baud-rate detection for LIN communications
- SPI mode

USCI\_Bx modules support:

- I<sup>2</sup>C mode
- SPI mode

## 1.2 USCI Introduction – SPI Mode

In synchronous mode, the USCI connects the device to an external system via three or four pins: UCxSIMO, UCxSOMI, UCxCLK, and UCxSTE. SPI mode is selected when the UCSYNC bit is set, and SPI mode (3-pin or 4-pin) is selected with the UCMODEx bits.

SPI mode features include:

- 7-bit or 8-bit data length
- LSB-first or MSB-first data transmit and receive
- 3-pin and 4-pin SPI operation
- Master or slave modes
- Independent transmit and receive shift registers
- Separate transmit and receive buffer registers
- Continuous transmit and receive operation
- Selectable clock polarity and phase control
- Programmable clock frequency in master mode
- Independent interrupt capability for receive and transmit
- Slave operation in LPM4

[Figure 1-1](#) shows the USCI when configured for SPI mode.

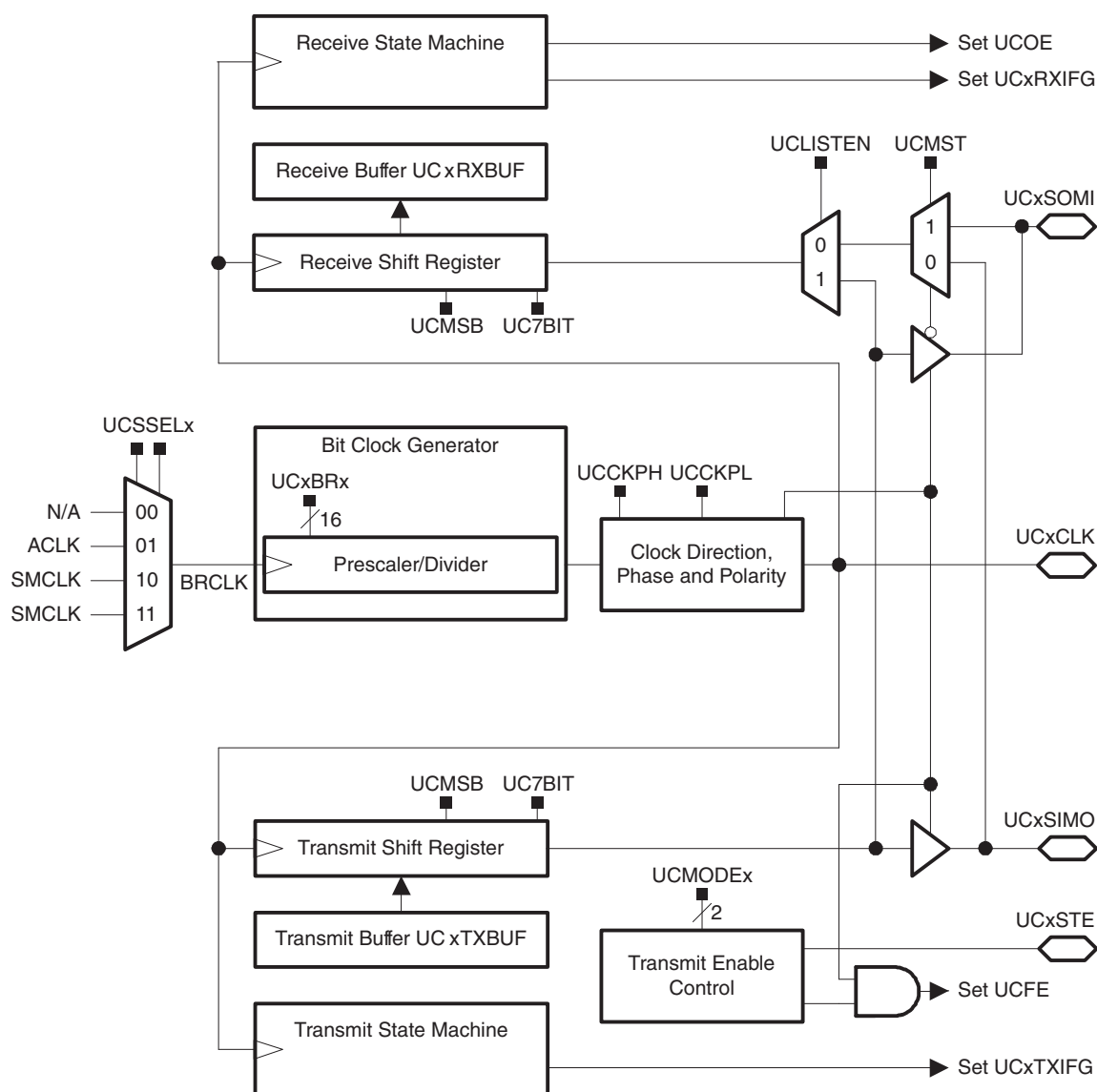


Figure 1-1. USCI Block Diagram – SPI Mode

### 1.3 USCI Operation – SPI Mode

In SPI mode, serial data is transmitted and received by multiple devices using a shared clock provided by the master. An additional pin, UCxSTE, is provided to enable a device to receive and transmit data and is controlled by the master.

Three or four signals are used for SPI data exchange:

- UCxSIMO – slave in, master out  
Master mode: UCxSIMO is the data output line.  
Slave mode: UCxSIMO is the data input line.
- UCxSOMI – slave out, master in  
Master mode: UCxSOMI is the data input line.  
Slave mode: UCxSOMI is the data output line.
- UCxCLK – USCI SPI clock  
Master mode: UCxCLK is an output.  
Slave mode: UCxCLK is an input.
- UCxSTE – slave transmit enable  
Used in 4-pin mode to allow multiple masters on a single bus. Not used in 3-pin mode.

[Table 1-1](#) describes the UCxSTE operation.

**Table 1-1. UCxSTE Operation**

UCMODEx	UCxSTE Active State	UCxSTE	Slave	Master
01	High	0	Inactive	Active
		1	Active	Inactive
10	Low	0	Active	Inactive
		1	Inactive	Active

#### 1.3.1 USCI Initialization and Reset

The USCI is reset by a PUC or by the UCSWRST bit. After a PUC, the UCSWRST bit is automatically set, keeping the USCI in a reset condition. When set, the UCSWRST bit resets the UCRXIE, UCTXIE, UCRXIFG, UCOE, and UCFE bits, and sets the UCTXIFG flag. Clearing UCSWRST releases the USCI for operation.

To avoid unpredictable behavior, configure or reconfigure the USCI module only when UCSWRST is set.

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**NOTE: Initializing or reconfiguring the USCI module**

The recommended USCI initialization/reconfiguration process is:

1. Set UCSWRST (BIS.B  
#UCSWRST, &UCxCTL1).
  2. Initialize all USCI registers with UCSWRST = 1 (including UCxCTL1).
  3. Configure ports.
  4. Clear UCSWRST via software (BIC.B  
#UCSWRST, &UCxCTL1).
  5. Enable interrupts (optional) via UCRXIE and/or UCTXIE.
- 

#### 1.3.2 Character Format

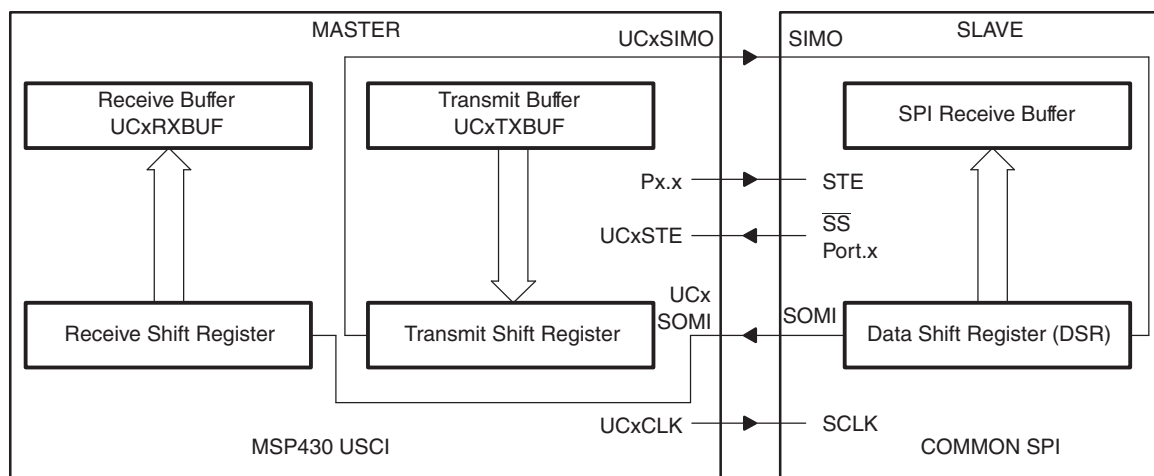
The USCI module in SPI mode supports 7-bit and 8-bit character lengths selected by the UC7BIT bit. In 7-bit data mode, UCxRXBUF is LSB justified and the MSB is always reset. The UCMSB bit controls the direction of the transfer and selects LSB or MSB first.

**NOTE: Default character format**

The default SPI character transmission is LSB first. For communication with other SPI interfaces, MSB-first mode may be required.

**NOTE: Character format for Figures**

Figures throughout this chapter use MSB-first format.

**1.3.3 Master Mode**

**Figure 1-2. USCI Master and External Slave**

Figure 1-2 shows the USCI as a master in both 3-pin and 4-pin configurations. The USCI initiates data transfer when data is moved to the transmit data buffer UCxTXBUF. The UCxTXBUF data is moved to the transmit (TX) shift register when the TX shift register is empty, initiating data transfer on UCxSIMO starting with either the MSB or LSB, depending on the UCMSB setting. Data on UCxSOMI is shifted into the receive shift register on the opposite clock edge. When the character is received, the receive data is moved from the receive (RX) shift register to the received data buffer UCxRXBUF and the receive interrupt flag UCRXIFG is set, indicating the RX/TX operation is complete.

A set transmit interrupt flag, UCTXIFG, indicates that data has moved from UCxTXBUF to the TX shift register and UCxTXBUF is ready for new data. It does not indicate RX/TX completion.

To receive data into the USCI in master mode, data must be written to UCxTXBUF, because receive and transmit operations operate concurrently.

**1.3.3.1 4-Pin SPI Master Mode**

In 4-pin master mode, UCxSTE is used to prevent conflicts with another master and controls the master as described in Table 1-1. When UCxSTE is in the master-inactive state:

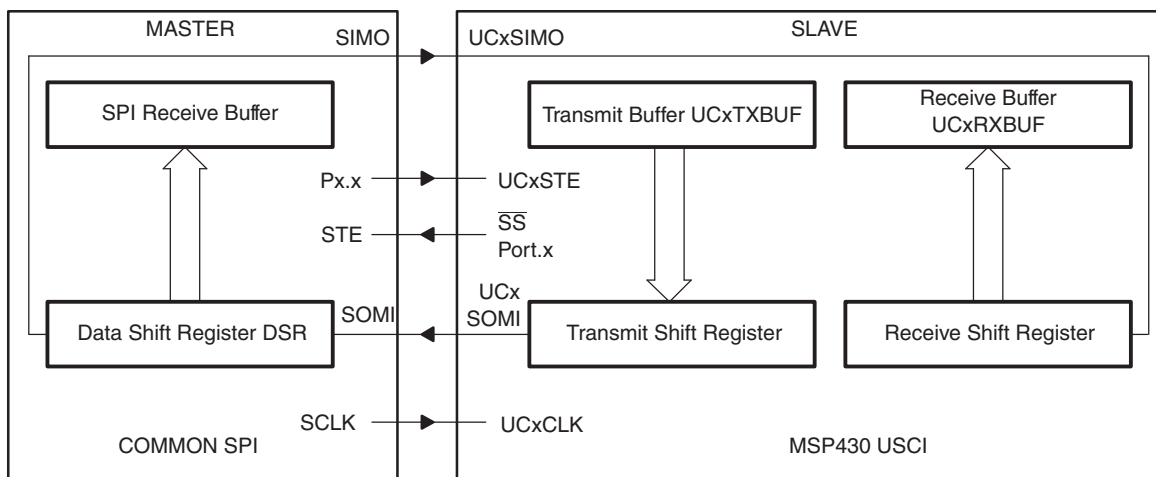
- UCxSIMO and UCxCLK are set to inputs and no longer drive the bus.
- The error bit UCFE is set, indicating a communication integrity violation to be handled by the user.
- The internal state machines are reset and the shift operation is aborted.

If data is written into UCxTXBUF while the master is held inactive by UCxSTE, it is transmit as soon as UCxSTE transitions to the master-active state. If an active transfer is aborted by UCxSTE transitioning to the master-inactive state, the data must be rewritten into UCxTXBUF to be transferred when UCxSTE transitions back to the master-active state. The UCxSTE input signal is not used in 3-pin master mode.

**NOTE: Shared UCxSTE and UCxCLK pins**

On some devices the UCxSTE functionality of an USCI\_Ax module shares the same pin with the UCxCLK functionality of the corresponding USCI\_Bx module and vice versa (UCBxSTE shared with UCxCLK). If the UCxCLK functionality is required by the corresponding module the UCxSTE functionality cannot be used by the other module. If the latter is configured in 4-pin SPI master mode, the clock signal will be interpreted as the STE signal and will corrupt its communication. To avoid this error, make sure that the latter module is configured in 3-pin SPI master mode.

### 1.3.4 Slave Mode



**Figure 1-3. USCI Slave and External Master**

Figure 1-3 shows the USCI as a slave in both 3-pin and 4-pin configurations. UCxCLK is used as the input for the SPI clock and must be supplied by the external master. The data-transfer rate is determined by this clock and not by the internal bit clock generator. Data written to UCxTXBUF and moved to the TX shift register before the start of UCxCLK is transmitted on UCxSOMI. Data on UCxSIMO is shifted into the receive shift register on the opposite edge of UCxCLK and moved to UCxRXBUF when the set number of bits are received. When data is moved from the RX shift register to UCxRXBUF, the UCRXIFG interrupt flag is set, indicating that data has been received. The overrun error bit UCOE is set when the previously received data is not read from UCxRXBUF before new data is moved to UCxRXBUF.

#### 1.3.4.1 4-Pin SPI Slave Mode

In 4-pin slave mode, UCxSTE is used by the slave to enable the transmit and receive operations and is provided by the SPI master. When UCxSTE is in the slave-active state, the slave operates normally. When UCxSTE is in the slave-inactive state:

- Any receive operation in progress on UCxSIMO is halted.
- UCxSOMI is set to the input direction.
- The shift operation is halted until the UCxSTE line transitions into the slave transmit active state.

The UCxSTE input signal is not used in 3-pin slave mode.

**NOTE: Shared UCxSTE and UCxCLK pins**

On some devices the UCxSTE functionality of an USCI\_Ax module shares the same pin with the UCBxCLK functionality of the corresponding USCI\_Bx module and vice versa (UCBxSTE shared with UCxCLK). If the UCxCLK functionality is required by the corresponding module the UCxSTE functionality cannot be used by the other module. If the latter is configured in 4-pin SPI master mode, the clock signal will be interpreted as the STE signal and will corrupt its communication. To avoid this error, make sure that the latter module is configured in 3-pin SPI master mode.

**1.3.5 SPI Enable**

When the USCI module is enabled by clearing the UCSWRST bit, it is ready to receive and transmit. In master mode, the bit clock generator is ready, but is not clocked nor producing any clocks. In slave mode, the bit clock generator is disabled and the clock is provided by the master.

A transmit or receive operation is indicated by UCBUSY = 1.

A PUC or set UCSWRST bit disables the USCI immediately and any active transfer is terminated.

**1.3.5.1 Transmit Enable**

In master mode, writing to UCxTXBUF activates the bit clock generator, and the data begins to transmit.

In slave mode, transmission begins when a master provides a clock and, in 4-pin mode, when the UCxSTE is in the slave-active state.

**1.3.5.2 Receive Enable**

The SPI receives data when a transmission is active. Receive and transmit operations operate concurrently.

**1.3.6 Serial Clock Control**

UCxCLK is provided by the master on the SPI bus. When UCMST = 1, the bit clock is provided by the USCI bit clock generator on the UCxCLK pin. The clock used to generate the bit clock is selected with the UCSSELx bits. When UCMST = 0, the USCI clock is provided on the UCxCLK pin by the master, the bit clock generator is not used, and the UCSSELx bits are don't care. The SPI receiver and transmitter operate in parallel and use the same clock source for data transfer.

The 16-bit value of UCBRx in the bit rate control registers (UCxxBR1 and UCxxBR0) is the division factor of the USCI clock source, BRCLK. The maximum bit clock that can be generated in master mode is BRCLK. Modulation is not used in SPI mode, and UCxMCTL should be cleared when using SPI mode for USCI\_A.

The UCxCLK/UCBxCLK frequency is given by:

$$f_{\text{BitClock}} = f_{\text{BRCLK}} / \text{UCBRx}$$

If UCBRx = 0,  $f_{\text{BitClock}} = f_{\text{BRCLK}}$

Even UCBRx settings result in even divisions and, thus, generate a bit clock with a 50/50 duty cycle.

Odd UCBRx settings result in odd divisions. In this case, the high phase of the bit clock is one BRCLK cycle longer than the low phase.

When UCBRx = 0, no division is applied to BRCLK, and the bit clock equals BRCLK.

**1.3.6.1 Serial Clock Polarity and Phase**

The polarity and phase of UCxCLK are independently configured via the UCCKPL and UCCKPH control bits of the USCI. Timing for each case is shown in [Figure 1-4](#).



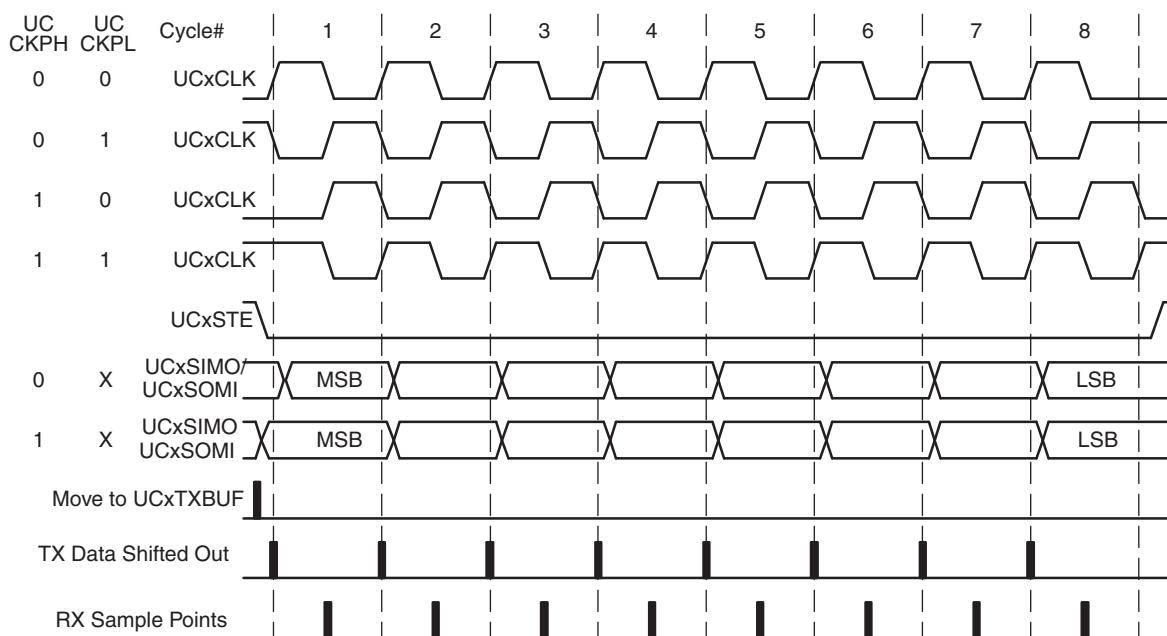


Figure 1-4. USCI SPI Timing With UCMSB = 1

### 1.3.7 Using the SPI Mode With Low-Power Modes

The USCI module provides automatic clock activation for use with low-power modes. When the USCI clock source is inactive because the device is in a low-power mode, the USCI module automatically activates it when needed, regardless of the control-bit settings for the clock source. The clock remains active until the USCI module returns to its idle condition. After the USCI module returns to the idle condition, control of the clock source reverts to the settings of its control bits.

In SPI slave mode, no internal clock source is required because the clock is provided by the external master. It is possible to operate the USCI in SPI slave mode while the device is in LPM4 and all clock sources are disabled. The receive or transmit interrupt can wake up the CPU from any low-power mode.

### 1.3.8 USCI Interrupts in SPI Mode

The USCI has only one interrupt vector that is shared for transmission and for reception. USCI\_Ax and USCI\_Bx do not share the same interrupt vector.

#### 1.3.8.1 SPI Transmit Interrupt Operation

The UCTXIFG interrupt flag is set by the transmitter to indicate that UCxTXBUF is ready to accept another character. An interrupt request is generated if UCTXIE and GIE are also set. UCTXIFG is automatically reset if a character is written to UCxTXBUF. UCTXIFG is set after a PUC or when UCSWRST = 1. UCTXIE is reset after a PUC or when UCSWRST = 1.

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**NOTE: Writing to UCxTXBUF in SPI mode**

Data written to UCxTXBUF when UCTXIFG = 0 may result in erroneous data transmission.

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#### 1.3.8.2 SPI Receive Interrupt Operation

The UCRXIFG interrupt flag is set each time a character is received and loaded into UCxRXBUF. An interrupt request is generated if UCRXIE and GIE are also set. UCRXIFG and UCRXIE are reset by a system reset PUC signal or when UCSWRST = 1. UCRXIFG is automatically reset when UCxRXBUF is read.

#### 1.3.8.3 UCxIV, Interrupt Vector Generator

The USCI interrupt flags are prioritized and combined to source a single interrupt vector. The interrupt vector register UCxIV is used to determine which flag requested an interrupt. The highest-priority enabled interrupt generates a number in the UCxIV register that can be evaluated or added to the program counter (PC) to automatically enter the appropriate software routine. Disabled interrupts do not affect the UCxIV value.

Any access, read or write, of the UCxIV register automatically resets the highest-pending interrupt flag. If another interrupt flag is set, another interrupt is immediately generated after servicing the initial interrupt.

##### 1.3.8.3.1 UCxIV Software Example

The following software example shows the recommended use of UCxIV. The UCxIV value is added to the PC to automatically jump to the appropriate routine. The following example is given for USCI\_B0.

```
USCI_SPI_ISR
    ADD    &UCB0IV, PC    ; Add offset to jump table
    RETI                                ; Vector 0: No interrupt
    JMP    RXIFG_ISR      ; Vector 2: RXIFG
TXIFG_ISR
    ...                    ; Vector 4: TXIFG
    ...                    ; Task starts here
    RETI                                ; Return
RXIFG_ISR
    ...                    ; Vector 2
    ...                    ; Task starts here
    RETI                                ; Return
```

## 1.4 USCI\_A SPI Mode Registers

The USCI\_A registers that are applicable in SPI mode are listed in [Table 1-2](#). The base addresses can be found in the device-specific data sheet. The address offsets are listed in [Table 1-2](#).

**Table 1-2. USCI\_A SPI Mode Registers**

Offset	Acronym	Register Name	Type	Access	Reset	Section
00h	UCAxCTLW0	USCI_Ax Control Word 0	Read/write	Word	0001h	
00h	UCAxCTL1	USCI_Ax Control 1	Read/write	Byte	01h	<a href="#">Section 1.4.2</a>
01h	UCAxCTL0	USCI_Ax Control 0	Read/write	Byte	00h	<a href="#">Section 1.4.1</a>
06h	UCAxBRW	USCI_Ax Bit Rate Control Word	Read/write	Word	0000h	
06h	UCAxBR0	USCI_Ax Bit Rate Control 0	Read/write	Byte	00h	<a href="#">Section 1.4.3</a>
07h	UCAxBR1	USCI_Ax Bit Rate Control 1	Read/write	Byte	00h	<a href="#">Section 1.4.4</a>
08h	UCAxMCTL	USCI_Ax Modulation Control	Read/write	Byte	00h	<a href="#">Section 1.4.5</a>
0Ah	UCAxSTAT	USCI_Ax Status	Read/write	Byte	00h	<a href="#">Section 1.4.6</a>
0Bh		Reserved - reads zero	Read	Byte	00h	
0Ch	UCAxRXBUF	USCI_Ax Receive Buffer	Read/write	Byte	00h	<a href="#">Section 1.4.7</a>
0Dh		Reserved - reads zero	Read	Byte	00h	
0Eh	UCAxTXBUF	USCI_Ax Transmit Buffer	Read/write	Byte	00h	<a href="#">Section 1.4.8</a>
0Fh		Reserved - reads zero	Read	Byte	00h	
1Ch	UCAxICTL	USCI_Ax Interrupt Control	Read/write	Word	0200h	
1Ch	UCAxIE	USCI_Ax Interrupt Enable	Read/write	Byte	00h	<a href="#">Section 1.4.9</a>
1Dh	UCAxIFG	USCI_Ax Interrupt Flag	Read/write	Byte	02h	<a href="#">Section 1.4.10</a>
1Eh	UCAxIV	USCI_Ax Interrupt Vector	Read	Word	0000h	<a href="#">Section 1.4.11</a>

### 1.4.1 UCxCTL0 Register

USCI\_Ax Control Register 0

**Figure 1-5. UCxCTL0 Register**

7	6	5	4	3	2	1	0
UCCKPH	UCCKPL	UCMSB	UC7BIT	UCMST	UCMODEx		UCSYNC
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Can be modified only when UCSWRST = 1.

**Table 1-3. UCxCTL0 Register Description**

Bit	Field	Type	Reset	Description
7	UCCKPH	RW	0h	Clock phase select 0b = Data is changed on the first UCLK edge and captured on the following edge. 1b = Data is captured on the first UCLK edge and changed on the following edge.
6	UCCKPL	RW	0h	Clock polarity select 0b = The inactive state is low. 1b = The inactive state is high.
5	UCMSB	RW	0h	MSB first select. Controls the direction of the receive and transmit shift register. 0b = LSB first 1b = MSB first
4	UC7BIT	RW	0h	Character length. Selects 7-bit or 8-bit character length. 0b = 8-bit data 1b = 7-bit data
3	UCMST	RW	0h	Master mode select 0b = Slave mode 1b = Master mode
2-1	UCMODEx	RW	0h	USCI mode. The UCMODEx bits select the synchronous mode when UCSYNC = 1. 00b = 3-pin SPI 01b = 4-pin SPI with UCxSTE active high: Slave enabled when UCxSTE = 1 10b = 4-pin SPI with UCxSTE active low: Slave enabled when UCxSTE = 0 11b = I <sup>2</sup> C mode
0	UCSYNC	RW	0h	Synchronous mode enable 0b = Asynchronous mode 1b = Synchronous mode

## 1.4.2 UCxCTL1 Register

USCI\_Ax Control Register 1

**Figure 1-6. UCxCTL1 Register**

7	6	5	4	3	2	1	0
UCSSELx		Reserved					UCSWRST
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-1

Can be modified only when UCSWRST = 1.

**Table 1-4. UCxCTL1 Register Description**

Bit	Field	Type	Reset	Description
7-6	UCSSELx	RW	0h	USCI clock source select. These bits select the BRCLK source clock in master mode. UCxCLK is always used in slave mode. 00b = Reserved 01b = ACLK 10b = SMCLK 11b = SMCLK
5-1	Reserved	RW	0h	Reserved. Always write as 0.
0	UCSWRST	RW	1h	Software reset enable 0b = Disabled. USCI reset released for operation. 1b = Enabled. USCI logic held in reset state.

### 1.4.3 UCABR0 Register

USCI\_Ax Bit Rate Control Register 0

**Figure 1-7. UCABR0 Register**

7	6	5	4	3	2	1	0
UCBRx							
rw	rw	rw	rw	rw	rw	rw	rw

Can be modified only when UCSWRST = 1.

**Table 1-5. UCABR0 Register Description**

Bit	Field	Type	Reset	Description
7-0	UCBRx	RW	undefined	Bit clock prescaler low byte. The 16-bit value of (UCABR0 + UCABR1 × 256) forms the prescaler value UCBRx. $f_{\text{BitClock}} = f_{\text{BRCLK}} / \text{UCBRx}$ If UCBRx = 0, $f_{\text{BitClock}} = f_{\text{BRCLK}}$

### 1.4.4 UCABR1 Register

USCI\_Ax Bit Rate Control Register 1

**Figure 1-8. UCABR1 Register**

7	6	5	4	3	2	1	0
UCBRx							
rw	rw	rw	rw	rw	rw	rw	rw

Can be modified only when UCSWRST = 1.

**Table 1-6. UCABR1 Register Description**

Bit	Field	Type	Reset	Description
7-0	UCBRx	RW	undefined	Bit clock prescaler high byte. The 16-bit value of (UCABR0 + UCABR1 × 256) forms the prescaler value UCBRx. $f_{\text{BitClock}} = f_{\text{BRCLK}} / \text{UCBRx}$ If UCBRx = 0, $f_{\text{BitClock}} = f_{\text{BRCLK}}$

### 1.4.5 UCAMCTL Register

USCI\_Ax Modulation Control Register

**Figure 1-9. UCAMCTL Register**

7	6	5	4	3	2	1	0
Reserved							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

**Table 1-7. UCAMCTL Register Description**

Bit	Field	Type	Reset	Description
7-0	Reserved	R	0h	Reserved. Always write as 0.

### 1.4.6 UCxSTAT Register

USCI\_Ax Status Register

**Figure 1-10. UCxSTAT Register**

7	6	5	4	3	2	1	0
UCLISTEN	UCFE	UCOE	Reserved				UCBUSY
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	r-0

Can be modified only when UCSWRST = 1.

**Table 1-8. UCxSTAT Register Description**

Bit	Field	Type	Reset	Description
7	UCLISTEN	RW	0h	Listen enable. The UCLISTEN bit selects loopback mode. 0b = Disabled 1b = Enabled. The transmitter output is internally fed back to the receiver.
6	UCFE	RW	0h	Framing error flag. This bit indicates a bus conflict in 4-wire master mode. UCFE is not used in 3-wire master or any slave mode. 0b = No error 1b = Bus conflict occurred.
5	UCOE	RW	0h	Overrun error flag. This bit is set when a character is transferred into UCxRXBUF before the previous character was read. UCOE is cleared automatically when UCxRXBUF is read, and must not be cleared by software. Otherwise, it does not function correctly. 0b = No error 1b = Overrun error occurred
4-1	Reserved	R	0h	Reserved. Always reads as 0.
0	UCBUSY	R	0h	USCI busy. This bit indicates if a transmit or receive operation is in progress. 0b = USCI inactive 1b = USCI transmitting or receiving

### 1.4.7 UCxRXBUF Register

USCI\_Ax Receive Buffer Register

**Figure 1-11. UCxRXBUF Register**

7	6	5	4	3	2	1	0
UCRXBUFx							
r	r	r	r	r	r	r	r

**Table 1-9. UCxRXBUF Register Description**

Bit	Field	Type	Reset	Description
7-0	UCRXBUFx	R	undefined	The receive-data buffer is user accessible and contains the last received character from the receive shift register. Reading UCRXBUF resets the receive-error bits and UCRXIFG. In 7-bit data mode, UCRXBUF is LSB justified and the MSB is always reset.

### 1.4.8 UCxTXBUF Register

USCI\_Ax Transmit Buffer Register

**Figure 1-12. UCxTXBUF Register**

7	6	5	4	3	2	1	0
UCTXBUFx							
rw	rw	rw	rw	rw	rw	rw	rw

**Table 1-10. UCxTXBUF Register Description**

Bit	Field	Type	Reset	Description
7-0	UCTXBUFx	RW	undefined	The transmit data buffer is user accessible and holds the data waiting to be moved into the transmit shift register and transmitted. Writing to the transmit data buffer clears UCTXIFG. The MSB of UCxTXBUF is not used for 7-bit data and is reset.



### 1.4.9 UCAXIE Register

USCI\_Ax Interrupt Enable Register

**Figure 1-13. UCAXIE Register**

7	6	5	4	3	2	1	0
Reserved						UCTXIE	UCRXIE
r-0	r-0	r-0	r-0	r-0	r-0	rw-0	rw-0

**Table 1-11. UCAXIE Register Description**

Bit	Field	Type	Reset	Description
7-2	Reserved	R	0h	Reserved. Always reads as 0.
1	UCTXIE	RW	0h	Transmit interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
0	UCRXIE	RW	0h	Receive interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled

### 1.4.10 UCAXIFG Register

USCI\_Ax Interrupt Flag Register

**Figure 1-14. UCAXIFG Register**

7	6	5	4	3	2	1	0
Reserved						UCTXIFG	UCRXIFG
r-0	r-0	r-0	r-0	r-0	r-0	rw-1	rw-0

**Table 1-12. UCAXIFG Register Description**

Bit	Field	Type	Reset	Description
7-2	Reserved	R	0h	Reserved. Always reads as 0.
1	UCTXIFG	RW	1h	Transmit interrupt flag. UCTXIFG is set when UCAxTXBUF empty. 0b = No interrupt pending 1b = Interrupt pending
0	UCRXIFG	RW	0h	Receive interrupt flag. UCRXIFG is set when UCAxRXBUF has received a complete character. 0b = No interrupt pending 1b = Interrupt pending

### 1.4.11 UCAXIV Register

USCI\_Ax Interrupt Vector Register

**Figure 1-15. UCAXIV Register**

15	14	13	12	11	10	9	8
UCIVx							
r0	r0	r0	r0	r0	r0	r0	r0
7	6	5	4	3	2	1	0
UCIVx							
r0	r0	r0	r-0	r-0	r-0	r-0	r0

**Table 1-13. UCAXIV Register Description**

Bit	Field	Type	Reset	Description
15-0	UCIVx	R	0h	USCI interrupt vector value 00h = No interrupt pending 02h = Interrupt Source: Data received; Interrupt Flag: UCRXIFG; Interrupt Priority: Highest 04h = Interrupt Source: Transmit buffer empty; Interrupt Flag: UCTXIFG; Interrupt Priority: Lowest

## 1.5 USCI\_B SPI Mode Registers

The USCI\_B registers applicable in SPI mode are listed in [Table 1-14](#). The base addresses can be found in the device-specific data sheet. The address offsets are listed in [Table 1-14](#).

**Table 1-14. USCI\_B SPI Mode Registers**

Offset	Acronym	Register Name	Type	Access	Reset	Section
00h	UCBxCTLW0	USCI_Bx Control Word 0	Read/write	Word	0101h	
00h	UCBxCTL1	USCI_Bx Control 1	Read/write	Byte	01h	<a href="#">Section 1.5.2</a>
01h	UCBxCTL0	USCI_Bx Control 0	Read/write	Byte	01h	<a href="#">Section 1.5.1</a>
06h	UCBxBRW	USCI_Bx Bit Rate Control Word	Read/write	Word	0000h	
06h	UCBxBR0	USCI_Bx Bit Rate Control 0	Read/write	Byte	00h	<a href="#">Section 1.5.3</a>
07h	UCBxBR1	USCI_Bx Bit Rate Control 1	Read/write	Byte	00h	<a href="#">Section 1.5.4</a>
08h	UCBxMCTL	USCI_Bx Modulation Control	Read/write	Byte	00h	<a href="#">Section 1.5.5</a>
0Ah	UCBxSTAT	USCI_Bx Status	Read/write	Byte	00h	<a href="#">Section 1.5.6</a>
0Bh		Reserved - reads zero	Read	Byte	00h	
0Ch	UCBxRXBUF	USCI_Bx Receive Buffer	Read/write	Byte	00h	<a href="#">Section 1.5.7</a>
0Dh		Reserved - reads zero	Read	Byte	00h	
0Eh	UCBxTXBUF	USCI_Bx Transmit Buffer	Read/write	Byte	00h	<a href="#">Section 1.5.8</a>
0Fh		Reserved - reads zero	Read	Byte	00h	
1Ch	UCBxICTL	USCI_Bx Interrupt Control	Read/write	Word	0200h	
1Ch	UCBxIE	USCI_Bx Interrupt Enable	Read/write	Byte	00h	<a href="#">Section 1.5.9</a>
1Dh	UCBxIFG	USCI_Bx Interrupt Flag	Read/write	Byte	02h	<a href="#">Section 1.5.10</a>
1Eh	UCBxIV	USCI_Bx Interrupt Vector	Read	Word	0000h	<a href="#">Section 1.5.11</a>

### 1.5.1 UCBxCTL0 Register

USCI\_Bx Control Register 0

Figure 1-16. UCBxCTL0 Register

7	6	5	4	3	2	1	0
UCCKPH	UCCKPL	UCMSB	UC7BIT	UCMST	UCMODEx		UCSYNC
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-1

Can be modified only when UCSWRST = 1.

Table 1-15. UCBxCTL0 Register Description

Bit	Field	Type	Reset	Description
7	UCCKPH	RW	0h	Clock phase select 0b = Data is changed on the first UCLK edge and captured on the following edge. 1b = Data is captured on the first UCLK edge and changed on the following edge.
6	UCCKPL	RW	0h	Clock polarity select 0b = The inactive state is low. 1b = The inactive state is high.
5	UCMSB	RW	0h	MSB first select. Controls the direction of the receive and transmit shift register. 0b = LSB first 1b = MSB first
4	UC7BIT	RW	0h	Character length. Selects 7-bit or 8-bit character length. 0b = 8-bit data 1b = 7-bit data
3	UCMST	RW	0h	Master mode select 0b = Slave mode 1b = Master mode
2-1	UCMODEx	RW	0h	USCI mode. The UCMODEx bits select the synchronous mode when UCSYNC = 1. 00b = 3-pin SPI 01b = 4-pin SPI with UCxSTE active high: Slave enabled when UCxSTE = 1 10b = 4-pin SPI with UCxSTE active low: Slave enabled when UCxSTE = 0 11b = I <sup>2</sup> C mode
0	UCSYNC	RW	1h	Synchronous mode enable 0b = Asynchronous mode 1b = Synchronous mode

## 1.5.2 UCBxCTL1 Register

USCI\_Bx Control Register 1

**Figure 1-17. UCBxCTL1 Register**

7	6	5	4	3	2	1	0
UCSSELx		Reserved					UCSWRST
rw-0	rw-0	r0	rw-0	rw-0	rw-0	rw-0	rw-1

Can be modified only when UCSWRST = 1.

**Table 1-16. UCBxCTL1 Register Description**

Bit	Field	Type	Reset	Description
7-6	UCSSELx	RW	0h	USCI clock source select. These bits select the BRCLK source clock in master mode. UCxCLK is always used in slave mode. 00b = Reserved 01b = ACLK 10b = SMCLK 11b = SMCLK
5-1	Reserved	RW	0h	Reserved. Always write as 0.
0	UCSWRST	RW	1h	Software reset enable 0b = Disabled. USCI reset released for operation. 1b = Enabled. USCI logic held in reset state.

### 1.5.3 UCBxBR0 Register

USCI\_Bx Bit Rate Control Register 0

**Figure 1-18. UCBxBR0 Register**

7	6	5	4	3	2	1	0
UCBRx							
rw	rw	rw	rw	rw	rw	rw	rw

Can be modified only when UCSWRST = 1.

**Table 1-17. UCBxBR0 Register Description**

Bit	Field	Type	Reset	Description
7-0	UCBRx	RW	undefined	Bit clock prescaler low byte. The 16-bit value of (UCBxBR0 + UCBxBR1 × 256) forms the prescaler value UCBRx. $f_{\text{BitClock}} = f_{\text{BRCLK}} / \text{UCBRx}$ If UCBRx = 0, $f_{\text{BitClock}} = f_{\text{BRCLK}}$

### 1.5.4 UCBxBR1 Register

USCI\_Bx Bit Rate Control Register 1

**Figure 1-19. UCBxBR1 Register**

7	6	5	4	3	2	1	0
UCBRx							
rw	rw	rw	rw	rw	rw	rw	rw

Can be modified only when UCSWRST = 1.

**Table 1-18. UCBxBR1 Register Description**

Bit	Field	Type	Reset	Description
7-0	UCBRx	RW	undefined	Bit clock prescaler high byte. The 16-bit value of (UCBxBR0 + UCBxBR1 × 256) forms the prescaler value UCBRx. $f_{\text{BitClock}} = f_{\text{BRCLK}} / \text{UCBRx}$ If UCBRx = 0, $f_{\text{BitClock}} = f_{\text{BRCLK}}$

### 1.5.5 UCBxMCTL Register

USCI\_Bx Modulation Control Register

**Figure 1-20. UCBxMCTL Register**

7	6	5	4	3	2	1	0
Reserved							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

**Table 1-19. UCBxMCTL Register Description**

Bit	Field	Type	Reset	Description
7-0	Reserved	R	0h	Reserved. Always write as 0.

### 1.5.6 UCBxSTAT Register

USCI\_Bx Status Register

**Figure 1-21. UCBxSTAT Register**

7	6	5	4	3	2	1	0
UCLISTEN	UCFE	UCOE	Reserved			UCBUSY	
rw-0	rw-0	rw-0	r0	r0	r0	r0	r-0

Can be modified only when UCSWRST = 1.

**Table 1-20. UCBxSTAT Register Description**

Bit	Field	Type	Reset	Description
7	UCLISTEN	RW	0h	Listen enable. The UCLISTEN bit selects loopback mode. 0b = Disabled 1b = Enabled. The transmitter output is internally fed back to the receiver.
6	UCFE	RW	0h	Framing error flag. This bit indicates a bus conflict in 4-wire master mode. UCFE is not used in 3-wire master or any slave mode. 0b = No error 1b = Bus conflict occurred.
5	UCOE	RW	0h	Overrun error flag. This bit is set when a character is transferred into UCxRXBUF before the previous character was read. UCOE is cleared automatically when UCxRXBUF is read, and must not be cleared by software. Otherwise, it does not function correctly. 0b = No error 1b = Overrun error occurred
4-1	Reserved	R	0h	Reserved. Always reads as 0.
0	UCBUSY	R	0h	USCI busy. This bit indicates if a transmit or receive operation is in progress. 0b = USCI inactive 1b = USCI transmitting or receiving

### 1.5.7 UCBxRXBUF Register

USCI\_Bx Receive Buffer Register

**Figure 1-22. UCBxRXBUF Register**

7	6	5	4	3	2	1	0
UCRXBUFx							
r	r	r	r	r	r	r	r

**Table 1-21. UCBxRXBUF Register Description**

Bit	Field	Type	Reset	Description
7-0	UCRXBUFx	R	undefined	The receive-data buffer is user accessible and contains the last received character from the receive shift register. Reading UCRXBUF resets the receive-error bits and UCRXIFG. In 7-bit data mode, UCRXBUF is LSB justified and the MSB is always reset.

### 1.5.8 UCBxTXBUF Register

USCI\_Bx Transmit Buffer Register

**Figure 1-23. UCBxTXBUF Register**

7	6	5	4	3	2	1	0
UCTXBUFx							
rw	rw	rw	rw	rw	rw	rw	rw

**Table 1-22. UCBxTXBUF Register Description**

Bit	Field	Type	Reset	Description
7-0	UCTXBUFx	RW	undefined	The transmit data buffer is user accessible and holds the data waiting to be moved into the transmit shift register and transmitted. Writing to the transmit data buffer clears UCTXIFG. The MSB of UCBxTXBUF is not used for 7-bit data and is reset.



### 1.5.9 UCBxIE Register

USCI\_Bx Interrupt Enable Register

**Figure 1-24. UCBxIE Register**

7	6	5	4	3	2	1	0
Reserved						UCTXIE	UCRXIE
r-0	r-0	r-0	r-0	r-0	r-0	rw-0	rw-0

**Table 1-23. UCBxIE Register Description**

Bit	Field	Type	Reset	Description
7-2	Reserved	R	0h	Reserved. Always reads as 0.
1	UCTXIE	RW	0h	Transmit interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
0	UCRXIE	RW	0h	Receive interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled

### 1.5.10 UCBxIFG Register

USCI\_Bx Interrupt Flag Register

**Figure 1-25. UCBxIFG Register**

7	6	5	4	3	2	1	0
Reserved						UCTXIFG	UCRXIFG
r-0	r-0	r-0	r-0	r-0	r-0	rw-1	rw-0

**Table 1-24. UCBxIFG Register Description**

Bit	Field	Type	Reset	Description
7-2	Reserved	R	0h	Reserved. Always reads as 0.
1	UCTXIFG	RW	1h	Transmit interrupt flag. UCTXIFG is set when UCBxTXBUF empty. 0b = No interrupt pending 1b = Interrupt pending
0	UCRXIFG	RW	0h	Receive interrupt flag. UCRXIFG is set when UCBxRXBUF has received a complete character. 0b = No interrupt pending 1b = Interrupt pending

### 1.5.11 UCBxIV Register

USCI\_Bx Interrupt Vector Register

**Figure 1-26. UCBxIV Register**

15	14	13	12	11	10	9	8
UCIVx							
r0	r0	r0	r0	r0	r0	r0	r0
7	6	5	4	3	2	1	0
UCIVx							
r0	r0	r0	r-0	r-0	r-0	r-0	r0

**Table 1-25. UCBxIV Register Description**

Bit	Field	Type	Reset	Description
15-0	UCIVx	R	0h	USCI interrupt vector value 00h = No interrupt pending 02h = Interrupt Source: Data received; Interrupt Flag: UCRXIFG; Interrupt Priority: Highest 04h = Interrupt Source: Transmit buffer empty; Interrupt Flag: UCTXIFG; Interrupt Priority: Lowest

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