Electrical and Computer Engineering Department

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ECE 2200L:

Experiment Number 11 & 12

MOSFET and BJT Logic Inverters

Professor Mostafa Yazdy

Fall 2024

Thursday

November 23rd, 2024

Background Information:

A JFET is a Type of FET that we work with. A JFET is a short for junction field-effect transistor.

Objective:

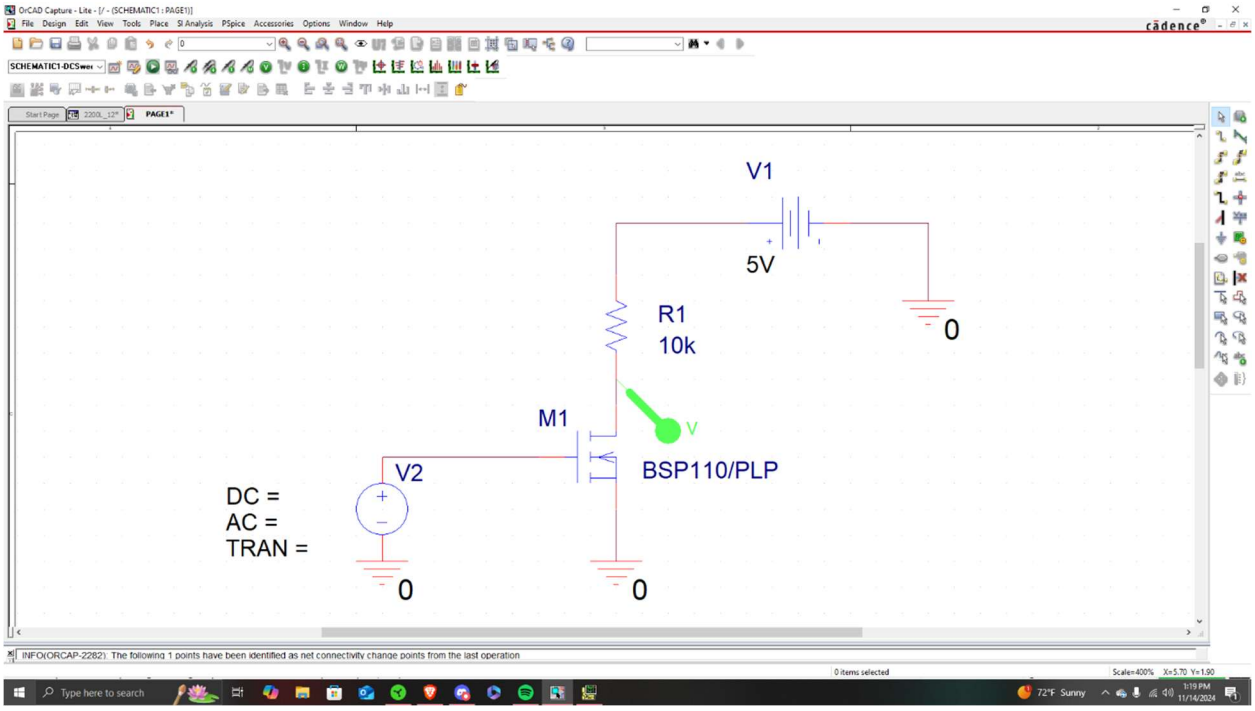
To study the transfer characteristic and output characteristics of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) through DC Sweep Simulation and Primary/Secondary Sweep Simulation. To study the applications of MOSFET and BJT devices to digital logic circuits. A MOSFET gate inverter and a BJT base inverter will be investigated. To find noise margins from VTC (Voltage Transfer Characteristic)

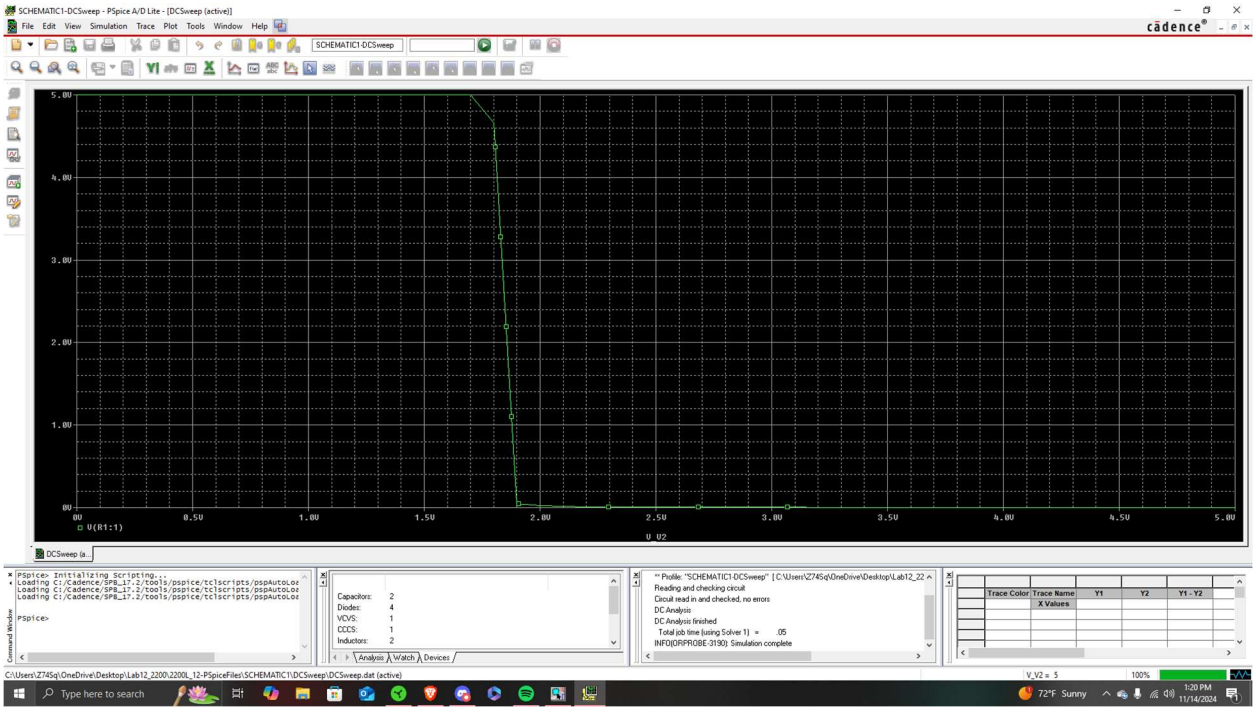
Pre-Lab:

1) Study the MOSFET sections of your textbook.

2) Capture the circuit in Figure 1 in PSPICE.

3) Using SPICE, ramp the DC input from 0 to 5V in 0.1V steps. Have SPICE plot the VOUT vs. VIN (DC sweep simulation).


V1
5V
R1
10k
0
M1
V
BSP110/PLP
V2
DC =
AC =
TRAN =
0
0
INFO(ORCAP-2282): The following 1 points have been identified as net connectivity change points from the last operation


5.0V
4.0V
3.0V
2.0V
1.0V
0V
0V
0.5V
1.0V
1.5V
2.0V
2.5V
3.0V
3.5V
4.0V
4.5V
5.0V
V(R1:1)
V_V2

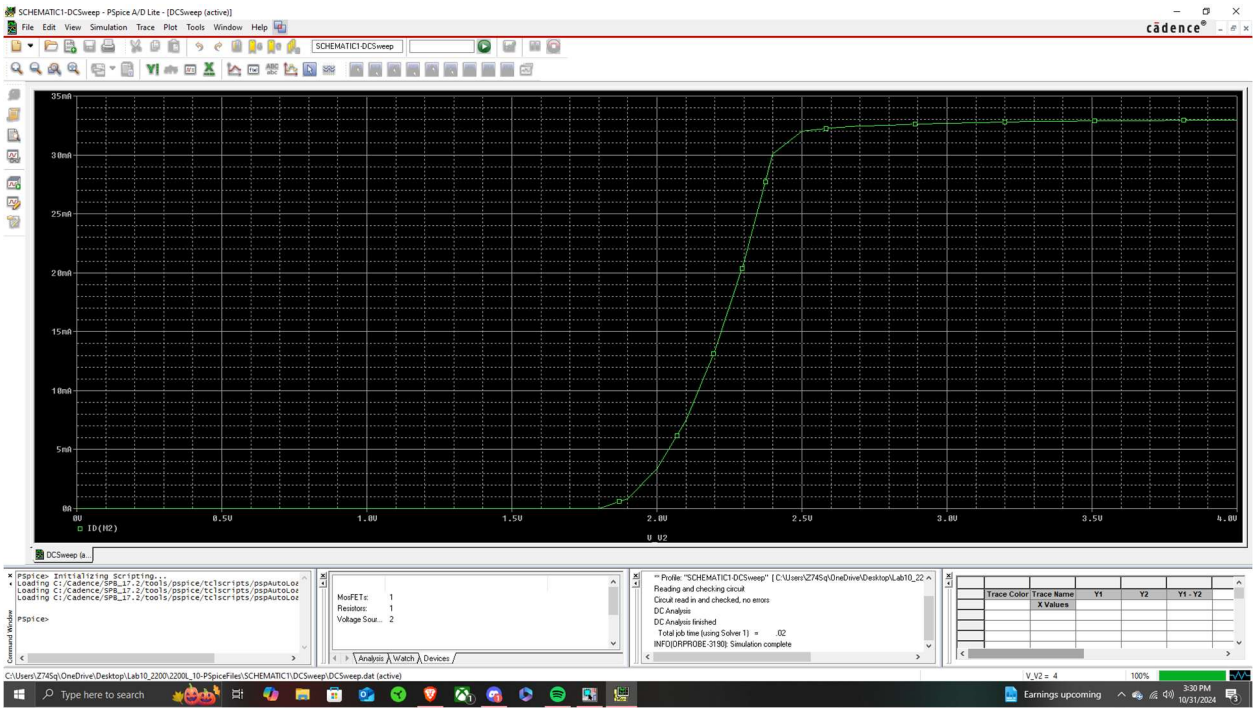
Lab Report (11):

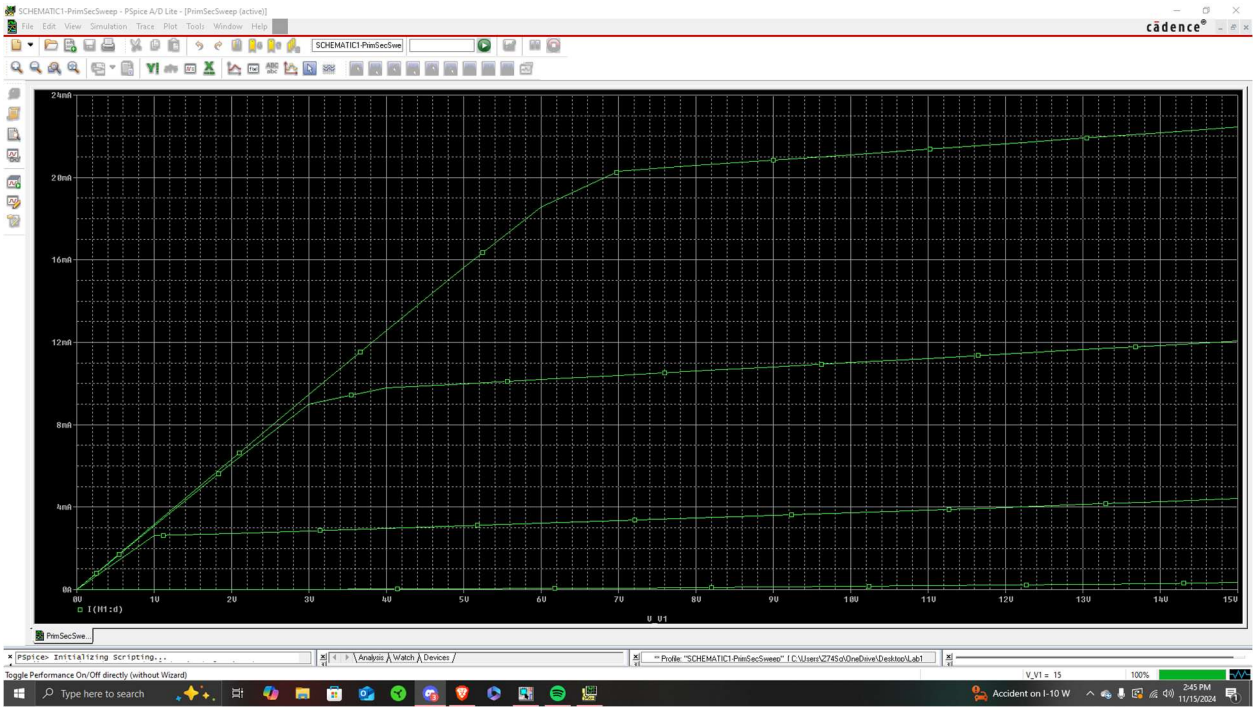
1) Find the “Transfer Characteristic” (relationship between the drain current ID and the gate source voltage VGS) for an N-Channel MOSFET.

Run simulation (DC sweep) changing Vgs from 0 to 3V or 4V with increments of 0.1V (Fig. 1). This graph is the “Transfer Characteristic” of the MOSFET. From this characteristic, determine the “Threshold Voltage” Vth.

2) Find the “Output Characteristic” using Primary/Secondary DC sweep:

A primary voltage sweep for Vdd (Fig. 2), changing from 0 to 15 V with intervals of 1V and a secondary voltage sweep for Vgs, with voltage values of: Vth, Vth + 0.2V, Vth + 0.4V, and Vth + 0.6V. Start value: Vth (which was found in part1, end value=Vth+0.6V, increments of 0.2V).


SCHEMATIC1-DCSweep - PSpice A/D Lite - [DCSweep (active)]
cadence
35mA
30mA
25mA
20mA
15mA
10mA
5mA
0A
0V
0.5V
1.0V
1.5V
2.0V
2.5V
3.0V
3.5V
4.0V
ID(M2)
V_V2
PSpice> Initializing Scripting...
PSpice>
MosFETs: 1
Resistors: 1
Voltage Sour... 2
Reading and checking circuit
Circuit read in and checked, no errors
DC Analysis
DC Analysis finished
Total job time (using Solver 1) = .02
INFO(ORPROBE-3190): Simulation complete
Trace Color
Trace Name
Y1
Y2
Y1 - Y2
X Values
V_V2 = 4
100%
Type here to search
Earnings upcoming
3:30 PM
10/31/2024


SCHEMATIC1-PrimSecSweep - PSpice A/D Lite - [PrimSecSweep (active)]
cadence
24mA
20mA
16mA
12mA
8mA
4mA
0A
0V
1V
2V
3V
4V
5V
6V
7V
8V
9V
10V
11V
12V
13V
14V
15V
I(M1:d)
V_V1
PSpice> Initializing Scripting...
Toggle Performance On/Off directly (without Wizard)
V_V1 = 15
100%
Type here to search
Accident on I-10 W
2:45 PM
11/15/2024

Lab Report (12):

1. ***Figure 1:***

Mosfet	
Vin	Vo
0	5
0.5	5
1	4.97
1.1	4.94
1.2	4.85
1.3	4.65
1.4	4.11
1.5	2.61
1.6	6.97E-02
1.7	2.14E-02
1.8	1.04E-02
1.9	6.40E-03
2	4.52E-03
2.5	1.97E-03
3	1.51E-03
3.5	1.31E-03
4	1.20E-03
4.5	1.12E-03
5	1.07E-03

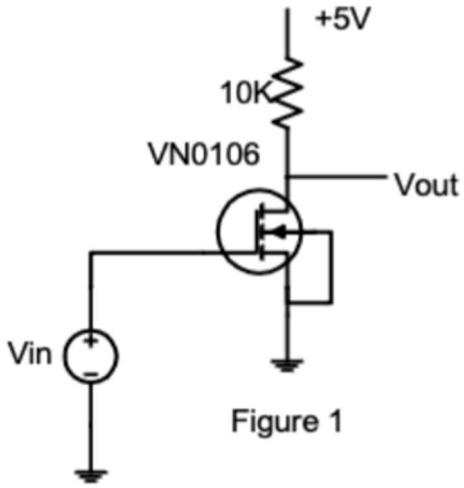
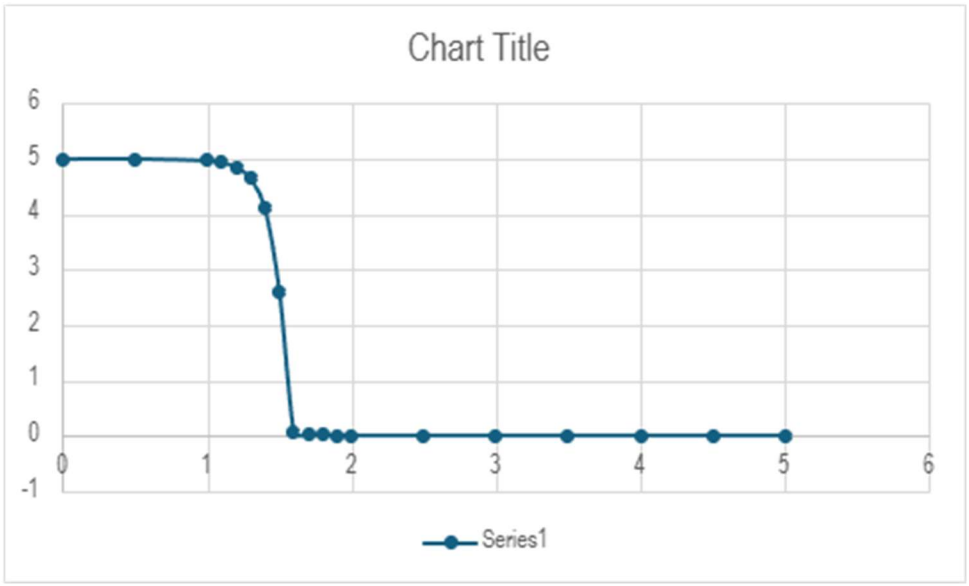


Figure 1



From graph:

- VIL = 1.5 V
- VOH = 5 V
- VIH = 1.6 V
- VOL = 0.0045 V
- $NML = VIL - VOL$ = 1.5 — 0.045 = 1.4955 V
- $NMH = VOH - VIL$ = 5 — 1.6 = 3.4 V

2. ***Figure 2:***

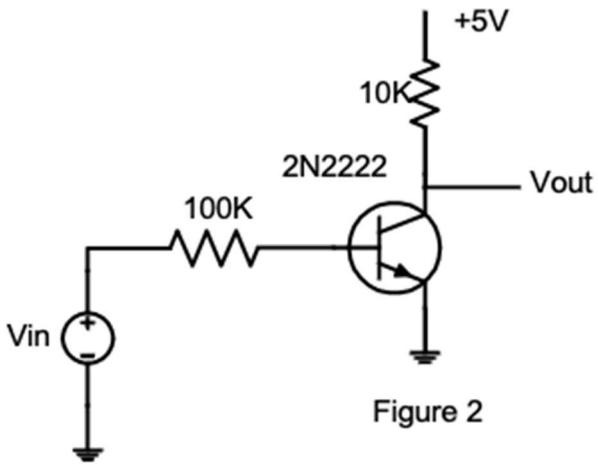
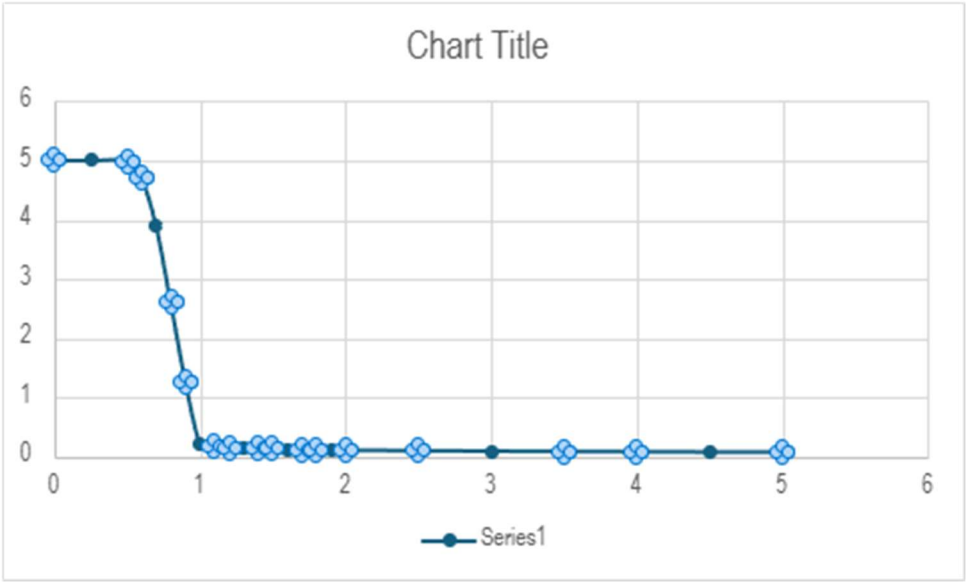


Figure 2

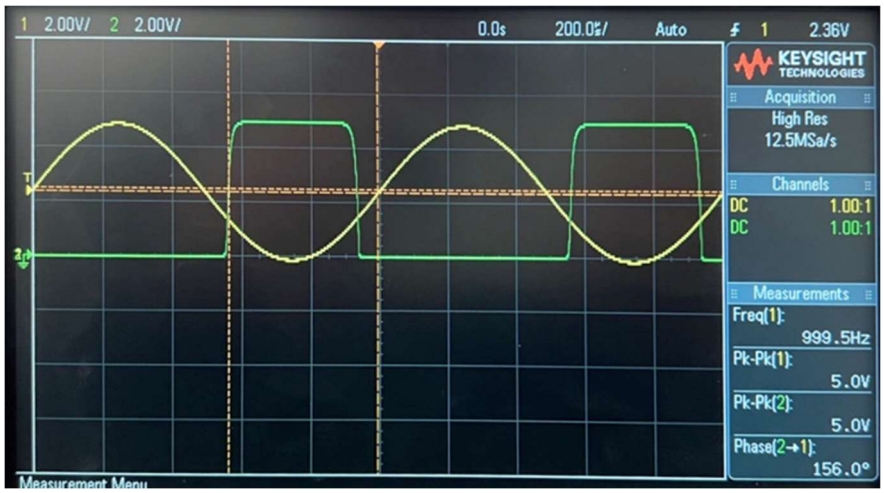
BJT	
Vin	Vo
0	5
0.25	5
0.5	4.99
0.6	4.7
0.7	3.89
0.8	2.6
0.9	1.27
1	2.18E-01
1.1	1.71E-01
1.2	1.52E-01
1.3	1.41E-01
1.4	1.33E-01
1.5	1.26E-01
1.6	1.21E-01
1.7	1.17E-01
1.8	1.13E-01
1.9	1.10E-01
2	1.07E-01
2.5	9.70E-02
3	9.00E-02
3.5	8.40E-02
4	7.90E-02
4.5	7.50E-02
5	7.20E-02



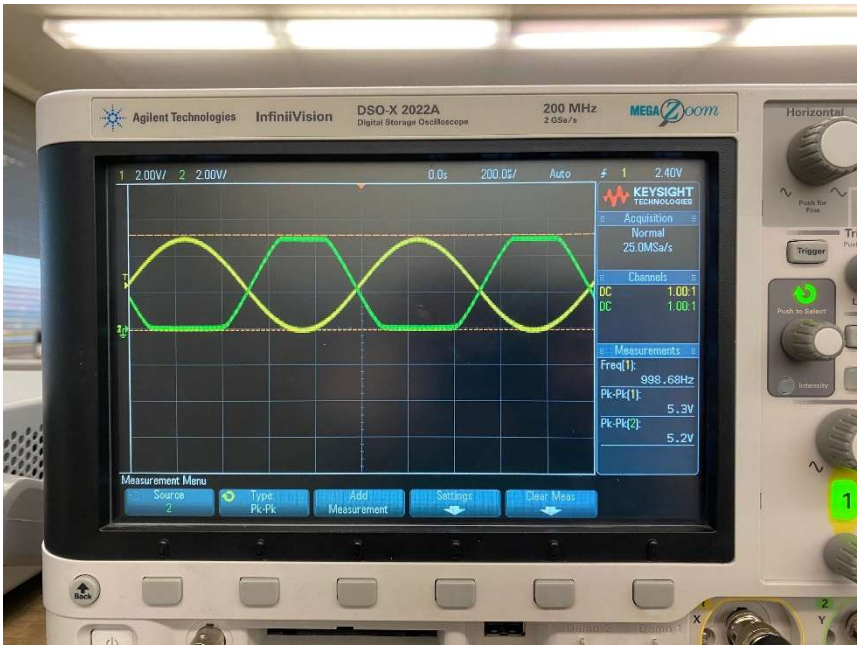
From graph:

- VIL = 0.8 V
- VOH = 5 V
- VIH = 1 V
- VOL = 0.107 V
- $NML = VIL - VO$L = 0.8 – 0.107 = 0.693 V
- $NMH = VOH - VIL$ = 5 – 1 = 4 V

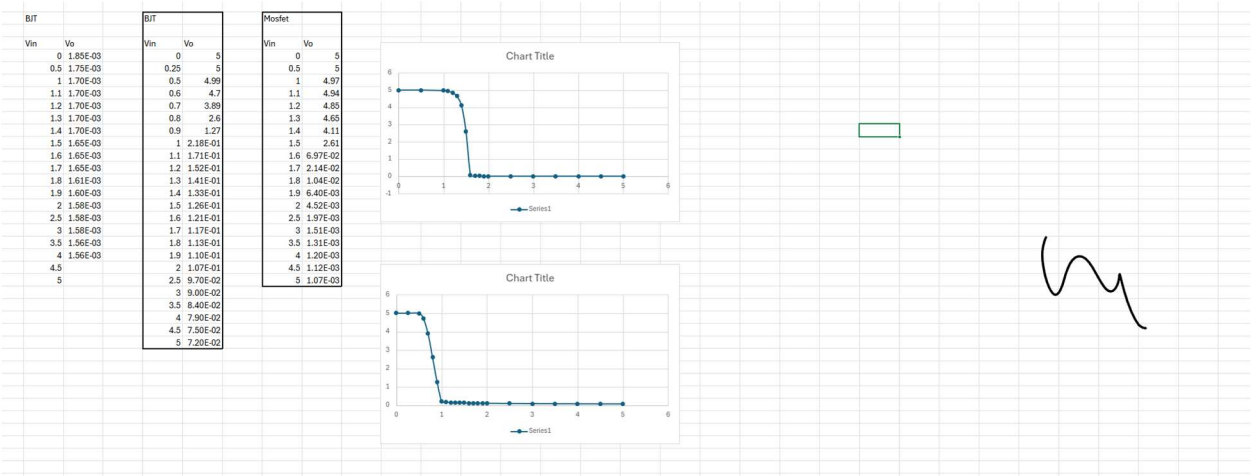
Mosftet



BJT



Proof:



BJT

Vin	Vo
0	1.85E-03
0.5	1.75E-03
1	1.70E-03
1.1	1.70E-03
1.2	1.70E-03
1.3	1.70E-03
1.4	1.70E-03
1.5	1.65E-03
1.6	1.65E-03
1.7	1.65E-03
1.8	1.61E-03
1.9	1.60E-03
2	1.58E-03
2.5	1.58E-03
3	1.58E-03
3.5	1.56E-03
4	1.56E-03
4.5	
5	

BJT

Vin	Vo
0	5
0.25	5
0.5	4.99
0.6	4.7
0.7	3.89
0.8	2.6
0.9	1.27
1	2.18E-01
1.1	1.71E-01
1.2	1.52E-01
1.3	1.41E-01
1.4	1.33E-01
1.5	1.26E-01
1.6	1.21E-01
1.7	1.17E-01
1.8	1.13E-01
1.9	1.10E-01
2	1.07E-01
2.5	9.70E-02
3	9.00E-02
3.5	8.40E-02
4	7.90E-02
4.5	7.50E-02
5	7.20E-02

Mosfet

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3.5	1.31E-03
4	1.20E-03
4.5	1.12E-03
5	1.07E-03

Conclusion:

In this experiment, we designed and constructed a circuit using both BJT and MOSFET transistors to implement inverters. Through our analysis and measurements, we observed that the MOSFET demonstrated a higher noise margin compared to the BJT. This indicates that the MOSFET is more tolerant of noise and can provide greater stability in digital logic applications. However, it also highlights that the BJT, with its lower noise margin, may offer better noise rejection characteristics under certain conditions, making it suitable for specific analog applications where precision is critical. This comparison between the two transistor types provided valuable insights into their strengths and limitations in inverter circuit design.