Electrical and Computer Engineering Department

Written by:

Group K

Brandon Contreras

Daniele Ricciardelli

ECE 2200L:

Experiment Number 8

Current-Voltage Characteristics of the Junction Field Effect

Professor Mostafa Yazdy

Fall 2024

Thursday

October 24th, 2024

Background Information:

This experiment explores the current-voltage characteristics of the Junction Field Effect Transistor (JFET). The primary objective is to analyze the relationships between terminal currents and voltages within the JFET, gaining insight into key parameters such as the saturation current (Idss) and pinch-off voltage (Vp). The experiment includes both simulation and practical measurement components. Using DC sweep simulation, the transfer characteristic is obtained by varying gate-to-source voltage (Vgs) to determine the drain current (Id) response. Additionally, a DC bias simulation of a self-biased circuit is performed to identify the operating points, including Vds and Id. These results are then cross-referenced with theoretical hand calculations to ensure accuracy. This comprehensive study provides practical experience with the JFET's behavior, bridging theoretical concepts and real-world measurements essential for understanding high-speed semiconductor devices.

Objective:

To study the relationships between the terminal currents and terminal voltages in the Junction Field Effect Transistor (JFET). A JFET is another useful 3-terminal device that has structure and characteristics very similar to Metal Semiconductor Field Effect Transistors (MESFET) used in high-speed III-V compound-based semiconductor devices.

Pre-Lab:

Read and understand the characteristic and parameters of JFET.

1) Find the Transfer Characteristic of JFET by running "DC sweep Simulation".

   Sweep the Vgs for given range to get a plot Id as a function of Vgs.

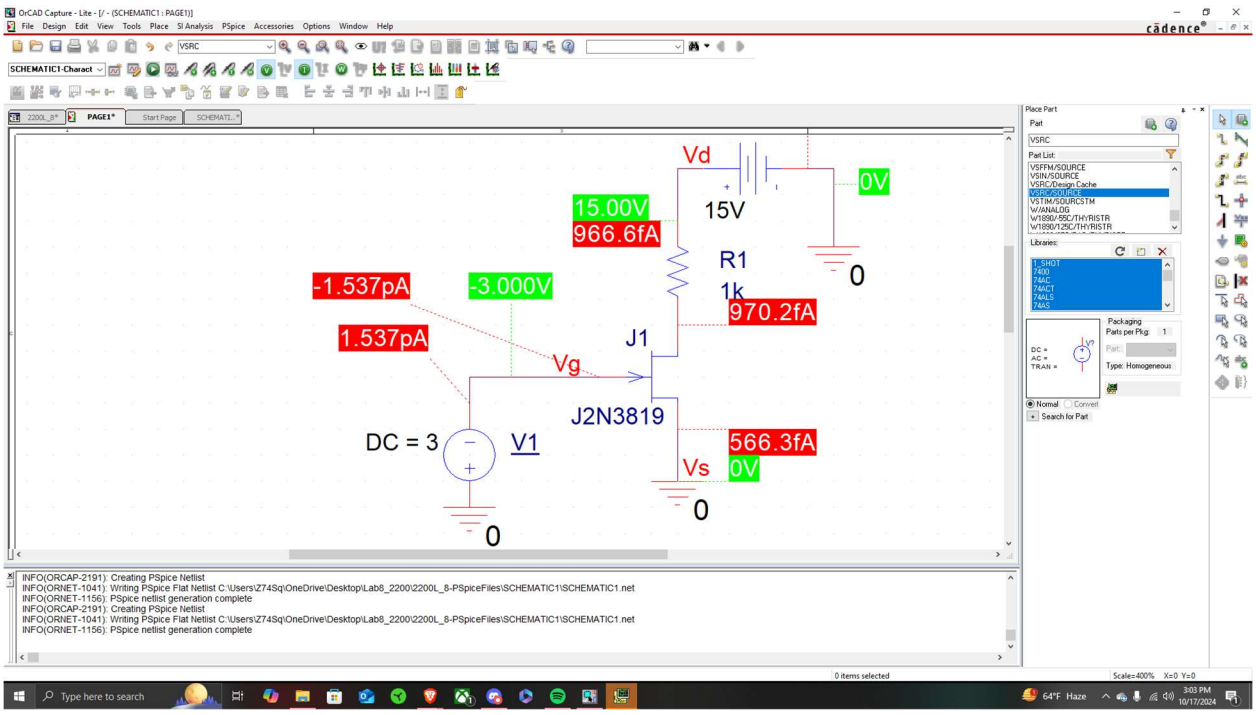
2) From the Transfer Characteristic find JFET parameters:

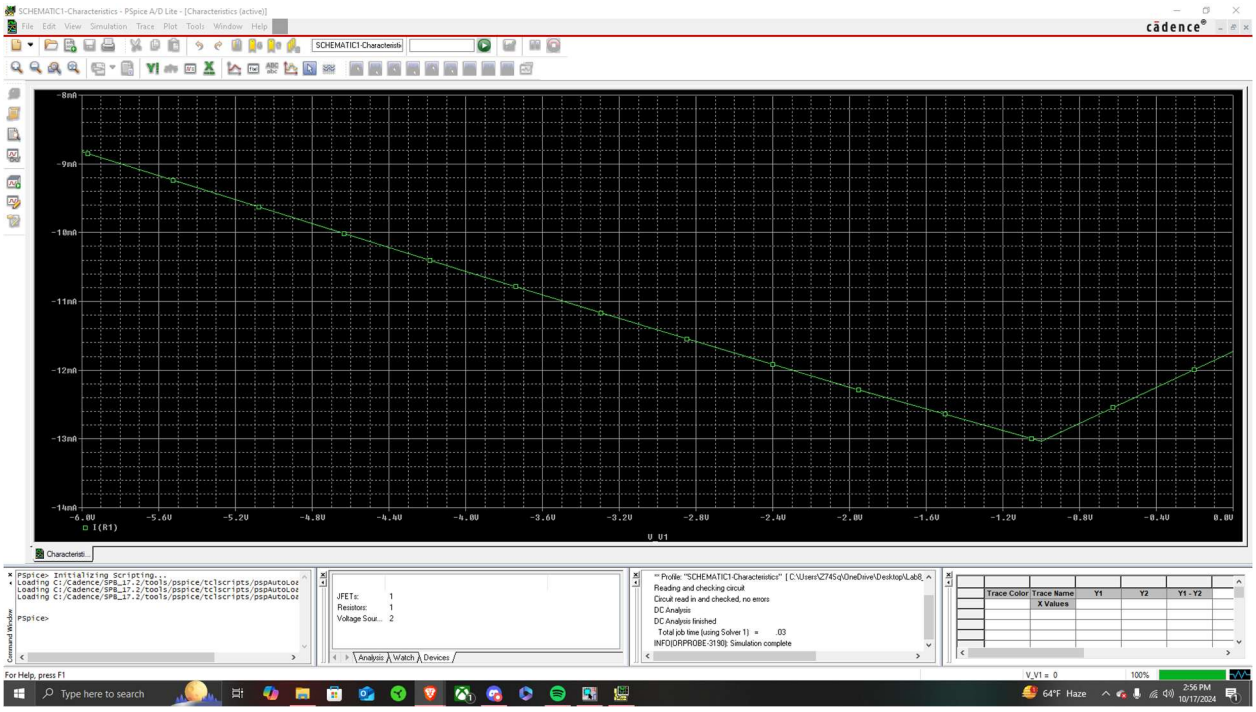
   Saturation Current (**Idss**)

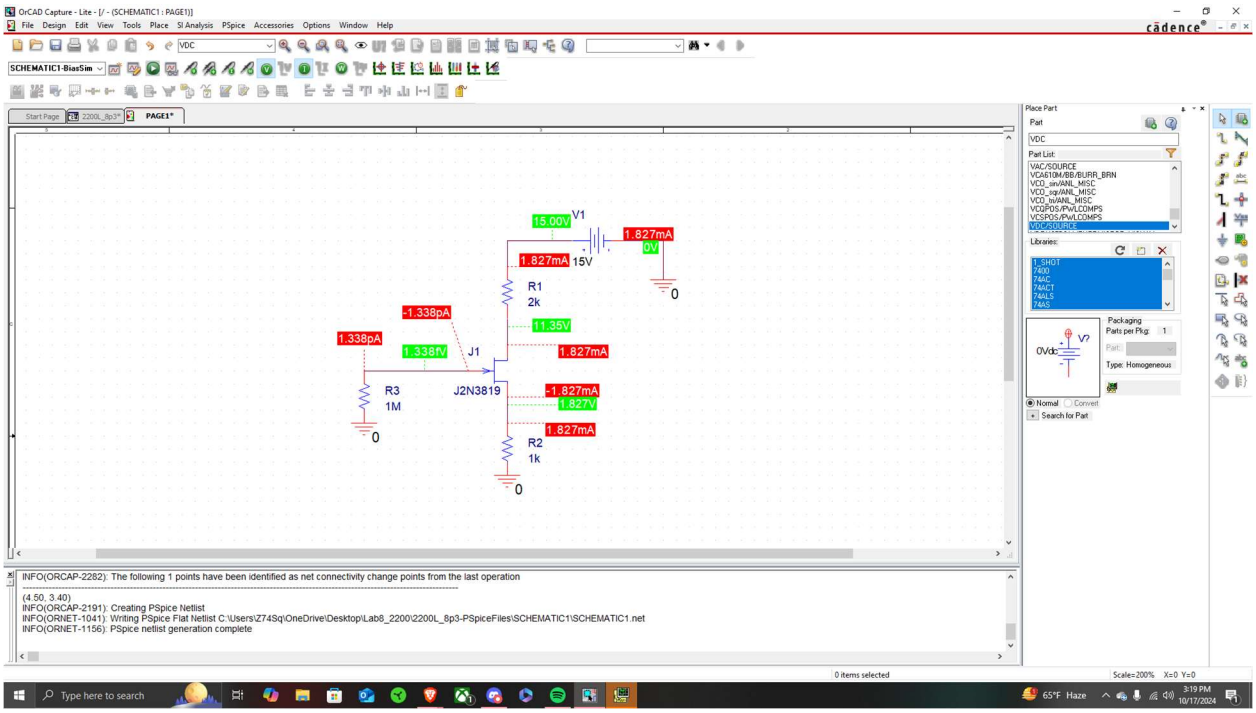
   Pinch-off voltage (**Vp**).

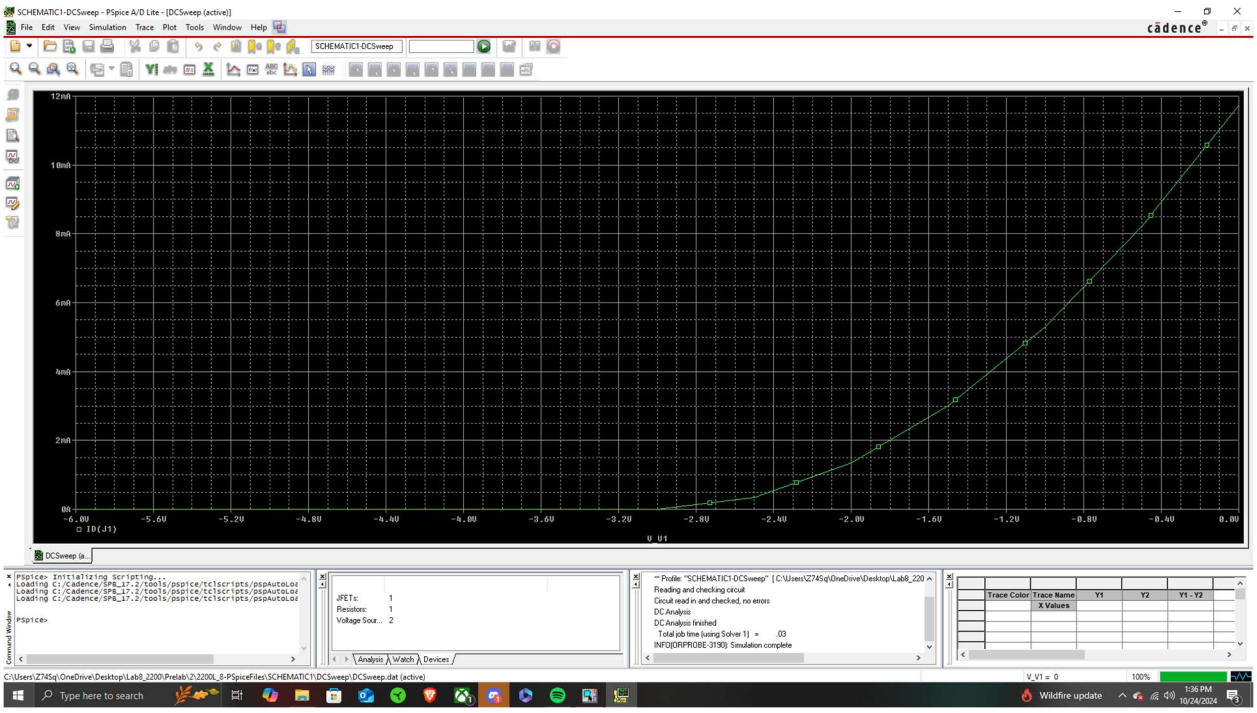
3) Run "DC Bias Simulation" for the "Self-Biased Circuit" to find Vds and Id.

4) Find Id by hand calculation as explained in lecture nodes. Using the value of Id, find Vds. Make a table and compare your simulation (part 3) and hand calculations.




SCHEMATIC1-Characteristics - PSpice A/D Lite - [Characteristics (active)]
cadence
-8mA
-9mA
-10mA
-11mA
-12mA
-13mA
-14mA
-6.0V
-5.6V
-5.2V
-4.8V
-4.4V
-4.0V
-3.6V
-3.2V
-2.8V
-2.4V
-2.0V
-1.6V
-1.2V
-0.8V
-0.4V
0.0V
I(R1)
V_V1
Characteristi...
PSpice> Initializing Scripting...
Loading C:/Cadence/SPB_17.2/tools/pspice/tclscripts/pspAutoLoa
Loading C:/Cadence/SPB_17.2/tools/pspice/tclscripts/pspAutoLoa
Loading C:/Cadence/SPB_17.2/tools/pspice/tclscripts/pspAutoLoa
PSpice>
Command Window
JFETs: 1
Resistors: 1
Voltage Sour... 2
Analysis
Watch
Devices
** Profile: "SCHEMATIC1-Characteristics" [C:\Users\Z745q\OneDrive\Desktop\Lab8_
Reading and checking circuit
Circuit read in and checked, no errors
DC Analysis
DC Analysis finished
Total job time (using Solver 1) = .03
INFO(ORPROBE-3190): Simulation complete
Trace Color
Trace Name
X Values
Y1
Y2
Y1 - Y2
For Help, press F1
V_V1 = 0
100%
Type here to search
64°F Haze
2:56 PM
10/17/2024


OrCAD Capture - Lite - [/ - (SCHEMATIC1 : PAGE1)]
File Design Edit View Tools Place SI Analysis PSpice Accessories Options Window Help
cadence
SCHEMATIC1-BiasSim
Start Page
2200L_8p3*
PAGE1*
15.00V
V1
0V
1.827mA
1.827mA
15V
R1
2k
-1.338pA
1.338pA
1.338fV
J1
J2N3819
11.35V
1.827mA
R3
1M
-1.827mA
1.827V
1.827mA
R2
1k
0
Place Part
Part
VDC
Part List:
VAC/SOURCE
VCA610M/BB/BURR_BRN
VCO_sin/ANL_MISC
VCO_sq/ANL_MISC
VCO_tri/ANL_MISC
VCQPOS/PWLCOMPS
VCSPOS/PWLCOMPS
VDC/SOURCE
Libraries:
1-SHOT
7400
74AC
74ACT
74ALS
74AS
Packaging
Parts per Pkg: 1
Part:
Type: Homogeneous
0Vdc
V?
Normal
Convert
Search for Part
INFO(ORCAP-2282): The following 1 points have been identified as net connectivity change points from the last operation
(4.50, 3.40)
INFO(ORCAP-2191): Creating PSpice Netlist
INFO(ORNET-1041): Writing PSpice Flat Netlist C:\Users\Z74Sq\OneDrive\Desktop\Lab8_2200\2200L_8p3-PSpiceFiles\SCHEMATIC1\SCHEMATIC1.net
INFO(ORNET-1156): PSpice netlist generation complete
0 items selected
Scale=200% X=0 Y=0
Type here to search
65°F Haze
3:19 PM
10/17/2024



Hand calculations/derivation

$$I_D = I_{Dss}\left(1 - \frac{R_S I_D}{V_P}\right)$$

$$V_P = V_{gs} \text{ when } I_D = 0 \rightarrow$$

$$\sqrt{\frac{I_D}{I_{Dss}}} + \frac{R_S I_D}{V_P} = 1$$

$$\rightarrow \frac{(R_S I_D)^2}{V_P} + \frac{I_D}{I_{Dss}} - 1 = 0$$

Table data

Vgs (V)	Id (mA)
-6.0	0.0
-5.5	0.1
-5.0	0.3
-4.5	0.7
-4.0	1.5
-3.5	2.5
-3.0	3.8
-2.5	5.5
-2.0	7.5
-1.5	9.2
-1.0	10.5
-0.5	11.8
0.0	12.0

List of Parts:

1. 3819 JFET (or equivalent), part number for PSpice is J2N3819.
2. Resistors; 100Ω, 1KΩ, 100KΩ

Lab Report:

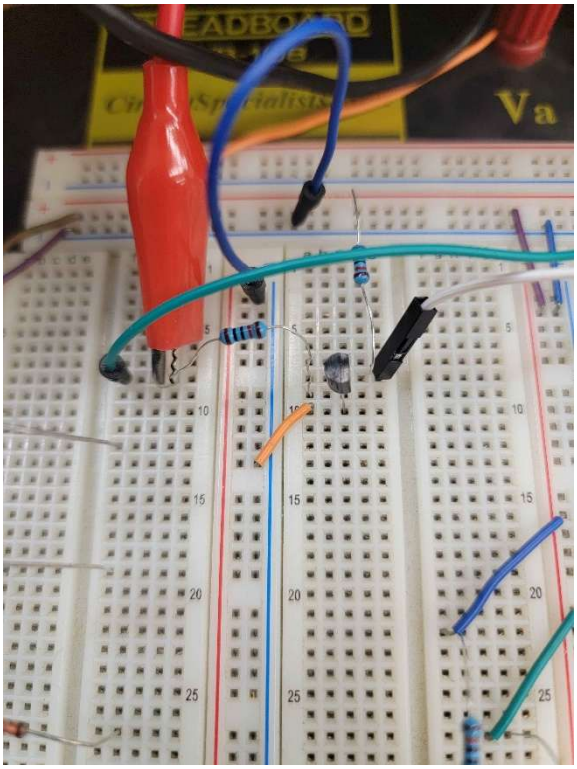
1) Find the Transfer Characteristic of JFET by changing Vgs for given values and find the Drain current (Id) for each.
   Complete a table and plot the Transfer Characteristic.

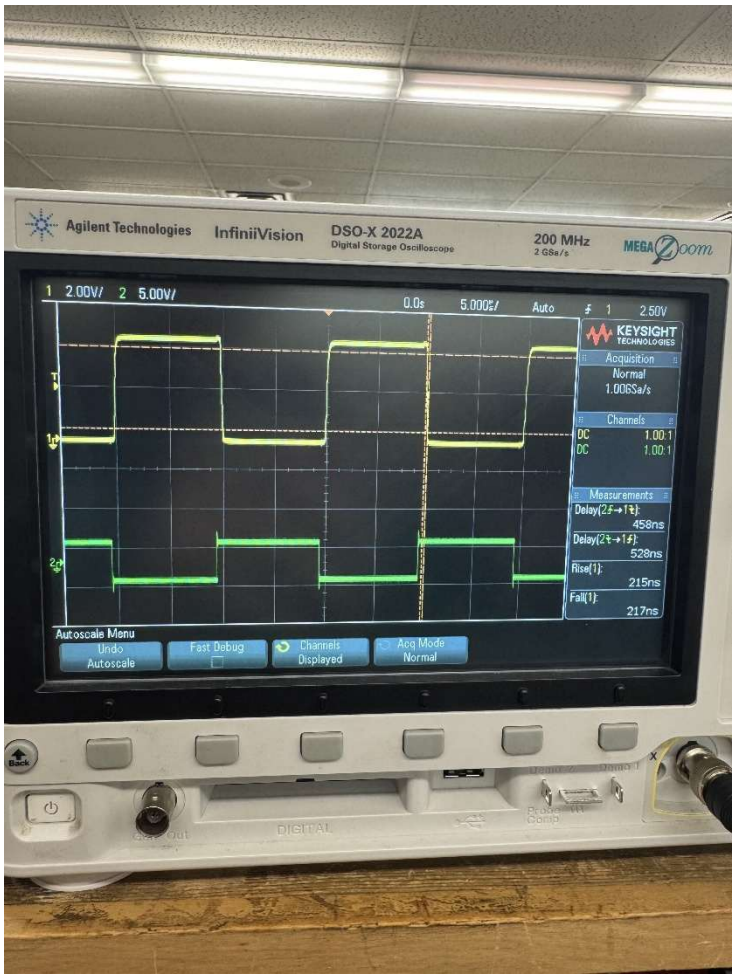
2) From the Transfer Characteristic find JFET parameters:
   Saturation Current (**Idss**)
   Pinch-off voltagr (**Vp**).

3) Construct the “self-biased circuit” and measure the operating points of the JFET (VDS, ID).

4) Use the JFET equation to find the drain current ID. Then find the JFET operating point (VDS, ID).

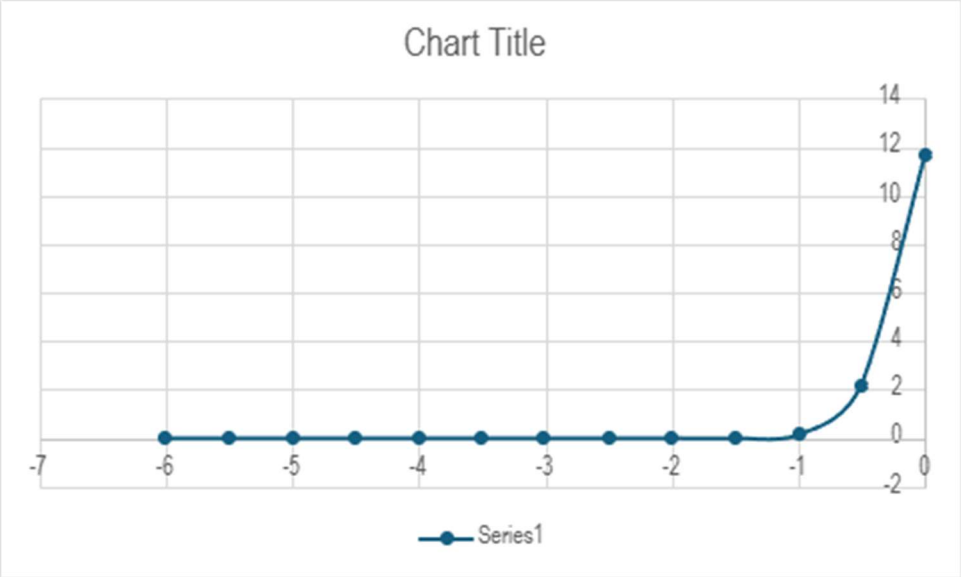
5) Compare the operating points from prelab and parts 3 and 4 of the experiment.





Procedure 1 Idss (first one)

Vgs (V)	Vrd (V)	Id (mA)
0.00	11.787	11.67376
-0.51	2.1628	2.142022
-1.00	0.140	0.138655
-1.50	0	0
-2.01	0	0
-2.50	0	0
-3.01	0	0
-3.50	0	0
-4.00	0	0
-4.50	0	0
-5.00	0	0
-5.50	0	0
-6.00	0	0



Procedure 3

Parameter	Measured	Calculated	Simulation
Vds (V)	13.087	12.12132	9.523
Id (mA)	0.637076	0.951	1.827

Procedure 5

	Parameter	Calculated	Simulation	Deviation	% Error
1	Vds (V)	12.12132	9.523	2.598320000000001	21.43594922005195
2	Id (mA)	0.951	1.827	-0.876	92.11356466876973

Conclusion:

This experiment demonstrated the current-voltage characteristics of the JFET through simulation and practical measurements. Key parameters like saturation current (Idss) and pinch-off voltage (Vp) were extracted, and the self-biased circuit provided insights into operating points (Vds, Id). While some discrepancies were observed between theoretical, simulated, and measured results, these highlighted the impact of real-world factors. Overall, the lab reinforced key concepts, linking theory with practical application essential for understanding JFET behavior.