Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Fall Term 2018

SYSTEMS PROGRAMMING AND COMPUTER ARCHITECTURE
Assignment 11: Caches & Virtual Memory

Assigned on: **5th Dec 2018**
Due by: **11th 23:59 Dec 2018**

Part I: Pen & Paper Exercises, Cache

Question 1

The physical address format is: **CT**: [13-6] **CI**: [5-2] **CO**: [1-0]

Physical address 0x2bb2.

a) Bit representation: 10 1011 1011 0010

b) Physical memory reference

Parameter	Value
Cache Offset (CO)	`0x2`
Cache Index (CI)	`0xc`
Cache Tag (CT)	`0xae`
Cache Hit? (Y/N)	No
Cache Byte returned	`-`

Physical address 0x098b.

a) Bit representation: 00 1001 1000 1011

b) Physical memory reference

Parameter	Value
Cache Offset (CO)	`0x3`
Cache Index (CI)	`0x2`
Cache Tag (CT)	`0x26`
Cache Hit? (Y/N)	Yes
Cache Byte returned	`0xa8`

Question 2

The array requires 128 * 4 = 512 bytes.

- For $B = 4$ bytes and $n = 1$: Cache $(S, E, B, m) = (256, 1, 4, 32)$

  The cache can hold 1024 bytes, i.e., twice than the size of the array. For block size 4 bytes, each access is to one int, and the first run through the array will be 100% misses (no support for spatial locality here...). The second loop will always be 100% hits. Total miss rate over both loops will be 50%.

$$\text{Miss rate} = \frac{\#\text{ misses}}{\#\text{ references}} = \frac{\#\text{ misses loop 1}+\#\text{ misses loop 2}}{\#\text{ refs loop 1}+\#\text{ refs loop 2}} = \frac{128+0}{128+128} = 0.5$$

- For $B = 16$ bytes and $n = 2$: Cache $(S, E, B, m) = (64, 1, 16, 32)$

  The cache can hold 1024 bytes, i.e., twice than the size of the array. Accessing the first array element brings along the next 3 as well, but we skip over two of them. This means the first loop will have a miss rate of 50%. So total miss rate is 25% (for both loops).

$$\text{Miss rate} = \frac{\#\text{ misses}}{\#\text{ references}} = \frac{\#\text{ misses loop 1}+\#\text{ misses loop 2}}{\#\text{ refs loop 1}+\#\text{ refs loop 2}} = \frac{32+0}{64+64} = 0.25$$

Part II: Pen & Paper Exercises, Virtual Memory

Question 3

P	# VPN bits	# VPO bits	# PPN bits	# PPO bits
$\mathbf{2^p}$	$\mathbf{n-p}$	$\mathbf{p}$	$\mathbf{m-p}$	$\mathbf{p}$
512 Bytes = $\mathbf{2^9}$	$\mathbf{30-9=21}$	$\mathbf{9}$	$\mathbf{22-9=13}$	$\mathbf{9}$
1 KB = $\mathbf{2^{10}}$	$\mathbf{30-10=20}$	$\mathbf{10}$	$\mathbf{22-10=12}$	$\mathbf{10}$
2 KB = $\mathbf{2^{11}}$	$\mathbf{30-11=19}$	$\mathbf{11}$	$\mathbf{22-11=11}$	$\mathbf{11}$

Question 4

Preparations

- Addressing: $n = 14, m = 12, p = 6$
  - VPN: $n - p = 14 - 6 = 8$
  - VPO = PPO: $p = 6$
  - PPN: $m - p = 12 - 6 = 6$
- TLB: $T = 2^t$ sets; here $4 = 2^2$ sets
  - TLB index (TLBI): t least significant bits of the VPN
  - TLB tag (TLBT): remaining bits of the VPN
- Cache: $(S, E, B, m) = (16, 1, 4, 12)$
  - Cache offset (CO): $b = 2$
  - Cache set index (CI): $s = 4$
  - Cache tag (CT): $t = m - (b + s) = 12 - (2 + 4) = 6$

a) Virtual address is 0x0268

(a) Virtual address (in binary)

13	*12*	*11*	*10*	*9*	*8*	*7*	*6*	*5*	*4*	*3*	*2*	*1*	*0*
0	0	0	0	1	0	0	1	1	0	1	0	0	0
VPN								VPO					
TLBT						TLBI							

(b) Address translation

Parameter	Value
VPN	0x9
TLB index	0x1
TLB tag	0x2
TLB hit (y/n)	Y
Page fault (y/n)	N
PPN	0x20

(c) Physical address (in binary)

CT						CI				CO	
11	*10*	*9*	*8*	*7*	*6*	*5*	*4*	*3*	*2*	*1*	*0*
1	0	0	0	0	0	1	0	1	0	0	0
PPN						PPO					

(d) Physical memory reference

Parameter	Value
Byte offset	0
Cache index	0xa
Cache tag	0x20
Cache hit (y/n)	Y
Cache byte returned	0x0d

b) Virtual address is 0x0197

(a) Virtual address (in binary)

13	*12*	*11*	*10*	*9*	*8*	*7*	*6*	*5*	*4*	*3*	*2*	*1*	*0*
0	0	0	0	0	1	1	0	0	1	0	1	1	1
VPN								VPO					
TLBT						TLBI							

(b) Address translation

Parameter	Value
VPN	0x6
TLB index	0x2
TLB tag	0x1
TLB hit (y/n)	Y
Page fault (y/n)	N
PPN	0x22

(c) Physical address (in binary)

CT						CI				CO	
11	*10*	*9*	*8*	*7*	*6*	*5*	*4*	*3*	*2*	*1*	*0*
1	0	0	0	1	0	0	1	0	1	1	1
PPN						PPO					

(d) Physical memory reference

Parameter	Value
Byte offset	3
Cache index	0x5
Cache tag	0x22
Cache hit (y/n)	N
Cache byte returned	–

c) Virtual address is 0x035e

(a) Virtual address (in binary)

13	*12*	*11*	*10*	*9*	*8*	*7*	*6*	*5*	*4*	*3*	*2*	*1*	*0*
0	0	0	0	1	1	0	1	0	1	1	1	1	0
VPN								VPO					
TLBT						TLBI							

(b) Address translation

Parameter	Value
VPN	0x0d
TLB index	0x1
TLB tag	0x3
TLB hit (y/n)	N
Page fault (y/n)	N
PPN	0x4

(c) Physical address (in binary)

CT						CI				CO	
11	*10*	*9*	*8*	*7*	*6*	*5*	*4*	*3*	*2*	*1*	*0*
0	0	0	1	0	0	0	1	1	1	1	0
PPN						PPO					

(d) Physical memory reference

Parameter	Value
Byte offset	0x2
Cache index	0x7
Cache tag	0x4
Cache hit (y/n)	N
Cache byte returned	–

d) Virtual address is 0x021a

(a) Virtual address (in binary)

13	*12*	*11*	*10*	*9*	*8*	*7*	*6*	*5*	*4*	*3*	*2*	*1*	*0*
0	0	0	0	1	0	0	0	0	1	1	0	1	0

VPN								VPO					
TLBT						TLBI							

(b) Address translation

Parameter	Value
VPN	0x8
TLB index	0x0
TLB tag	0x2
TLB hit (y/n)	N
Page fault (y/n)	Y
PPN	–