Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

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SYSTEMS PROGRAMMING AND COMPUTER ARCHITECTURE
Sample Solution 12: Cache Coherence & Page Table Programming

Part I: Pen & Paper Exercises

Question 1

a) In the table below, describe the sequence of operations that ensure cache coherence according to the MSI protocol. For each phase specify the state of the cache lines, the value of X they are holding, and the value of X in main memory.
Important: Reading from an invalid state can return anything. We therefore mark those values with the special symbol '–'.

n	State C_A	Value C_A	State C_B	Value C_B	Value M
1	S	10	I	–	10
2	S	10	S	10	10
3	M	0	I	–	10
4	S	0	S	0	0
5	I	–	M	20	0

b) Now describe the same sequence but assume the architecture uses the MESI protocol.

n	State C_A	Value C_A	State C_B	Value C_B	Value M
1	E	10	I	–	10
2	S	10	S	10	10
3	M	0	I	–	10
4	S	0	S	0	0
5	I	–	M	20	0

Question 2

a) Which cache-line will be used by the three processors?
The address $0xA0C0$ will map to index 8 in the direct mapped cache (bits[6:3]).

b) Describe MSI protocol transition for the caches of each processor in every step, after the instruction has been executed. Assume all cache-lines are marked as invalid in the beginning.