

# **Device Electrical Characterization Laboratory**

## **Work assignments**

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## **1. Abstract**

In this laboratory session, we will be applying methodologies acquired in our coursework to perform measurements on a range of device resistances, including sheet resistance and contact resistance. Subsequently, our focus will shift to an exploration of the voltage and current characteristics associated with PN junctions, MOSFETs, and other relevant components. The objective is to enhance our comprehension of the intricate properties exhibited by these devices through practical experimentation and analysis.

## **2. Lab Objectives**

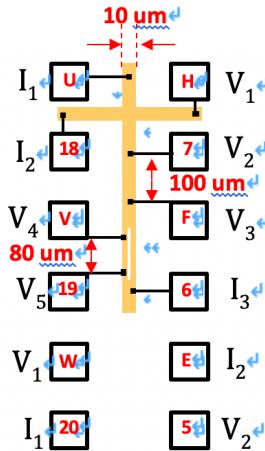
In this experimental endeavor, our focus is on characterizing specific devices. Our initial step involves the application of methods acquired in our instructional sessions to measure a spectrum of resistances exhibited by the devices, including sheet resistance and contact resistance. Subsequently, we will delve into an examination of the electrical properties inherent in PN junctions. The culminating phase of our investigation centers on the exploration of the voltage and current characteristics of MOSFETs. This comprehensive analysis aims to deepen our comprehension of the intricate properties manifested by these devices.

## **3. Results and Discussion**

### 3.1 Resistance Measurements

#### Test 1: Cross / Bridge / Split Bridge / Kelvin Resistor Measurements

A cross-bridge resistor configuration is employed to assess the sheet resistance and electrical line width of n<sup>+</sup> diffusion layers in both single crystal silicon and polysilicon. I-V curves are derived for both material types, allowing the determination of resistance through R=dV/dI. Figure 1 depicts I-V curves resulting from measurements conducted on the active-area cross-bridge resistor for an n<sup>+</sup> diffusion layer in single crystal silicon.



**Resistance test structures**

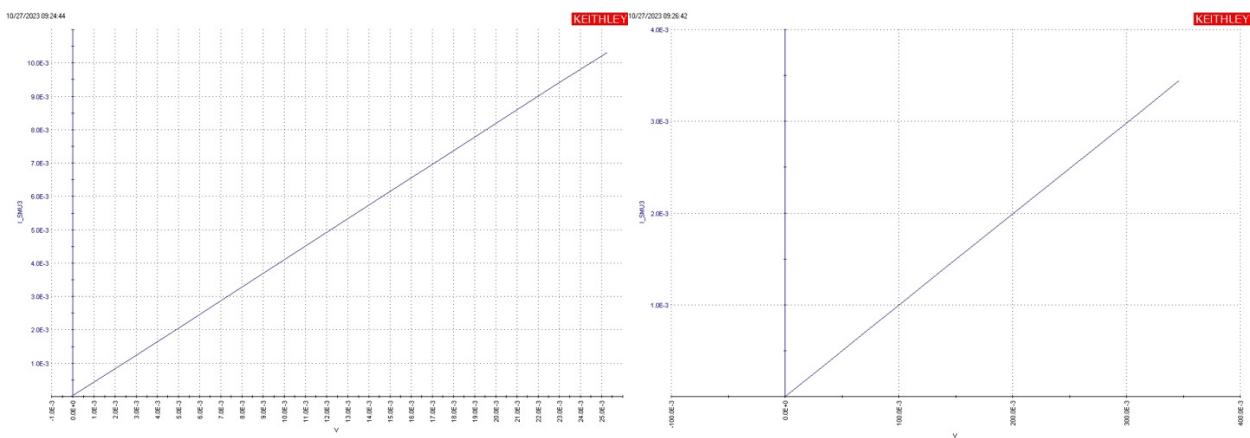
The equations for both sheet resistance and the electrical line width are showed below, respectively.

$$R_s = \frac{(V_1 - V_2) \pi}{I_{12} \ln 2} \quad R_s: \text{sheet resistance}$$

$$W_b = R_s (100 \mu m) \frac{I_{13}}{V_2 - V_3} \quad W_b: \text{electrical line width (bridge measurement)}$$

$$W_s = 2W = R_s (80 \mu m) \frac{I_{13}}{V_4 - V_5} \quad W_s: \text{electrical line width (split bridge measurement)},$$

S=electrical line space= W<sub>b</sub> - W<sub>s</sub>, Line Pitch: P= W + S



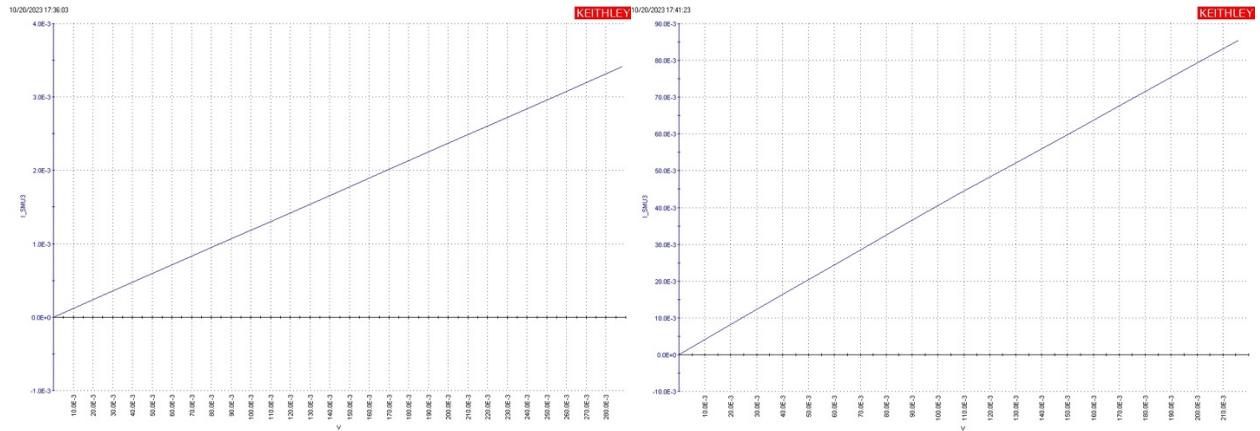


Figure 1:I-V curves obtained for n<sup>+</sup> diffusion in single crystal silicon

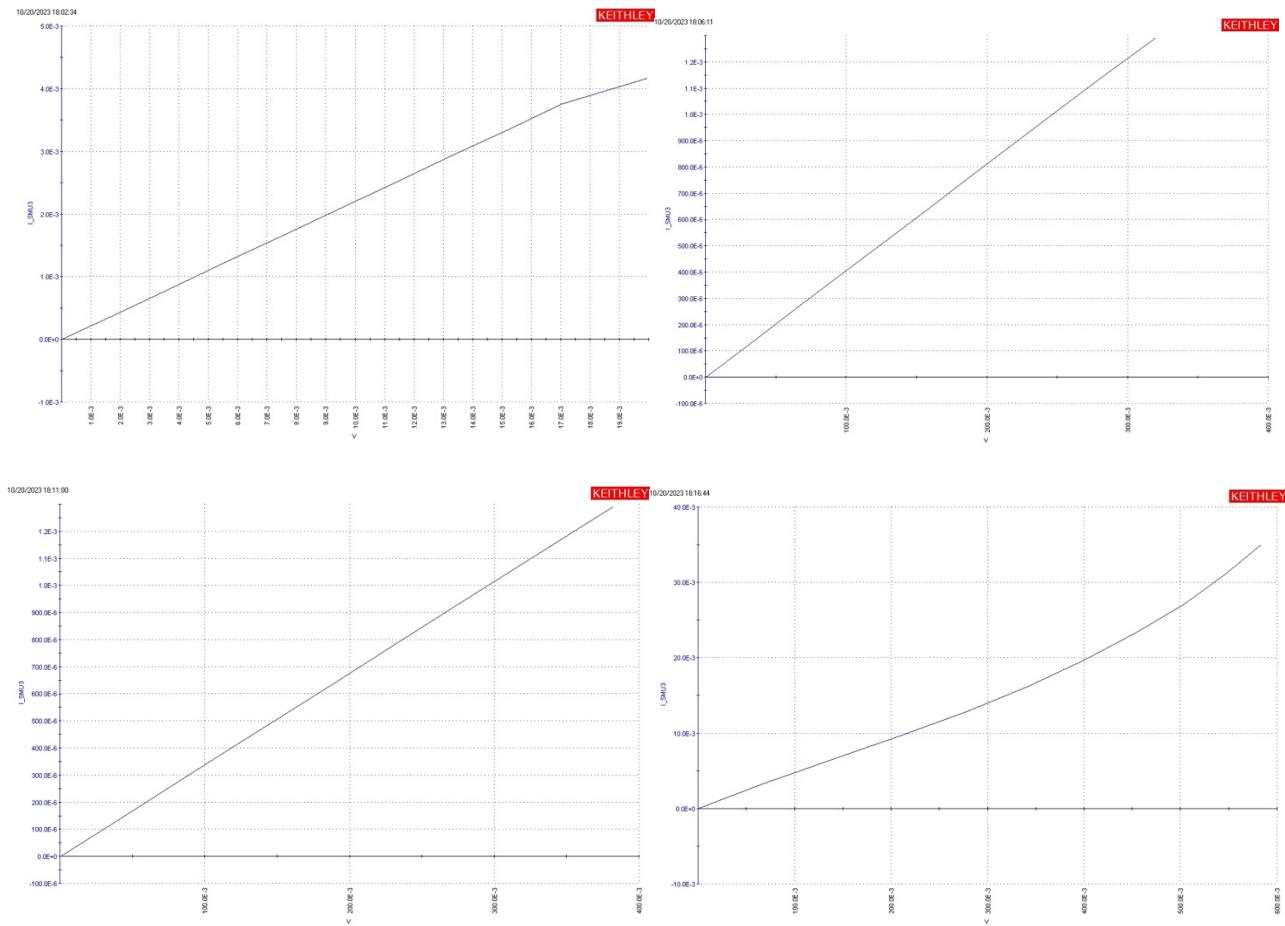


Figure 2: I-V curves obtained for n<sup>+</sup> diffusion in poly polysilicon

Table 1: Extracted and calculated data obtained for n<sup>+</sup> diffusion layers in single crystal silicon and polysilicon

	Unit	Single Crystal Silicon	Polysilicon
Sheet Resistance (R <sub>s</sub> )	Ω/sq	11.05	20.74
Line Width (W <sub>s</sub> )	μm	10.48	5.59
Line Spacing (S)	μm	0.53	2.79
Line Pitch (P)	μm	5.77	5.59
Contact Resistance (R <sub>c</sub> )	Ω/cm <sup>2</sup>	2.49	19.87

Table 2 potential reasons for differences between **Expected vs. Measured Results**

Potential factors impacting the difference	Single Crystal Silicon	Polysilicon
Sheet Resistance	impurities, crystal defects, or process variations	grain boundaries, impurities, or variations in the polysilicon structure
Line Spacing and Line Pitch	manufacturing tolerances and process variations	process variations in the fabrication of polysilicon structures.
Contact Resistance	surface conditions, interface quality, or process variations	surface conditions, doping levels, or process variations.

#### **Minimizing Differences in Electrical Linewidth:**

- (a) Process control: Regularly monitor and adjust key parameters in lithography, etching, and deposition processes.
- (b) Optical Proximity Correction (OPC): Implement OPC techniques to compensate for optical and process effects. This involves modifying the design layout to account for variations introduced during the lithography process.
- (c) Resolution Enhancement Techniques (RET): Use resolution enhancement techniques, such as phase-shifting masks and sub-resolution assist features, to improve the resolution and fidelity of fine features in the semiconductor design.
- (d) Mask Quality and Fabrication: Ensure the quality of photomasks used in the lithography process. Any defects or imperfections in the mask can lead to variations in the transferred pattern.

#### **Process Steps Affecting Contact Resistance:**

- (a) Surface Cleaning: The effectiveness of surface cleaning steps influences contact resistance. Ensure thorough cleaning to reduce surface contaminants.
- (b) Doping Levels: Optimize doping levels to enhance conductivity and minimize contact resistance.
- (c) Annealing Processes: Annealing steps can impact the quality of the interface. Proper annealing conditions contribute to lower contact resistance.
- (d) Material Deposition: Control deposition processes to ensure uniform and quality material interfaces, minimizing contact resistance.

#### **Achieving Low Contact Resistance**

- (a) Contaminants on the semiconductor surface can increase contact resistance. Effective cleaning ensures a clean and well-prepared surface for metal contact.
- (b) Higher dopant concentrations can enhance carrier mobility and conductivity, leading to lower contact resistance
- (c) Annealing can reduce defects, improve crystallinity, and enhance the bonding between the metal and semiconductor, resulting in lower contact resistance.

(d) Non-uniform deposition can lead to variations in contact resistance. Precise control ensures consistency across the semiconductor wafer.

### Differences in Measured Resistance Values:

Crystal structure: comparing to the polysilicon, the lack of impurities and uniformity in single crystal silicon contributes to low resistance. The absence of grain boundaries reduces scattering of charge carriers, enhancing electrical conductivity, since the boundaries would disrupt the flow of charge carriers, acting as obstacles. Apart from the above factor, inherent different materials and doping levels are also could be factors that makes the differences.

## 3.2 Diode Measurements

### Test 2: N+ p-Si Diode (turn-on and breakdown voltage)

Forward bias and reverse bias will lead I-V curve of diode to have one common feature, which the current will exponentially increase as voltage rises or goes down up to the special points. In forward bias region, the transition between -0.9 and 0.5 voltage, the current suddenly increased from  $-3.5308 \times 10^{-9}$  to  $-4.5955 \times 10^{-6}$ . This transition point is called turn-on voltage or threshold voltage. On the other hand, in the reverse bias region, the transition between -13.5 and -14.0 voltage, the current suddenly increased from  $-113.5925 \times 10^{-9}$  to  $-56.8582 \times 10^{-6}$ . This transition point is called breakdown voltage. The equations of turn-on voltage and breakdown voltage are showed below, respectively. In the reverse bias region, the reverse current sharply increases, and the diode can be damaged if the reverse voltage exceeds its breakdown voltage.

The equations for both turn-on voltage and the breakdown voltage are showed below, respectively.

$$I = I_0(\exp(\frac{qV_A}{nkT}) - 1) = eA(\frac{D_p p_{eo}}{L_p} + \frac{D_n n_{eo}}{L_n})(\exp(\frac{qV_A}{nkT}) - 1) \sim eA(\frac{D_n n_{eo}}{L_n})(\exp(\frac{qV_A}{nkT}) - 1)$$

$V_A$ : turn-on voltage

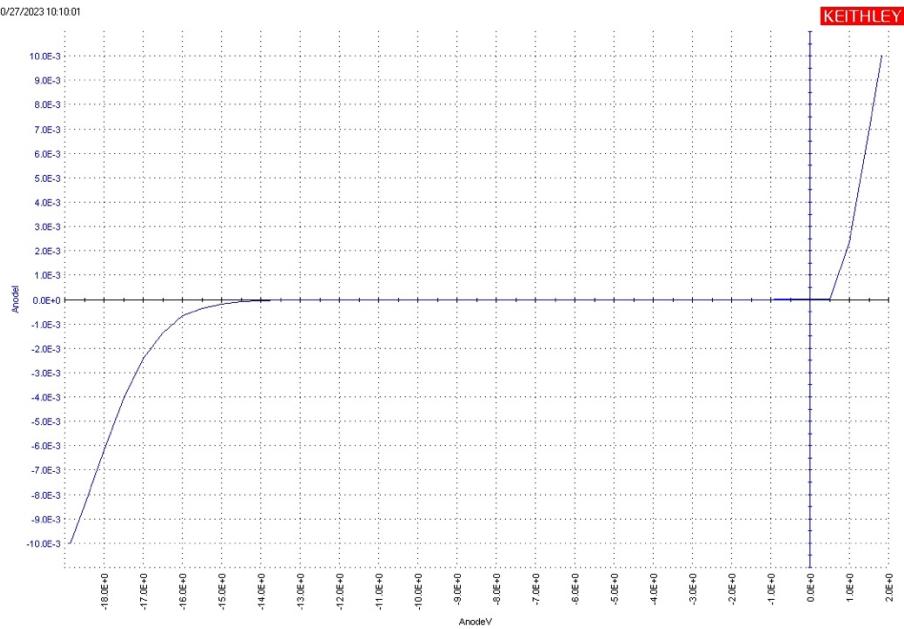
$$V_{br} = \frac{eE_{br}^2}{2eN_d}$$

$V_{br}$ : breakdown voltage

Table 3: turn-on voltage and the breakdown voltage

Turn-on voltage (threshold voltage)	Breakdown voltage
0.5	-14.0

Figure 3: The diode I-V curves



Discrepancies between expected and measured turn-on voltage or breakdown voltage may arise due to fabrication tolerances, impurities, or temperature variations. Moreover, materials properties, such as different materials have different bandgap, and doping levels are also one of the impacting factors for the difference. For example, higher doping levels in the diode reduce the turn-on voltage. In other words, it becomes easier to conduct.

#### **Designing for High Breakdown Voltage:**

- (a) Materials: Choose materials known for their superior breakdown characteristics, such as silicon carbide (SiC) or gallium nitride (GaN). For instance, using temperature effects on breakdown voltage chooses materials with a lower temperature coefficient of breakdown voltage.
- (b) Ion Implantation: Utilize ion implantation techniques for precise doping control, ensuring a tailored doping profile for optimized breakdown characteristics.
- (c) Epitaxial Growth: Consider epitaxial growth processes to produce thin, high-quality semiconductor layers with controlled doping for improved breakdown performance.

### **3.3 MOSFET Measurements**

#### **Test 3: Field Effect Transistor Measurements**

##### **A1: Drain characteristics ( $I_{DS}$ vs. $V_{DS}$ ): demonstrate basic transistor operation**

The primary objective of this experiment is to investigate the drain characteristics of Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) with varying channel lengths. The study focuses on understanding how the transistor's drain current responds to different drain-source voltages and gate-source voltages. By varying the channel lengths ( $L_{mask} = 2, 3, 4, 5, 10$ , and  $40 \mu\text{m}$ ), the experiment aims to observe how the device's characteristics change, especially in short-channel devices. In this section, we implement multiple measurements to attain the following data

needed for comparison, drain characteristics ( $I_D$  vs  $V_{DS}$ ), linear characteristics with substrate bias ( $I_D$  vs  $V_{GS}$  with varying  $V_{SB}$ , and subthreshold characteristics ( $I_D$  vs  $V_{GS}$  at small  $V_{GS}$ ).

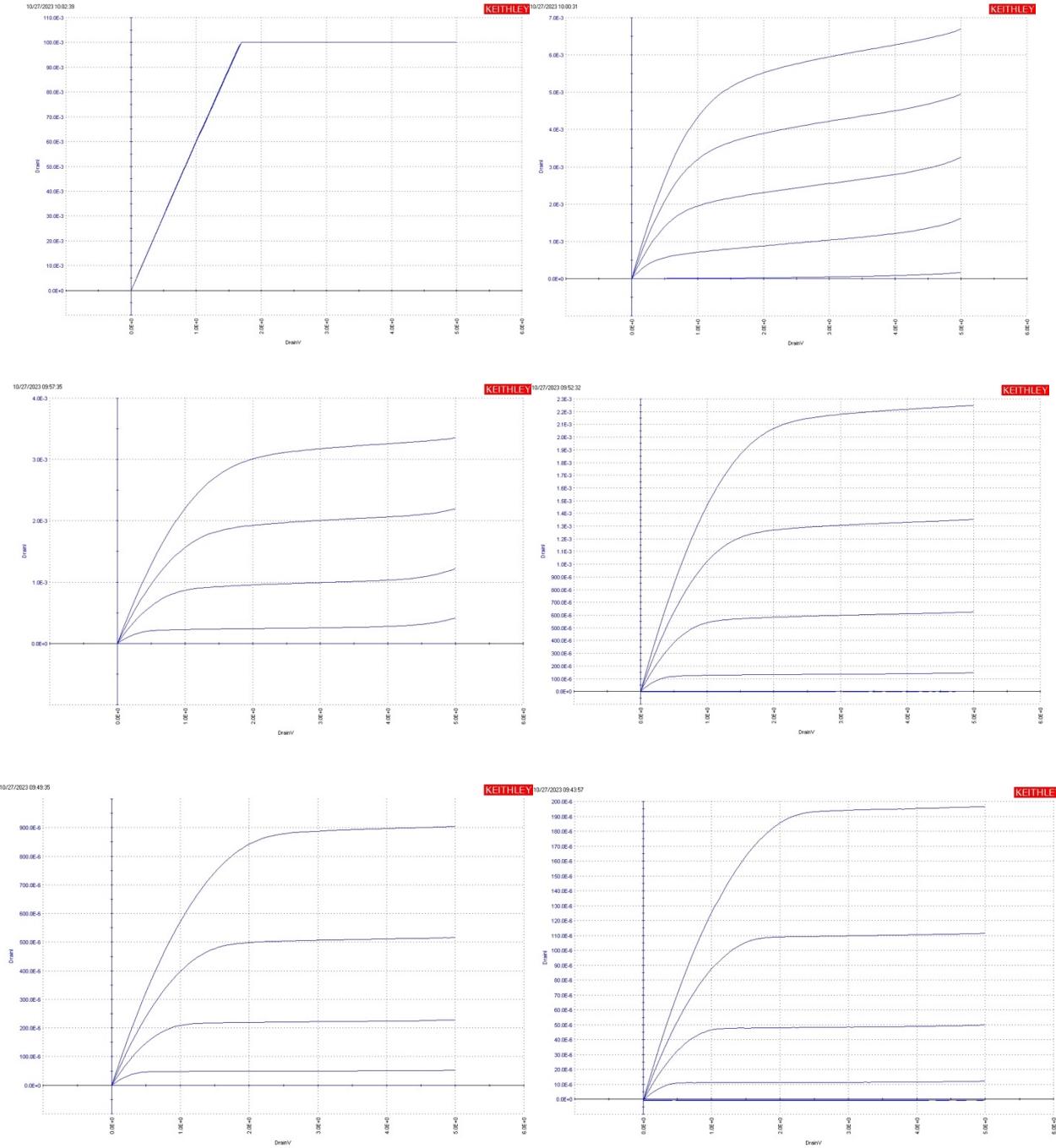


Figure 4:  $I_D$  vs  $V_{DS}$  of 6 transistors with width=40  $\mu\text{m}$  and Lmask=2, 3, 4, 5, 10 and 40  $\mu\text{m}$   
The equations of calculating the drain current are presented below.

$$I_D = k'_n \frac{W}{L} \left[ V_{GS} - V_T - \frac{V_{DS}}{2} \right] V_{DS}$$

where  $k'_n = \mu_n C_{ox}$

For linear region ( $0 < V_{DS} < V_{GS} - V_T$ ):

process transconductance parameter

$$I_{DSAT} = \frac{k'_n}{2} \frac{W}{L} (V_{GS} - V_T)^2$$

where  $k'_n = \mu_n C_{ox}$

For saturation region ( $V_{DS} > V_{GS} - V_T$ ):

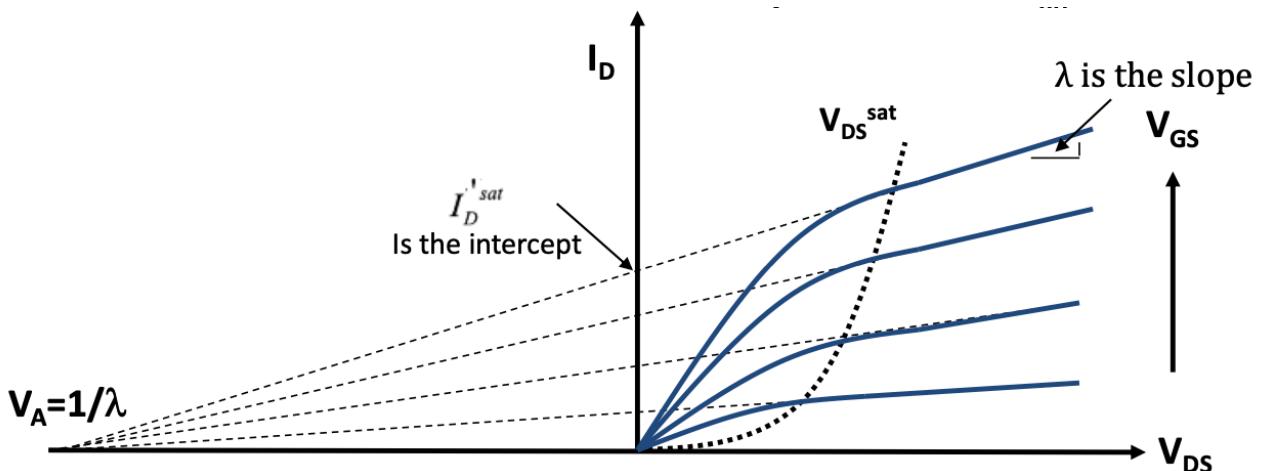
The above six figures show when the channel length ( $\Delta L$ ) is extended, the drain current appears to stabilize, resulting in relatively consistent values across varying drain-source voltages. This phenomenon contrasts with shorter channel lengths, where the drain current tends to display more dynamic behaviour, often characterized by pronounced upward tails.

The exceedingly short channel length, as exemplified by the 2μm diagram presented earlier, facilitates the creation of a conducting channel even in the absence of an externally applied gate-source voltage. This occurrence is attributed to **short-channel effects**, including impact ionization and velocity saturation, which become increasingly pronounced as the channel length diminishes. These effects contribute to the premature establishment of a conductive channel, causing the drain current to rise linearly in a manner that extends beyond the linear region and approaches the upper boundaries of the measurement instrument's current capacity.

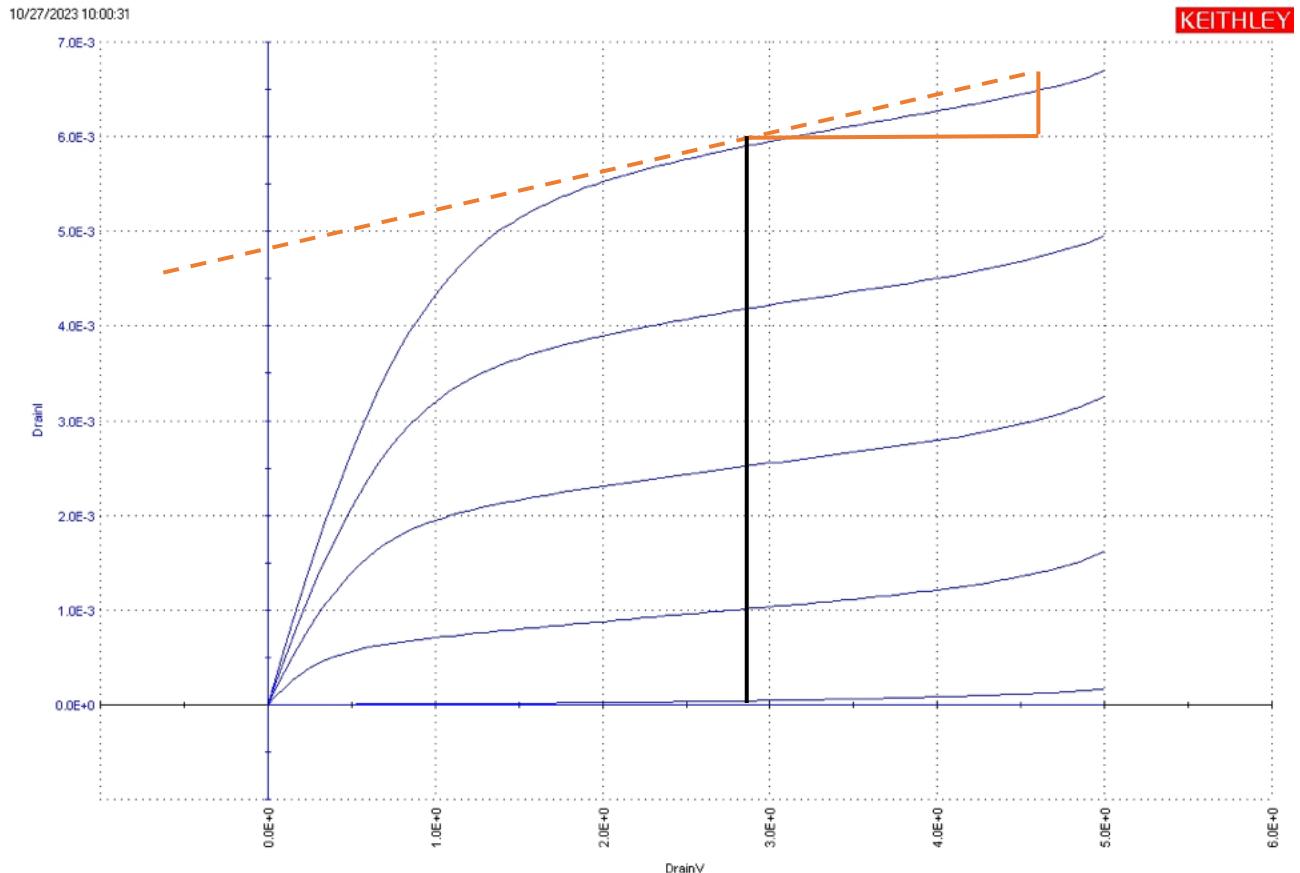
As the channel length decreases, electron velocities in the channel can approach a saturation limit, leading to reduced mobility. This is called velocity saturation, and this also can explain why the drain current stabilizes after drain voltage applied to certain points. However, short-channel effects impact the magnitude of drain current in saturation region, making the drain current still can increase when we apply more drain voltage. The degree of how much drain current will be can be attained based on the **channel length modulation ( $\lambda$ )**. The equation of drain current in saturation region impacted by the short-channel effects is showed below.

$$I_{DS} = \frac{1}{2} \mu_{eff} C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

To get the channel length modulation ( $\lambda$ ) for  $V_{GS}=5$ , we need to calculate the slope of that curve on the diagram.  $V_A$  is called **early voltage**.



- Take the channel length=3μm for example to calculate the ( $\lambda$ ) for  $V_{GS}=5$ .



Steps:

1. Pick up two points on the curve, (5.00037, 0.00669) and (3.15008, 0.00600)
2. slope=(Y<sub>2</sub>-Y<sub>1</sub>)/(X<sub>2</sub>-X<sub>1</sub>)
3. slope=3.729x10<sup>-4</sup>

Table 4: channel length vs channel length modulation parameter ( $\lambda$ ) for  $V_{GS} = 5$

Channel length (μm)	channel length modulation ( $\lambda$ ) for $V_{GS}=5$
2	5.878x10 <sup>-2</sup>
3	3.729x10 <sup>-4</sup>
4	1.139x10 <sup>-4</sup>
5	4.491x10 <sup>-5</sup>
10	1.000x10 <sup>-5</sup>
40	1.629x10 <sup>-6</sup>

Based on the calculation values in the table 4, as the channel length decreases, the impact of Channel Length Modulation ( $\lambda$ ) tends to increase. The increase in prominence of channel length modulation as the channel length decreases is primarily attributed to the spatial extension of the depletion region near the drain, leading to the effective channel length ( $L_{eff}$ ) becoming smaller than the physical channel length. Therefore, these measure results are expected. The reason why reducing the effective channel length is that as  $V_{DS}$  increases, the electric field between the drain and the channel also increases, which extends the depletion region deeper into the channel from the

drain terminal. Moreover, same trend can be attained if we increase drain voltage. The relationship between effective channel length and both physical channel length and drain voltage is showed.

$$L_{\text{eff}} = L - \lambda \cdot V_{DS}$$

## A2: Linear region characteristics ( $I_{DS}$ vs. $V_{GS}$ )

### Transconductance

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}}$$

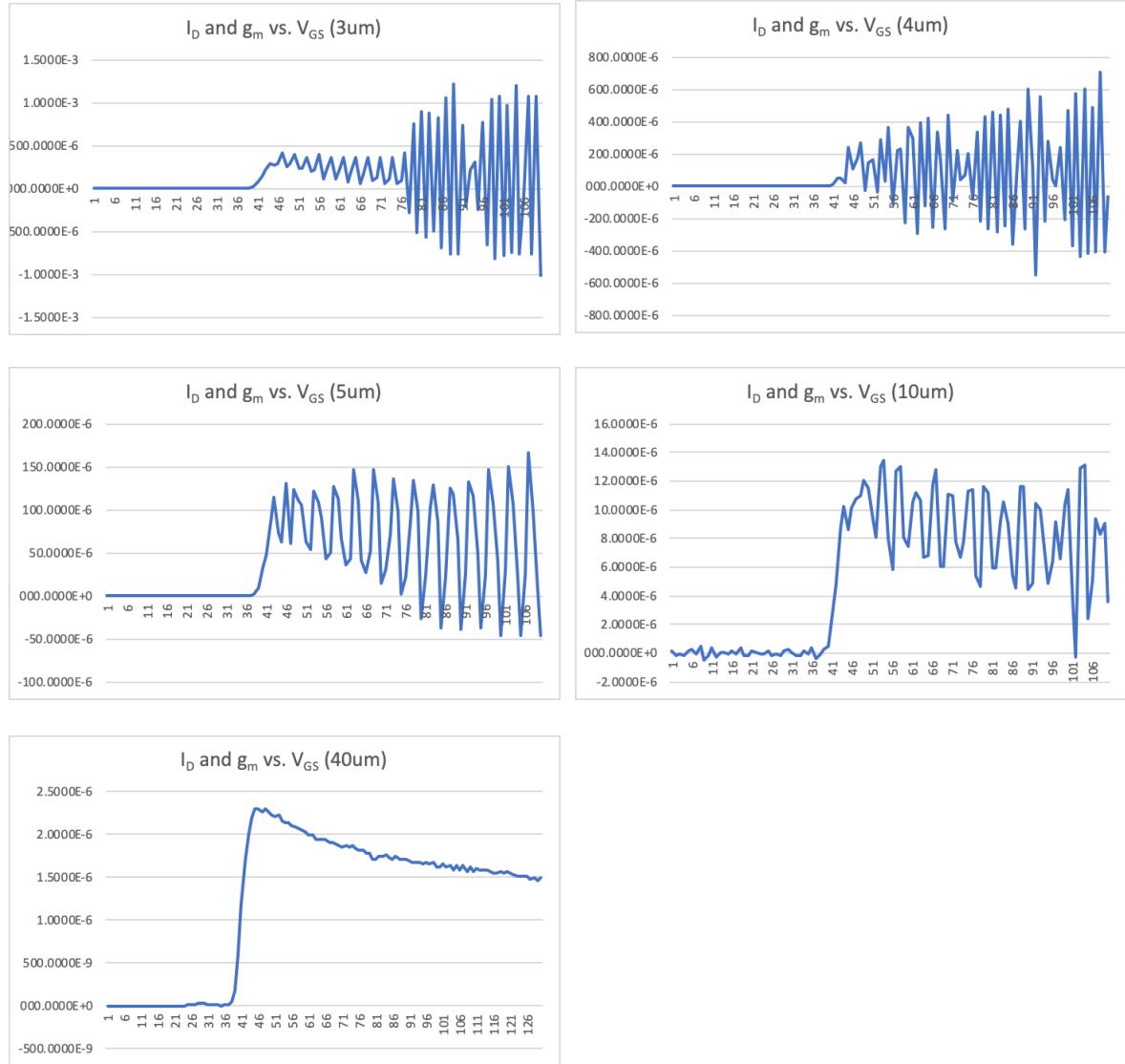


Figure 5:  $I_D$  and  $g_m$  vs.  $V_{GS}$

### Threshold voltage

$$V_T = V_{GS,0} - V_{DS}/2$$

Where  $V_{GS,0}$  is the extrapolate point to zero  $I_D$

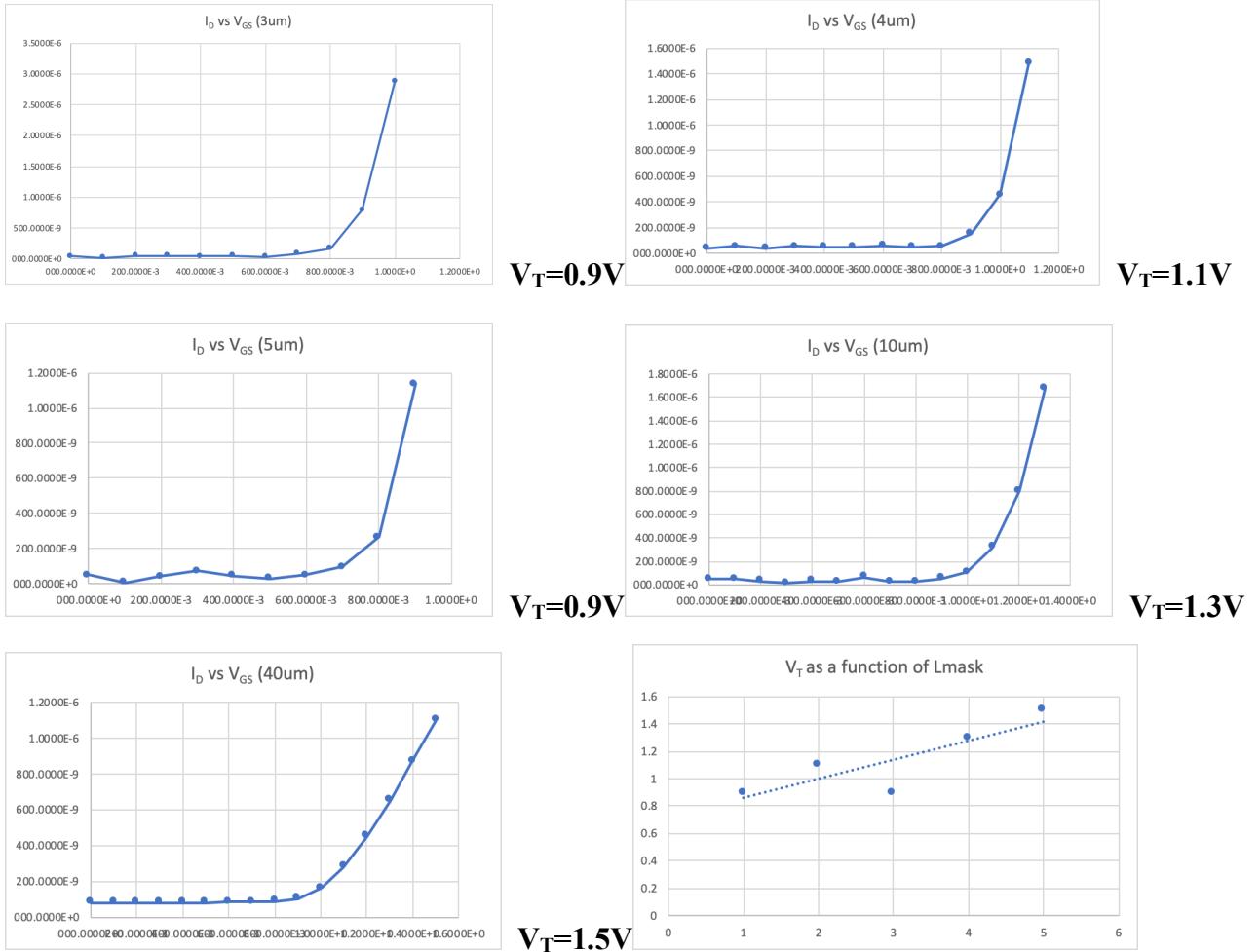


Figure 6: extracted  $V_T$  on the  $I_D$  vs  $V_{GS}$  and  $V_T$  as a function of  $L_{mask}$

Based on the figure 6, the dash line (trend) indicates that if we increase the channel length, the threshold voltage we also increase, which requires larger gate voltage to activate the device. In other words, we can shorten the channel length to make threshold voltage decrease, which means that we can activate the device without applying larger amount of the voltage. This result corresponds to the expectation. The reason why  $V_T$  varies with  $L_{mask}$  is that shorter channels have a smaller physical separation between the gate and the channel, leading to a higher capacitance.

$$V_T = V_{FB} + \frac{\sqrt{2\epsilon_s(2|\Phi_F|)qN_a}}{C_{ox}} + 2|\Phi_F|$$

we can simplify this into the following equation.

$$V_T = V_{FB} + 2\sqrt{\frac{q\epsilon_s N_a}{2C_{ox}}}$$

, where  $V_{FB}$  is the flat-band voltage,  $q$  is the elementary charge,

$\epsilon_s$  is the permittivity of silicon,  $N_a$  is the acceptor doping concentration, and  $C_{ox}$  is the oxide capacitance.

Table 5 shows the comparison for  $\Delta L$  vs  $g_m$  obtained in this set of measurements to those obtained in part A1. We can find out that maximum of transconductance will decrease if the channel length increases. Longer channels provide more resistive paths for the flow of charge carriers. This increased resistance reduces the ability of the device to amplify input signals, leading to a decrease in transconductance. Based on the following results, we can also find out that longer channels result

in lower transconductance and reduced sensitivity to changes in the gate voltage. Therefore, the channel length modulation and the maximum of transconductance have the same trend.

Table 5: the comparison for channel length modulation and maximum of transconductance with various channel length

Channel length ( $\mu\text{m}$ )	channel length modulation ( $\lambda$ ) for $V_{GS}=5$	maximum ( $g_m$ )
2	$5.878 \times 10^{-2}$	--
3	$3.729 \times 10^{-4}$	$1.214 \times 10^{-3}$
4	$1.139 \times 10^{-4}$	$7.049 \times 10^{-4}$
5	$4.491 \times 10^{-5}$	$1.664 \times 10^{-4}$
10	$1.000 \times 10^{-5}$	$1.343 \times 10^{-5}$
40	$1.629 \times 10^{-6}$	$2.296 \times 10^{-6}$

source / drain contact resistances and  $\Delta L$  from using channel resistance method

$$V_{GS,ex} = V_{GS} + I_D R_S$$

$$R_{tot} = \frac{V_{DS,ex}}{I_D}$$

$$= [R_S + R_D + R_{ch}]$$

$$V_{DS,ex} = V_{DS} + I_D (R_S + R_D)$$

$$= [R_{SD} + R_{ch}]$$

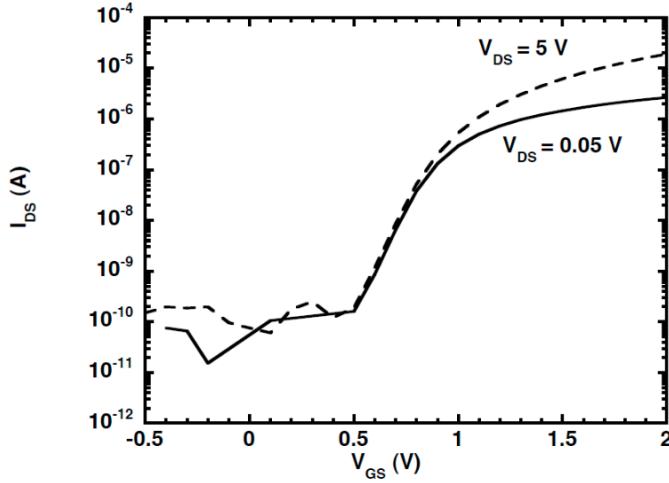
Once we know the  $V_{DS,ex}$ , we can get  $R_{SD}$  by  $R_{total} - R_{ch}$ .

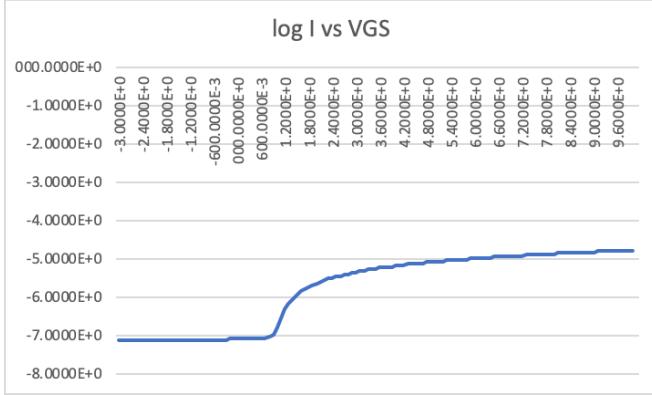
For  $L_{mask} = 40 \mu\text{m}$  only, extract electron inversion layer mobility ( $\mu$ ) vs. gate field ( $E_{eff}$ ); the body effect coefficient ( $\gamma$ ) and the substrate doping ( $N_A$ )

### A3: Subthreshold characteristics (log $I_{DS}$ vs. $V_{GS}$ ).

For  $L_{mask} = 40 \mu\text{m}$  transistors only with  $V_{DS} = 50 \text{ mV}$  and  $5 \text{ V}$ ;  $V_{SB} = 0$ ;  $-0.5 < V_{GS} < 2 \text{ V}$ .

#### Subthreshold Current for $40 \mu\text{m}$ long MOSFET





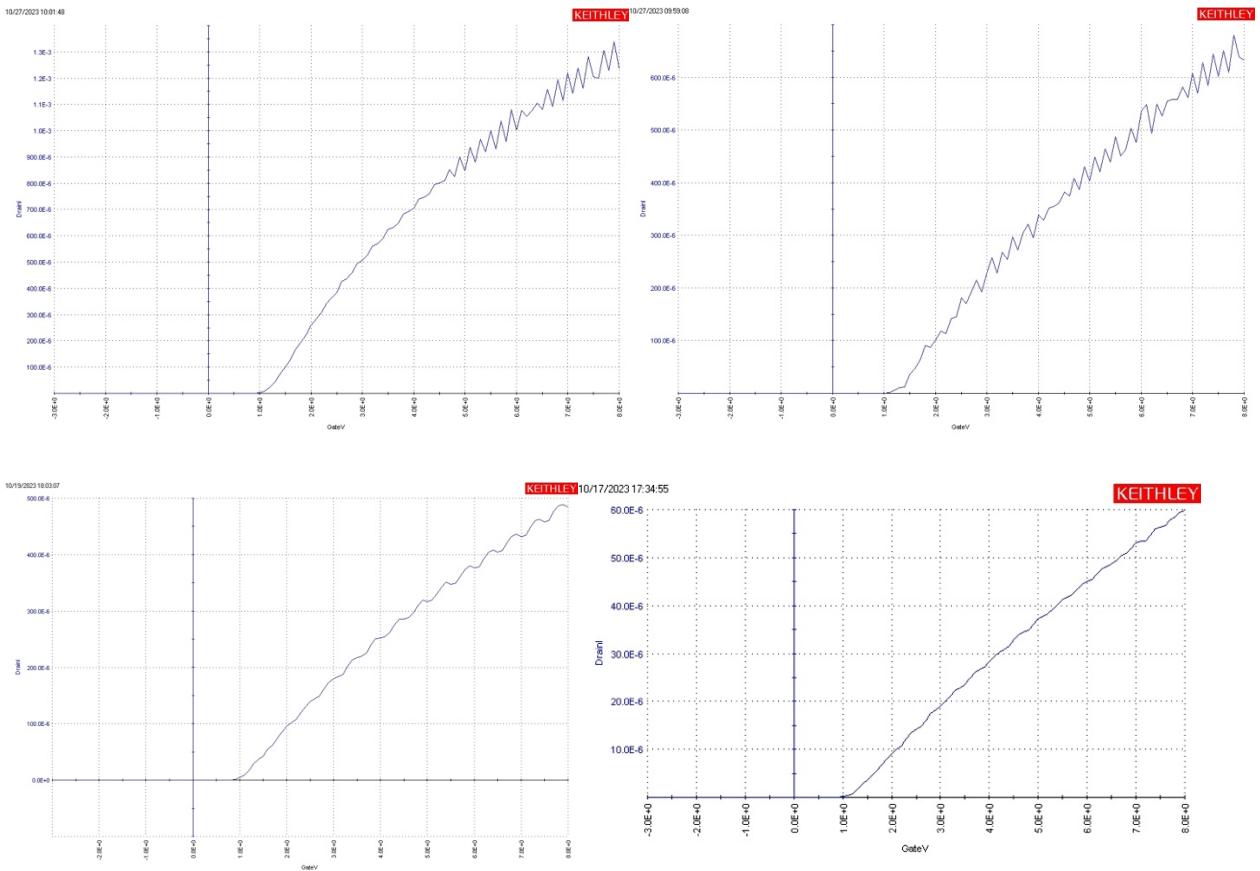
To get the background device leakage current and the subthreshold slope S (mV/decade), we need the following equation.

$$S = \frac{\partial V_{GS}}{\partial \log I_D}$$

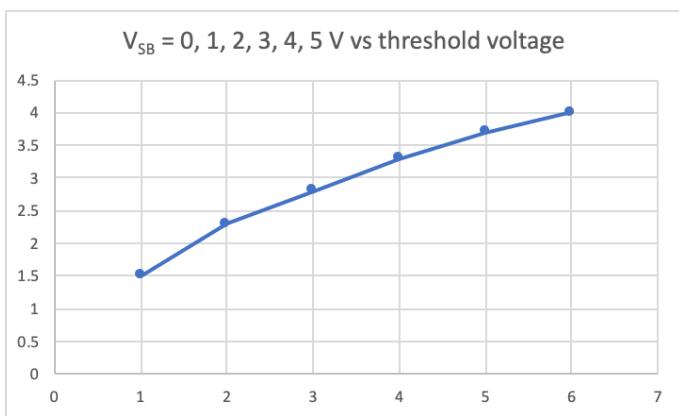
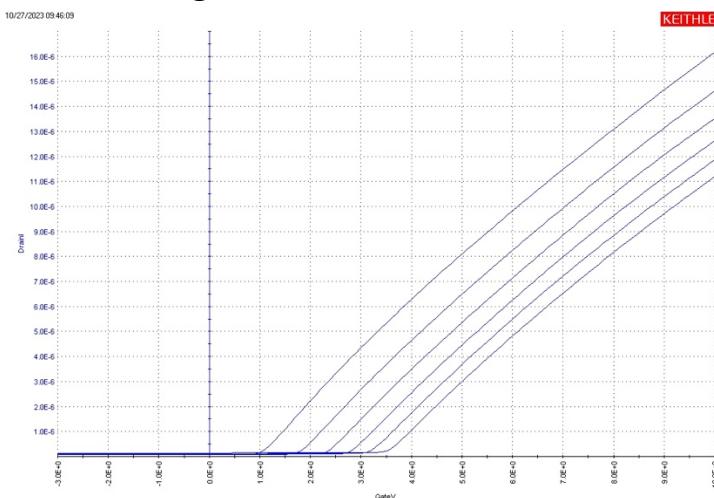
This is the slope of curve on the above diagram of  $\log I$  versus  $V_{GS}$ . We can get this value by taking the slopes of the points between the leakage current and the current.

$S = 8.0685$  mV/decade, and leakage current is  $122.7805 \times 10^{-9}$

To reduce S to get better design, we can use 4 major ways to achieve. Implementing **well-controlled doping profiles** can enhance the electric field control and reduce S. **Use high-k dielectric materials** in the gate oxide to reduce gate leakage current and improve electrostatic control. Explore advanced **gate structures**, such as FinFETs or nanowire FETs, which offer improved electrostatic control and reduced short-channel effects. Consider **ultra-thin body devices** to improve gate control over the channel. For better process, we can introduce **low-resistance contacts** to minimize parasitic resistances, which can contribute to better subthreshold swing. Implement **low-temperature** processing techniques to reduce defects and improve the quality of the gate oxide.

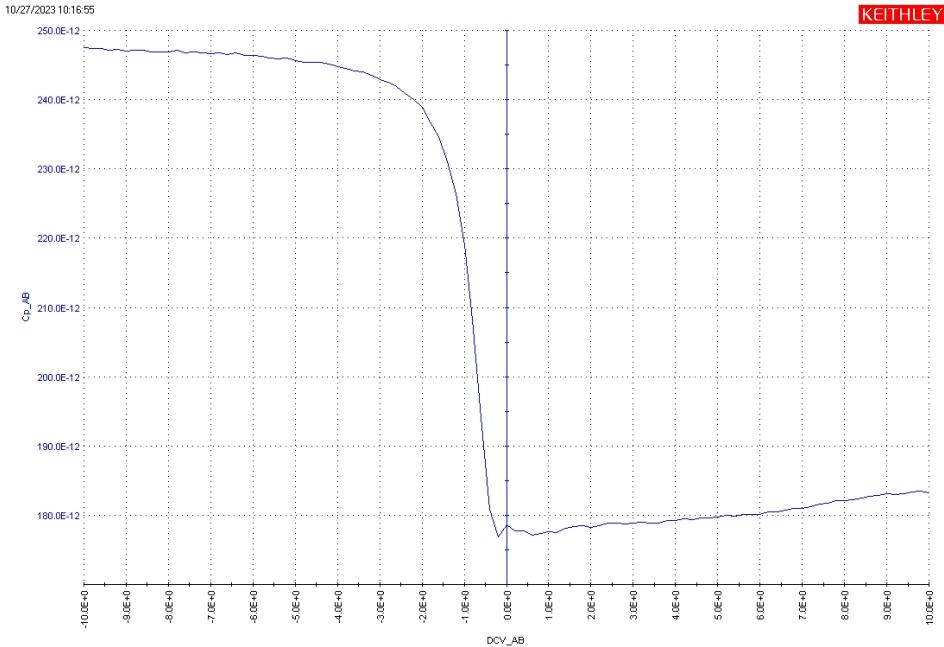


#### A4: Linear region characteristics for Field Transistors ( $I_{DS}$ vs. $V_{GS}$ )



We can find out that threshold voltage increases with increasing subthreshold voltage.

### 3.4 Capacitor Measurements



#### A) Oxide capacitance and oxide thickness

$$C_{ox} = \frac{E_{ox}A}{t_{ox}}$$

$$C_{max} = C_{ox} = 247 * 10^{-12} F$$

$$t_{ox} = 39.5 nm$$

#### B) Substrate Doping

$$C_{min} = 176 * 10^{-12} F$$

$$C_{min} = \frac{C_{s(min)}C_{ox}}{C_{s(min)} + C_{ox}} \quad C_{s(min)} = \frac{E_{si}}{W_{d(max)}}$$

$$W_{d(max)} = \left( \frac{2E_{si}\phi_{s(max)}}{qN_A} \right)^{1/2} = 2 \left( \frac{E_{si}\phi_B}{qN_A} \right)^{1/2} \text{ where } \phi_B = \frac{kT}{q} \ln \left( \frac{N_A}{n_i} \right)$$

$$N_A = 2.12 \times 10^{16} cm^{-3}$$

**Comparing with the measured  $N_A$ :  $3.96 \times 10^{-3}$**

The observed disparity can be elucidated from various viewpoints. The capacitance of MOS (Metal-Oxide-Semiconductor) structures is intricately linked to the surface state of the oxide and semiconductor interface. Factors such as impurities, defects, or other non-ideal elements within the actual device might contribute to this deviation. Furthermore, the influence of temperature on MOS capacitance cannot be overlooked. If there are any leakage currents present, even in static conditions, they could introduce fluctuations in capacitance values.

#### C) Flat-band voltage and fixed oxide charge density.

$$V_{FB} = \phi_{ms} - \frac{Q_f}{C_{ox}} \quad \phi_{ms} = -\frac{E_g}{2} - \phi_B = -\left[\frac{E_s}{2} + \frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right)\right]$$

The presence of oxide charge plays a pivotal role in influencing the electric field distribution between the gate electrode of a Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) and the semiconductor. This influence can result in a deviation of the threshold voltage, potentially causing the MOSFET to display distinct on and off states even under identical gate voltage conditions. Such variations can significantly impact the performance of applications like logic gates in digital circuits and amplifiers in analog circuits.

Consequently, these shifts in characteristics can be observed through alterations in the capacitance-voltage (C-V) curve, attributed to changes in the flatband voltage ( $V_{FB}$ ).

To mitigate the impact of oxide charge on MOSFET performance, strategic measures can be implemented in the oxide layer preparation processes. One effective approach involves employing high-quality oxide layer preparation techniques, such as thermal oxidation. By meticulously controlling parameters such as temperature, duration, and atmospheric conditions during the oxidation process, a more uniform and stable oxide layer can be achieved, consequently minimizing the introduction of oxide charges.

Following the oxide layer preparation, a thermal annealing process can be employed as an additional step to further diminish the presence of oxide charge. This post-preparation treatment contributes to refining the properties of the oxide layer.

Moreover, the choice of materials for the oxide layer is pivotal. Opting for materials with high dielectric constants, such as HfO<sub>2</sub>, proves advantageous. This choice not only enables a reduction in the thickness of the oxide layer but also serves to decrease the overall number of fixed charges. Such meticulous material selection enhances the overall quality of the oxide layer, thereby promoting improved MOSFET performance and reliability in various applications.

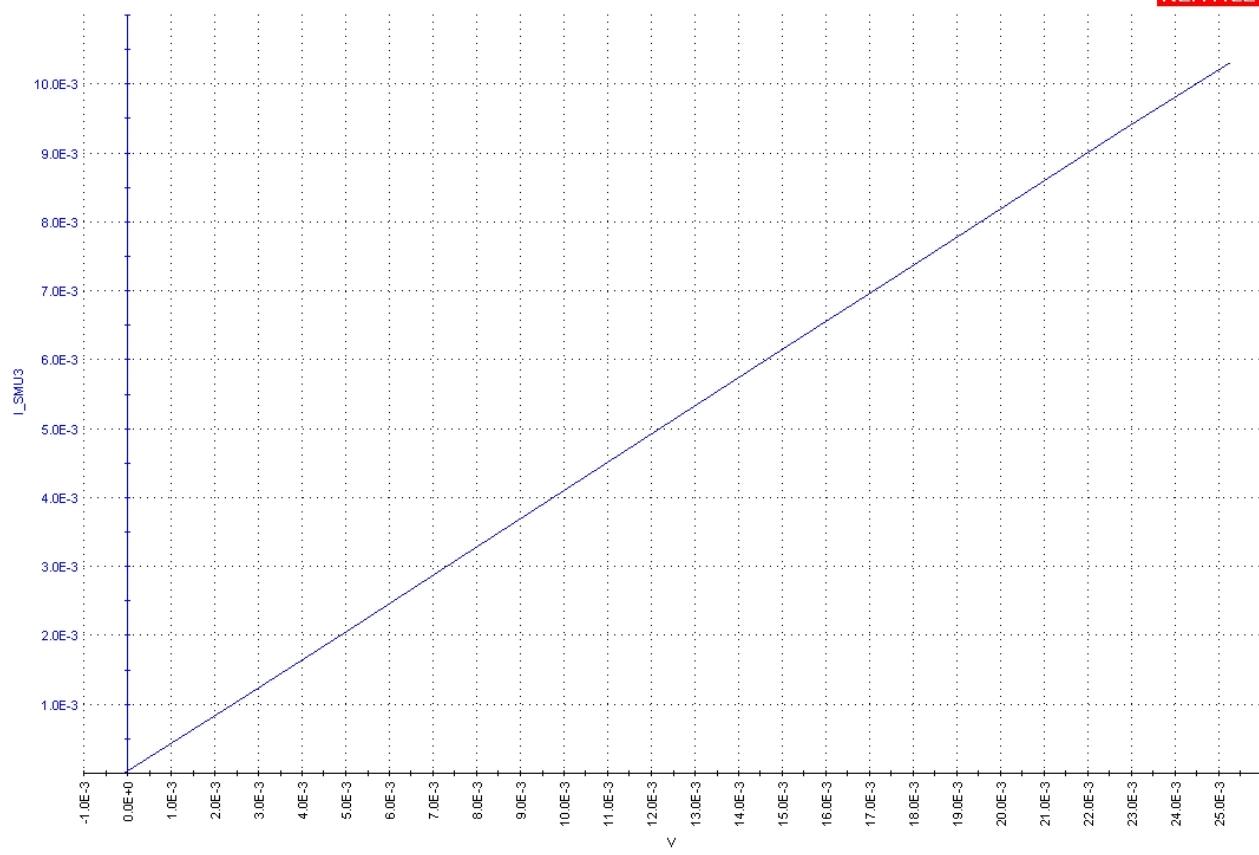
## 4. Conclusion

In this experimental study, our primary objective is to assess specific characteristics of electronic devices. Initially, we will apply the techniques acquired in class to measure diverse resistances inherent in devices, including sheet resistance and contact resistance. Subsequently, we will delve into the electrical properties associated with PN junctions. To complete our investigation, we will scrutinize the voltage and current characteristics of MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors). Given the ubiquity of MOSFETs in contemporary integrated circuits, our exploration will extend to the examination of short-channel effects and the intricacies of MOS capacitance. This experiment holds significant value as it bridges our theoretical simulations with real-world applications, providing a comprehensive understanding of these devices' characteristics.

## Figure Data

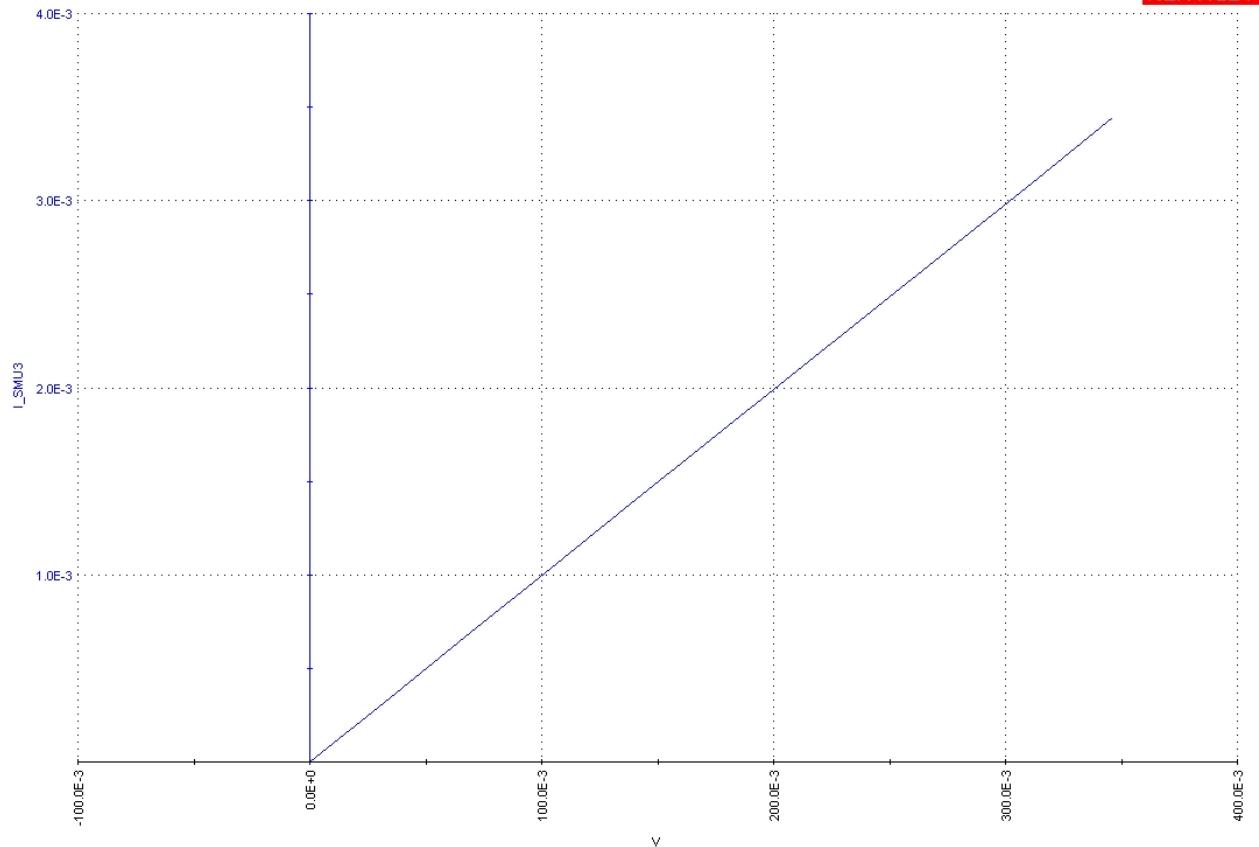
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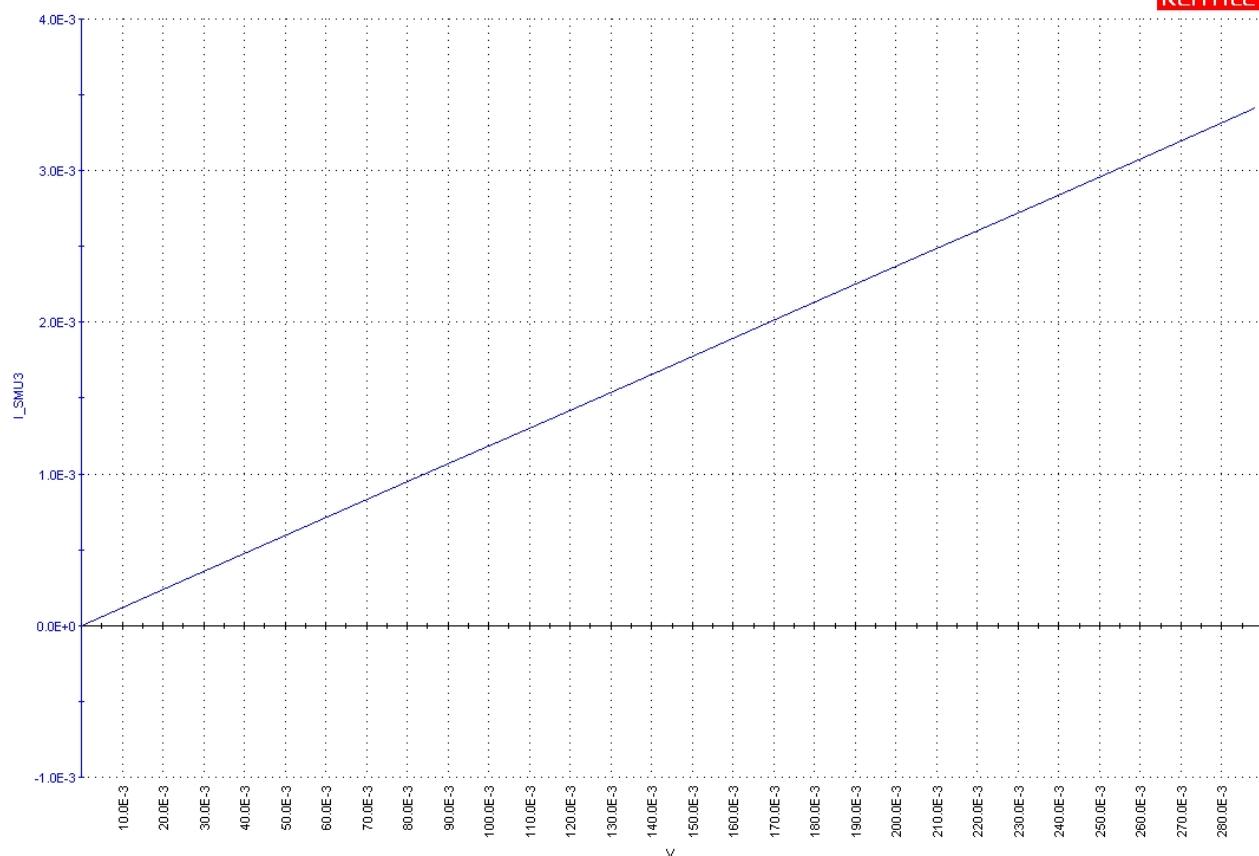
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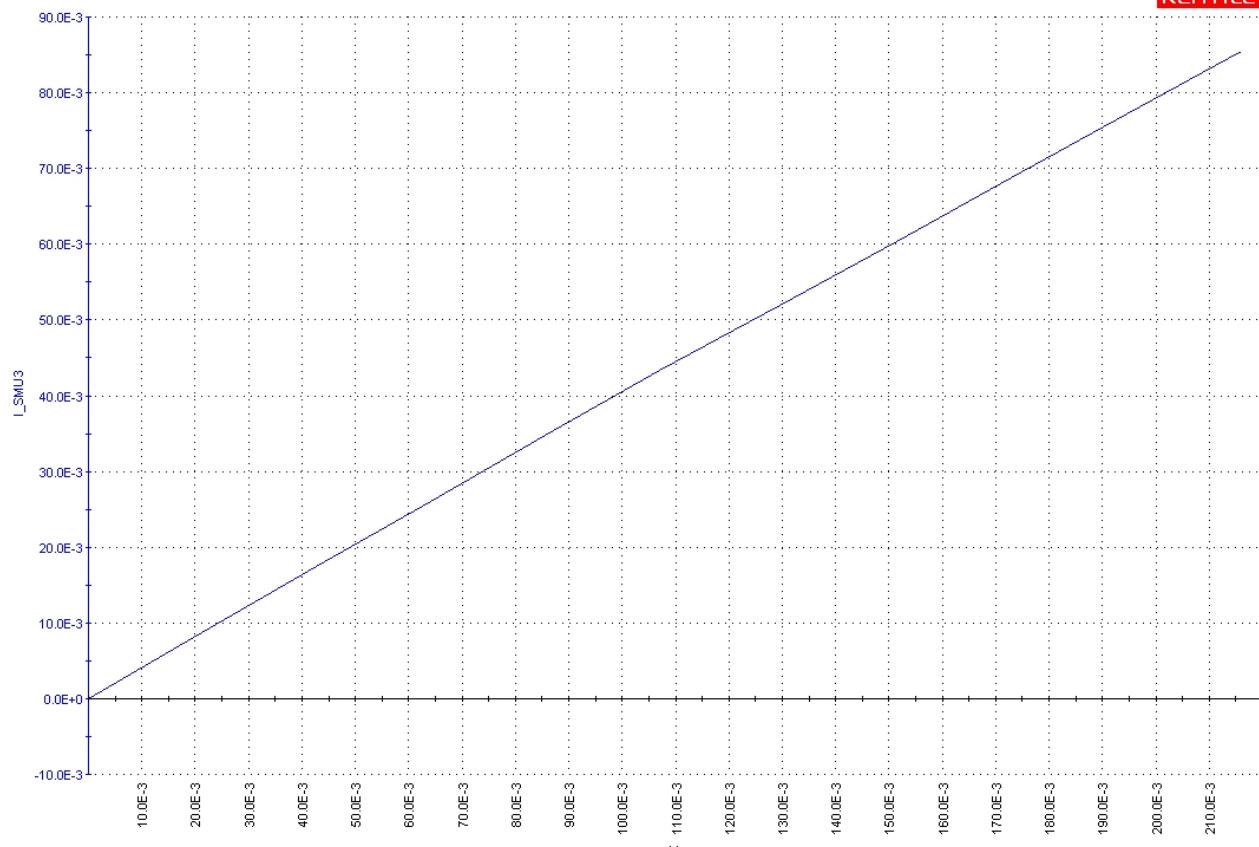
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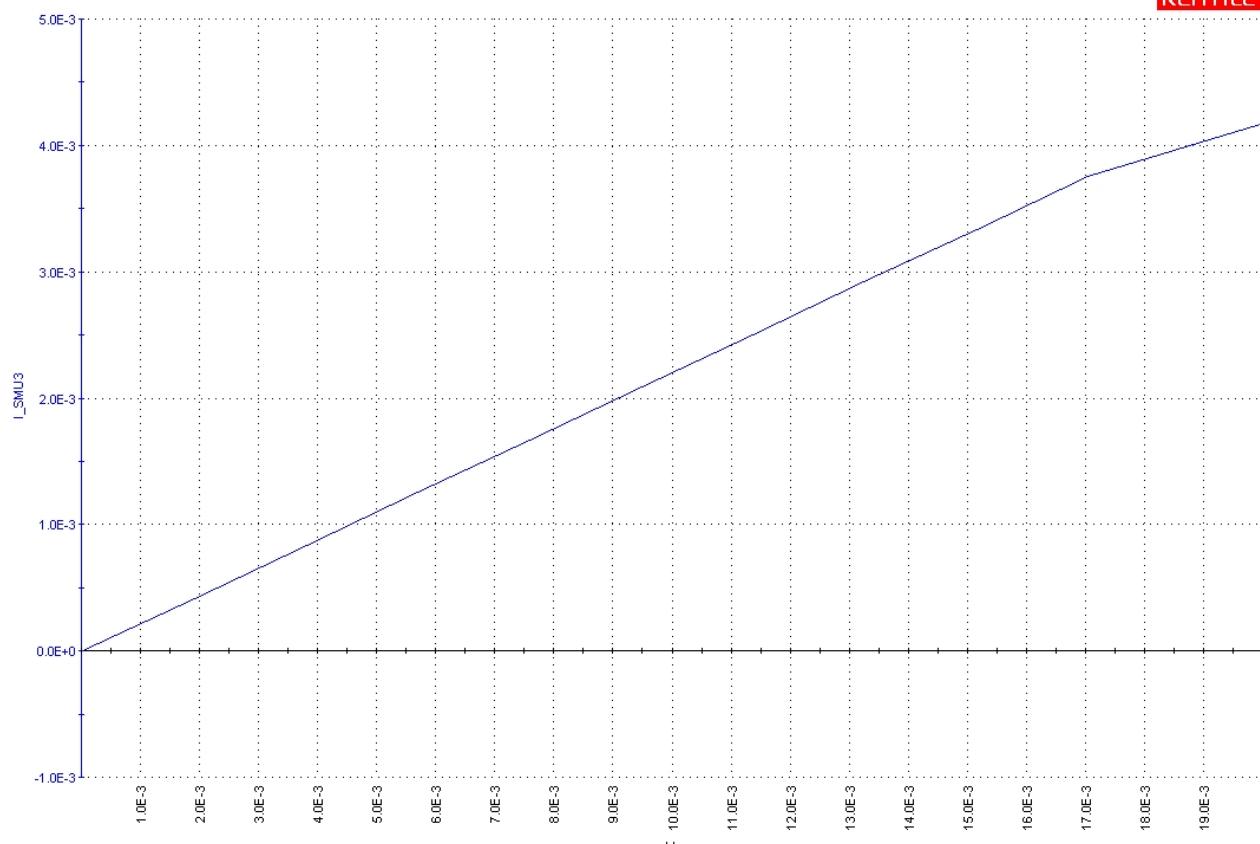
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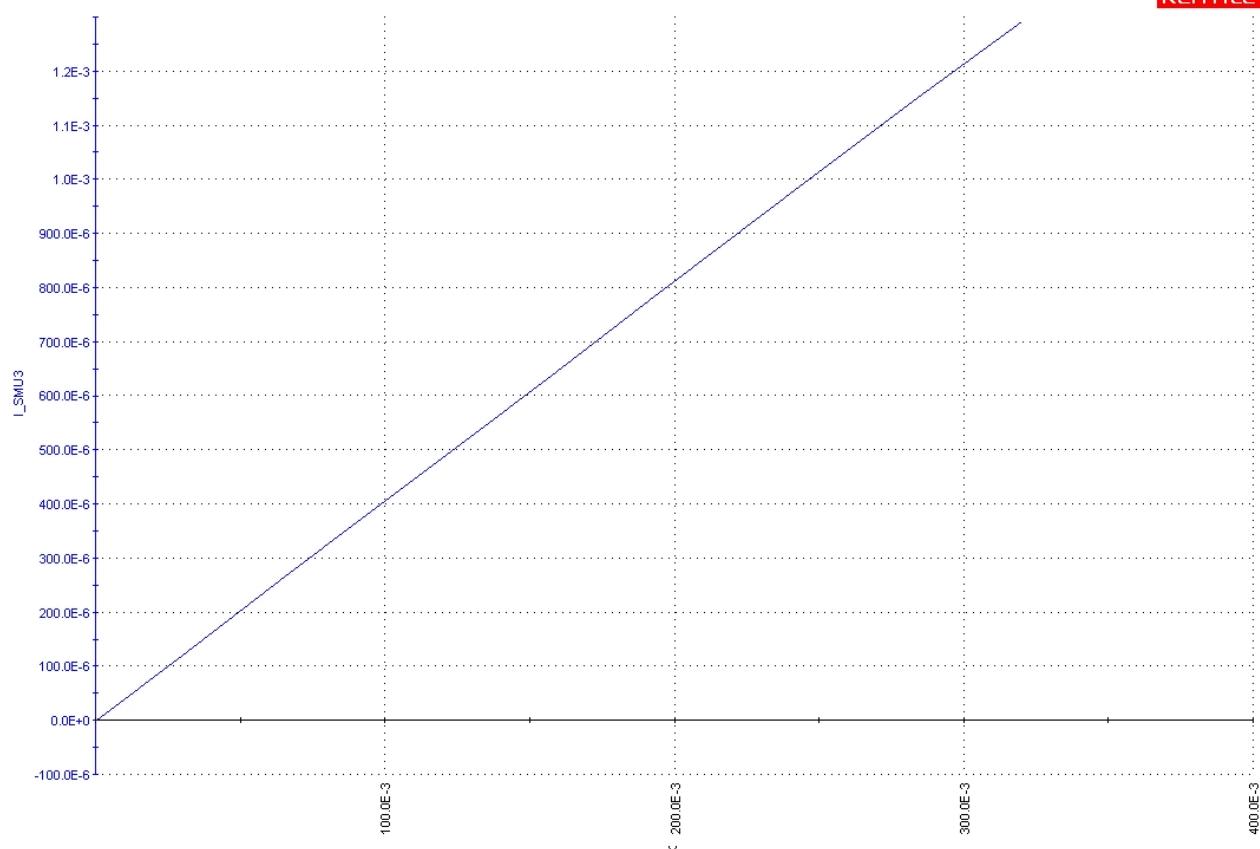
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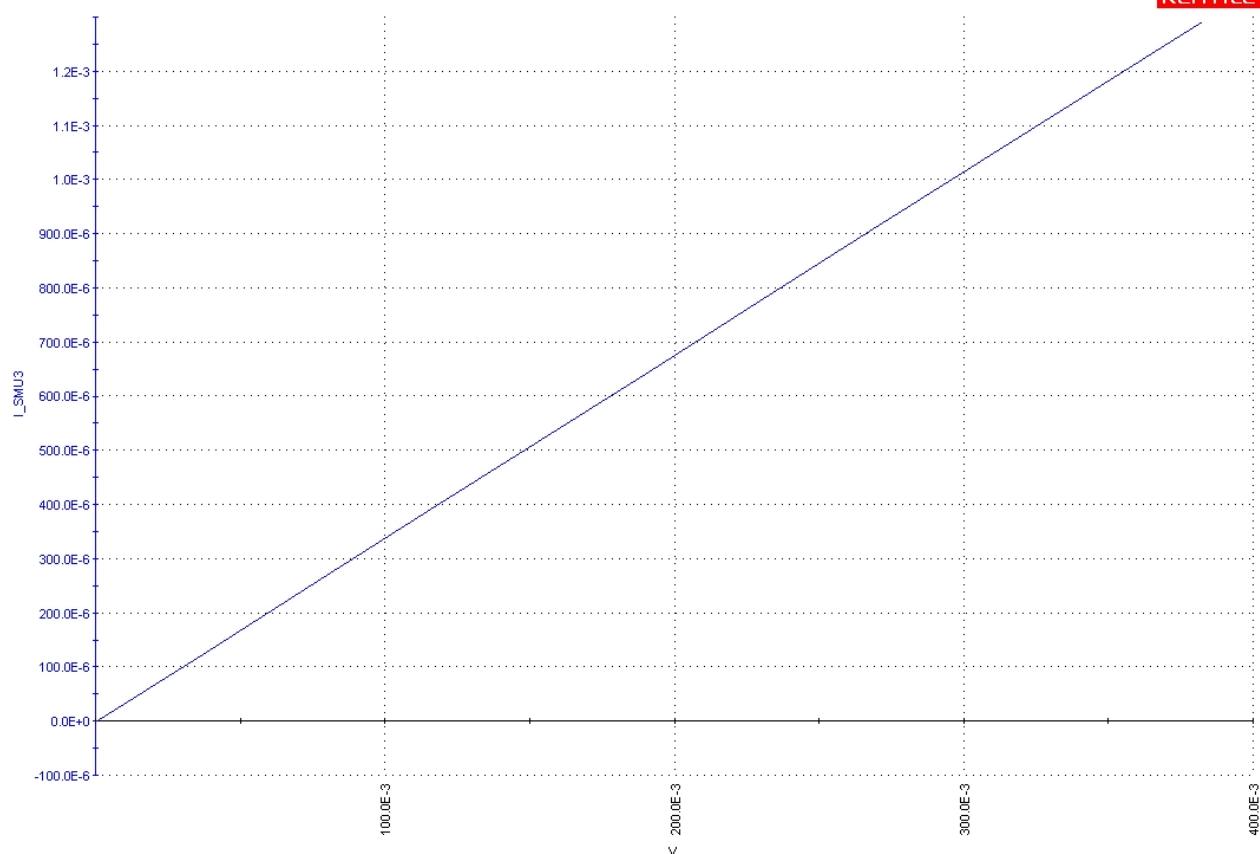
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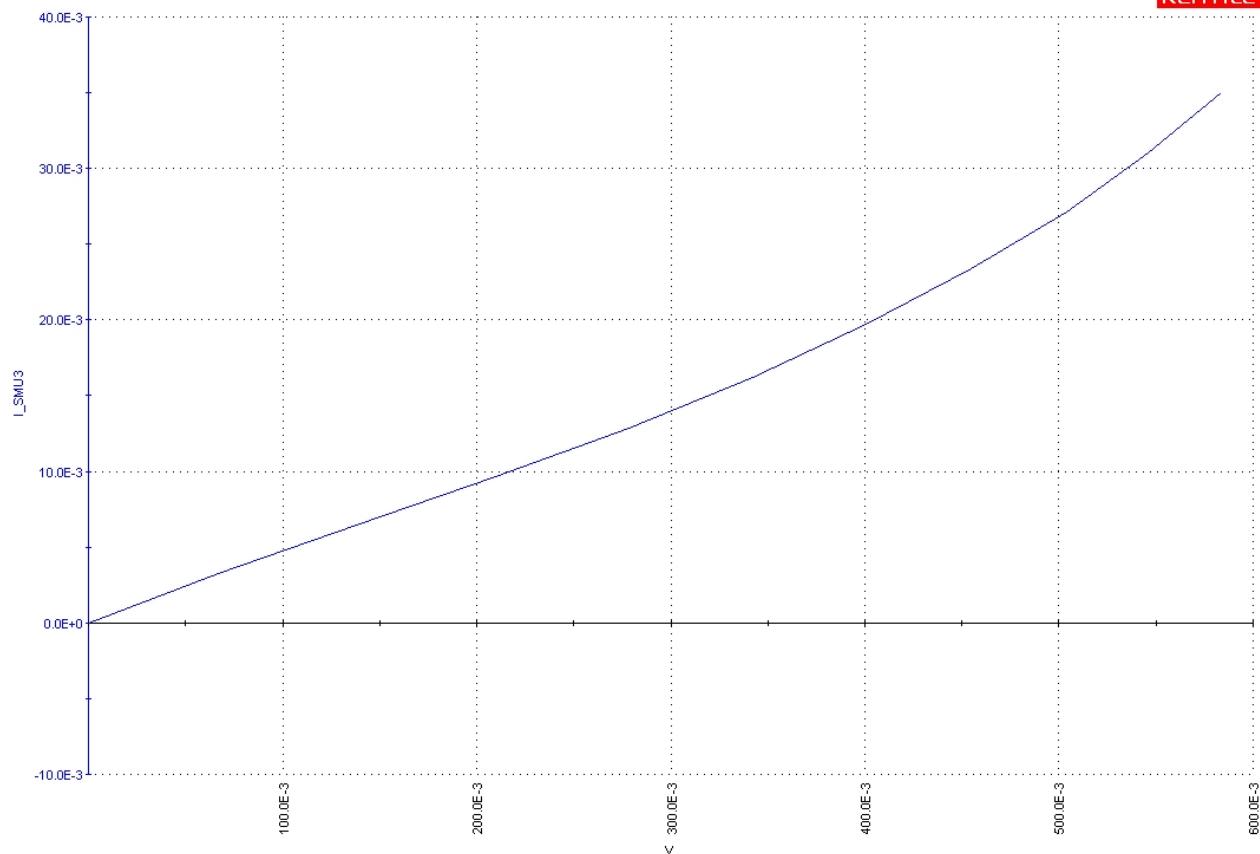
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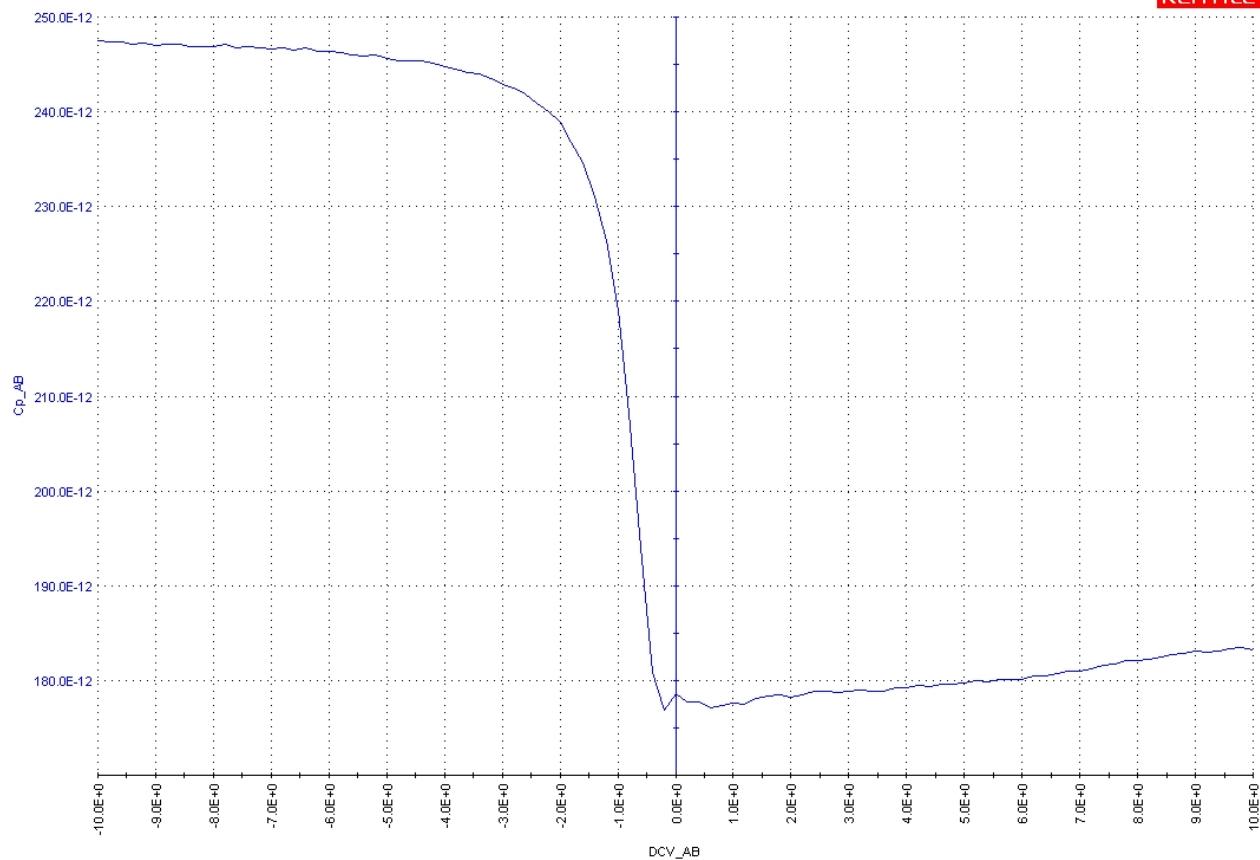
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KEITHLEY



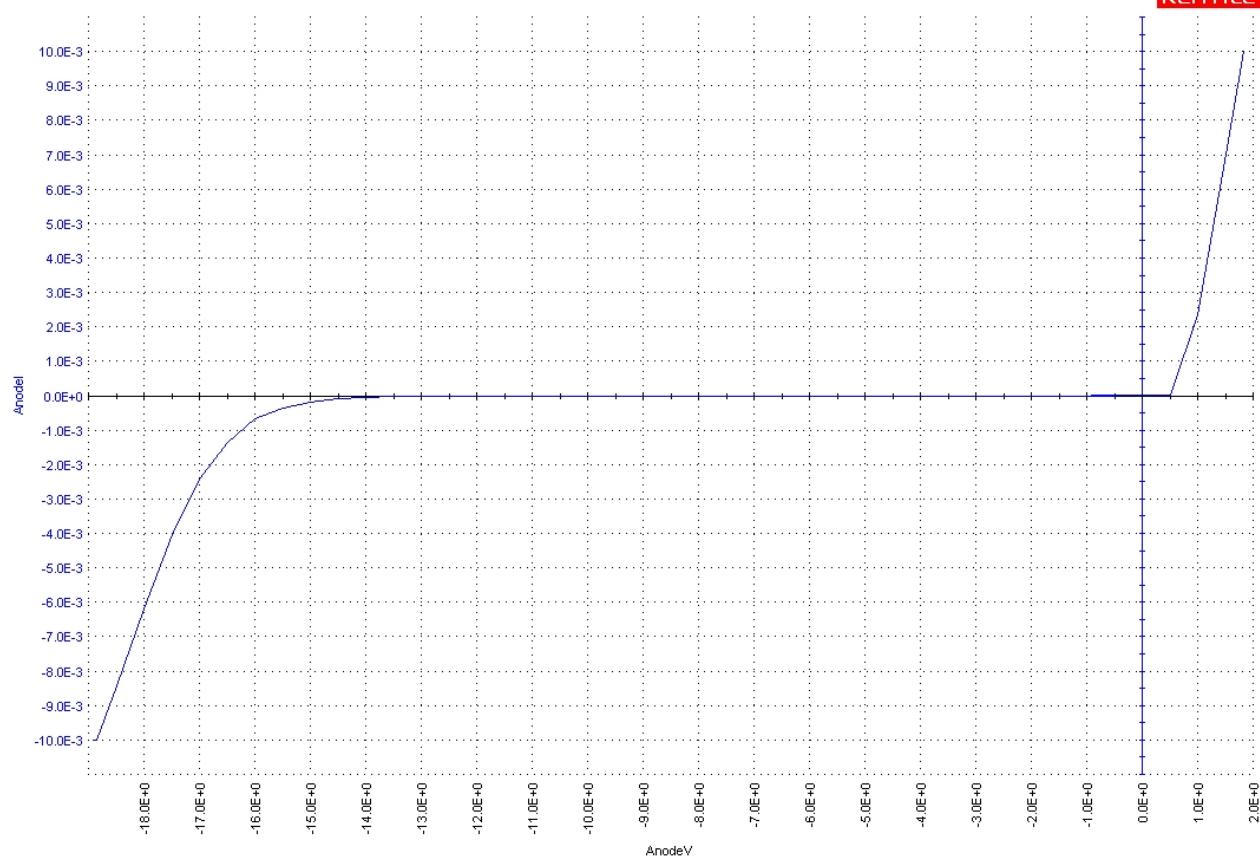
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KEITHLEY



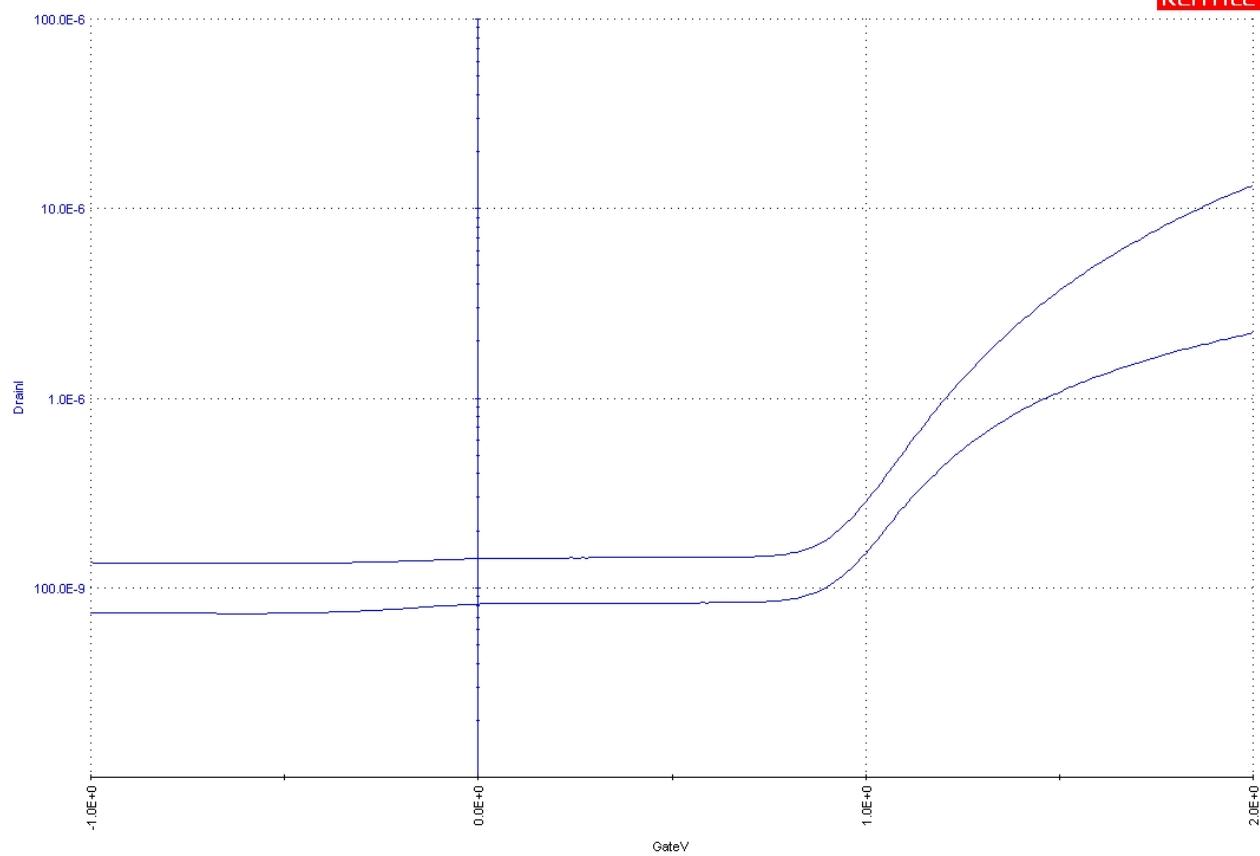
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KEITHLEY



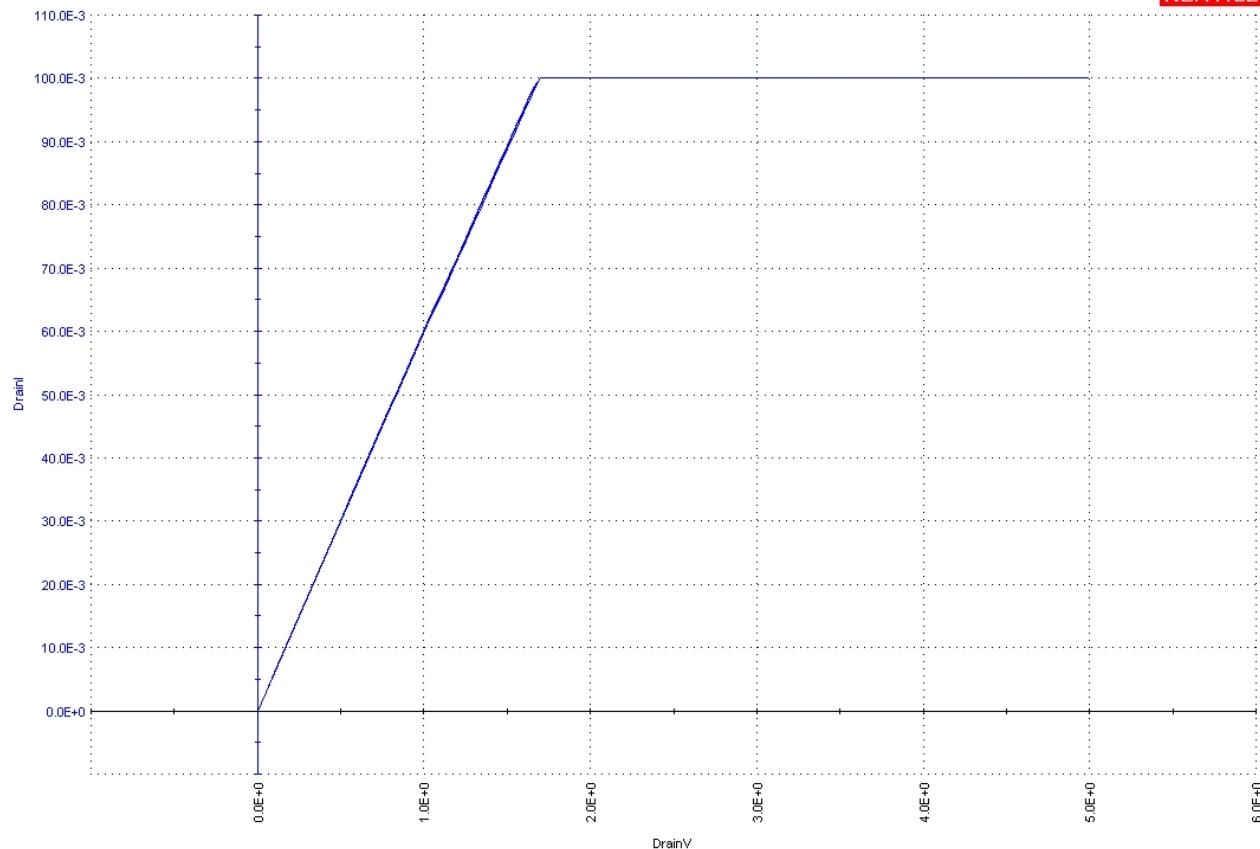
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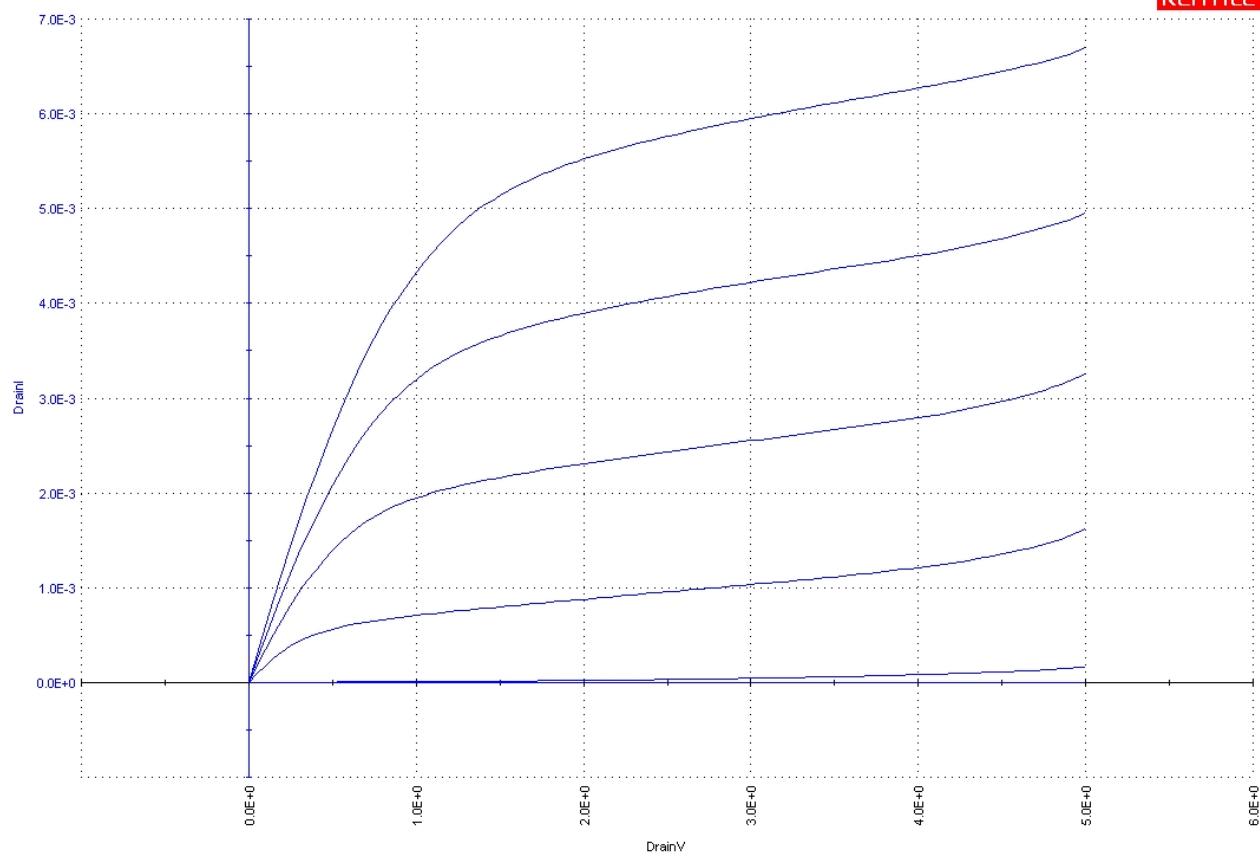
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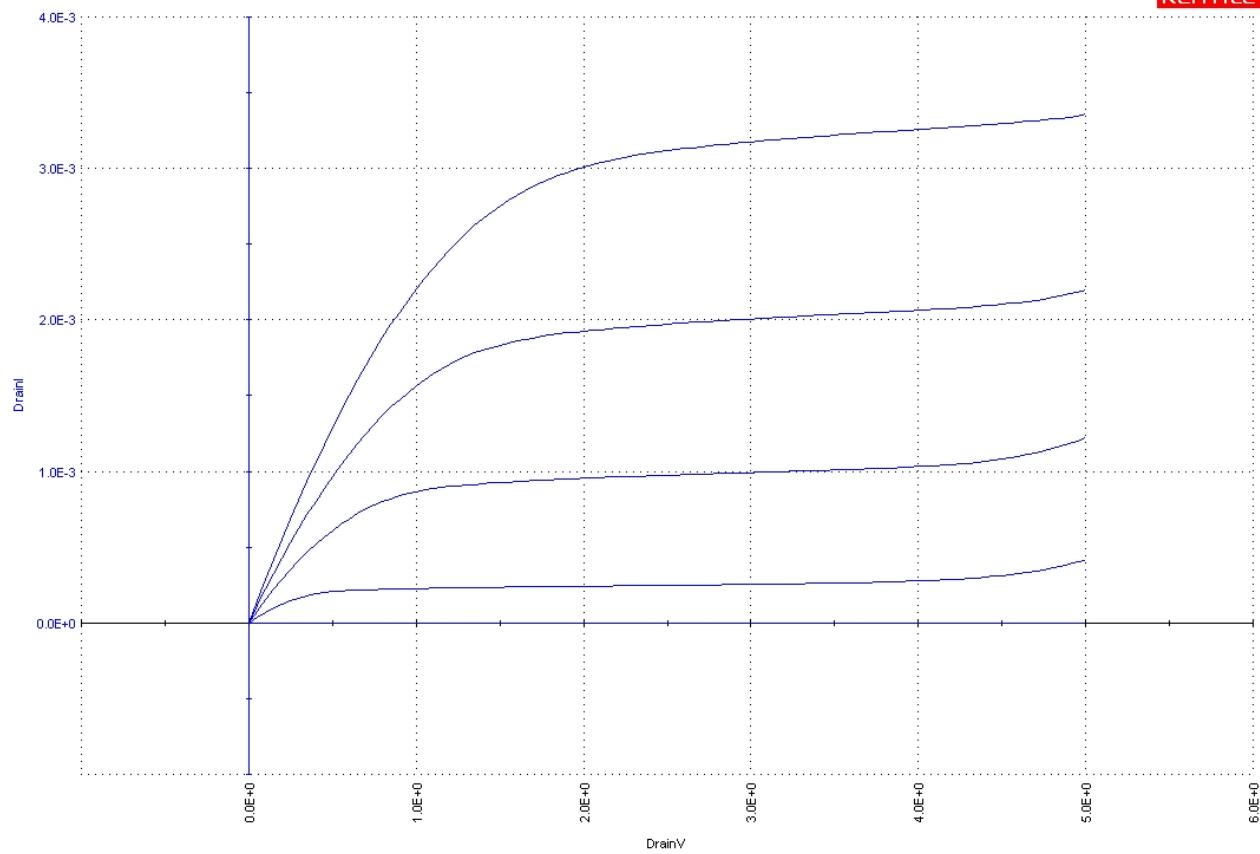
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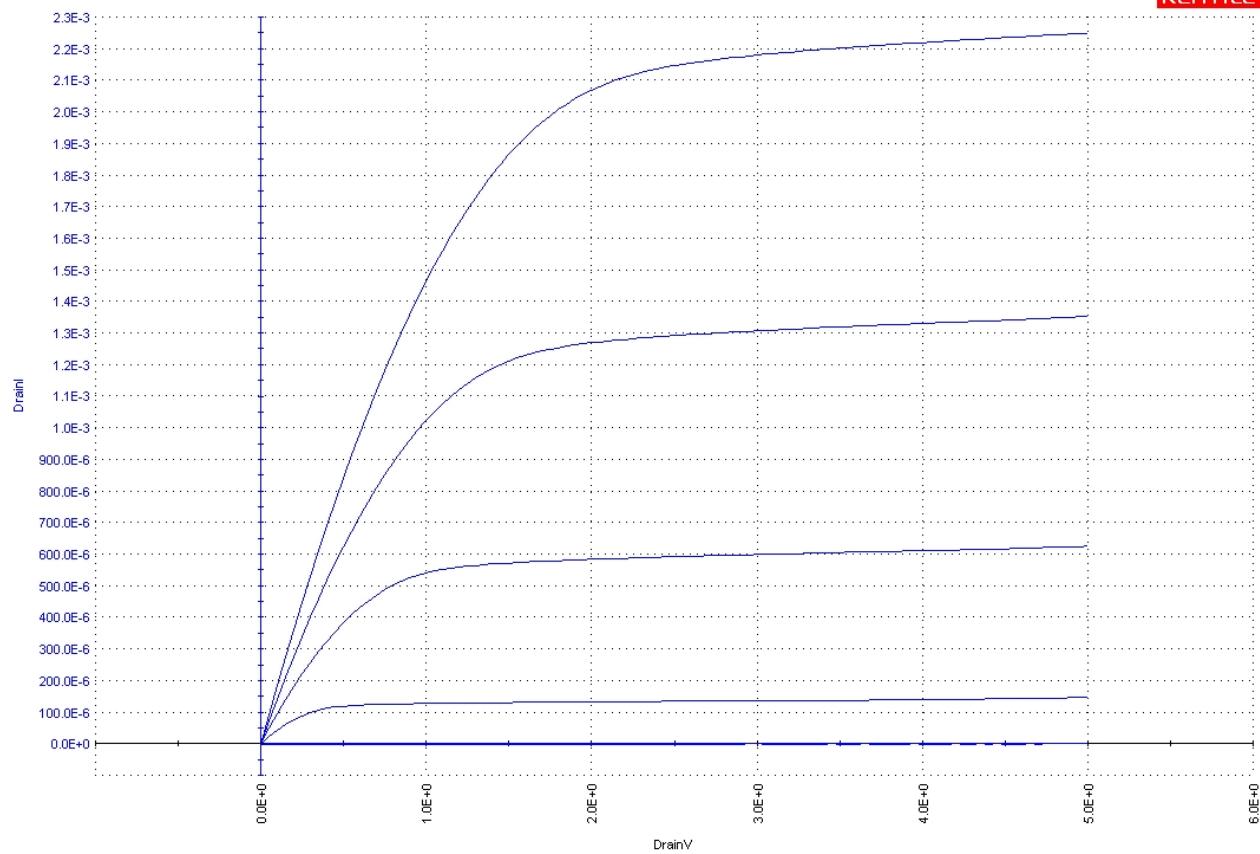
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KEITHLEY



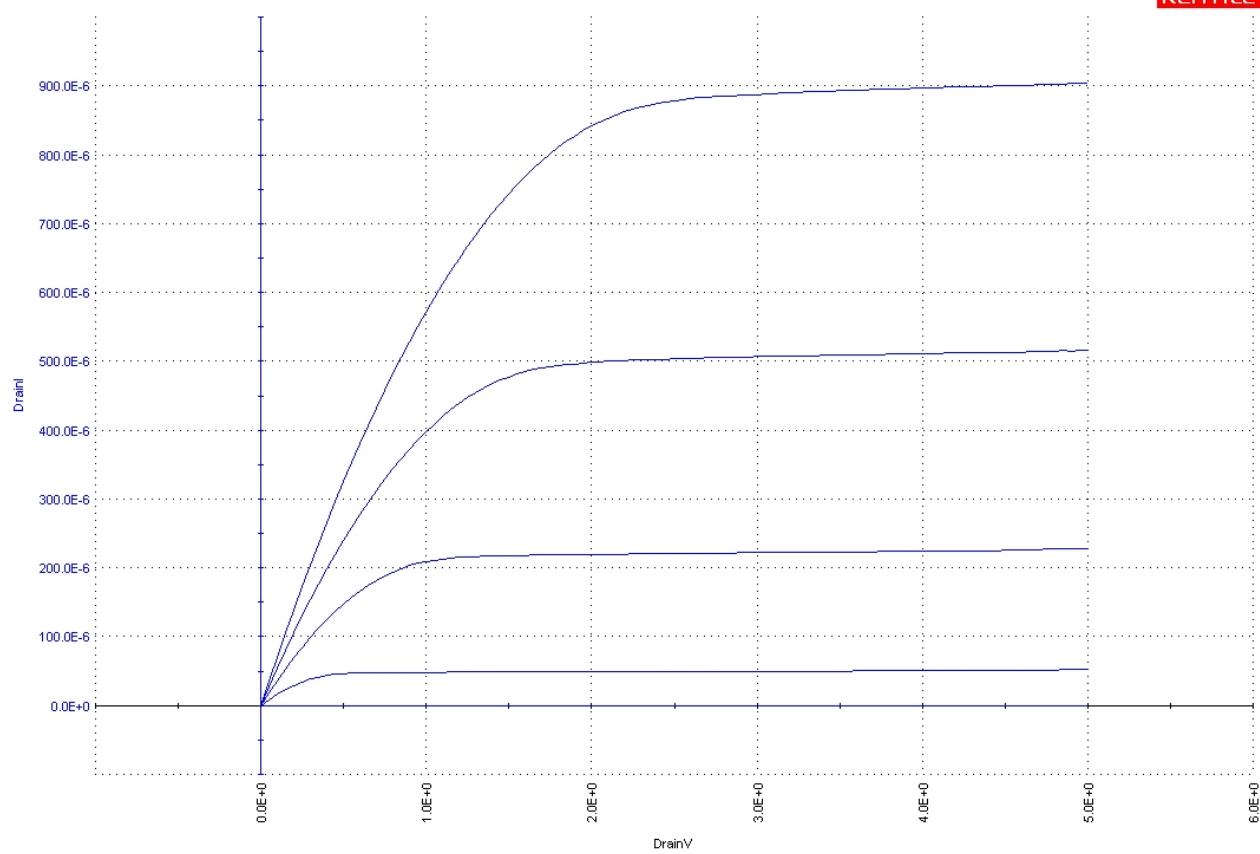
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KEITHLEY



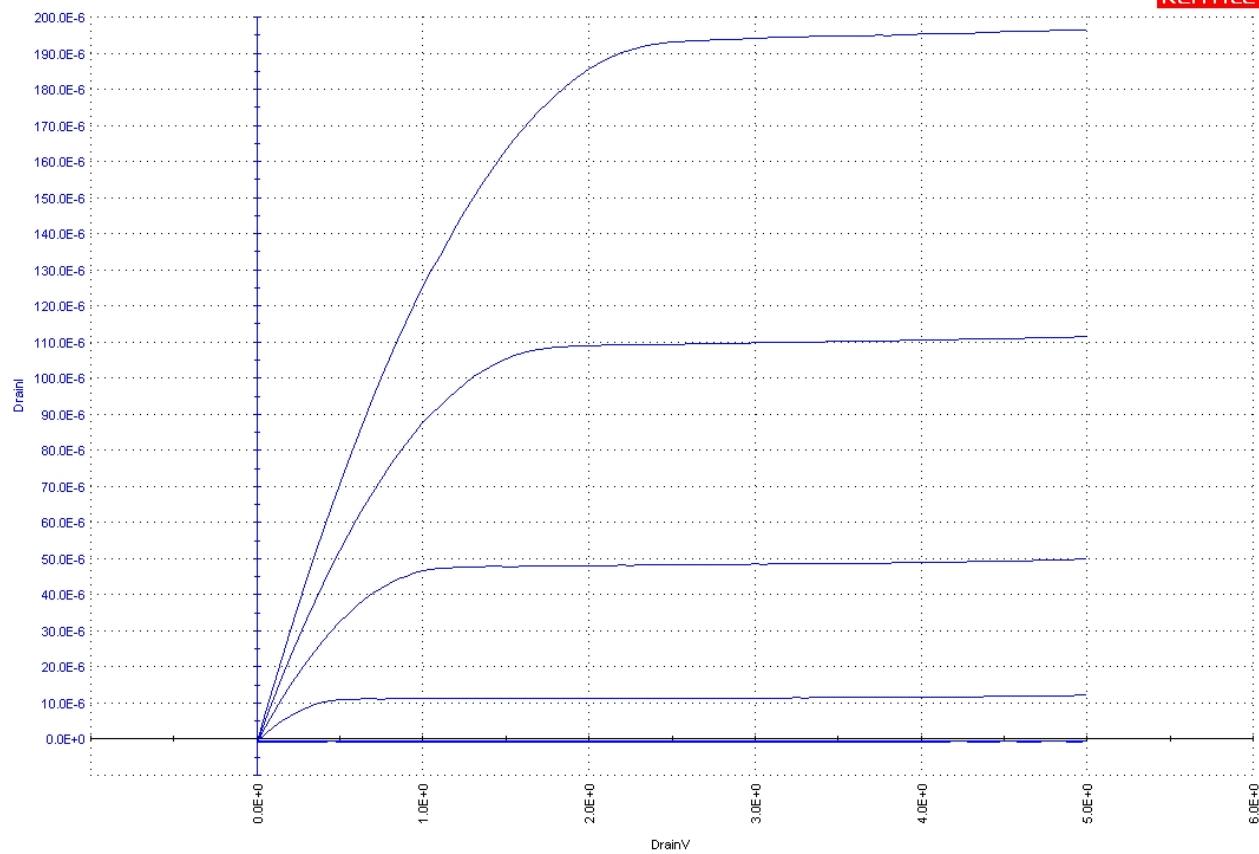
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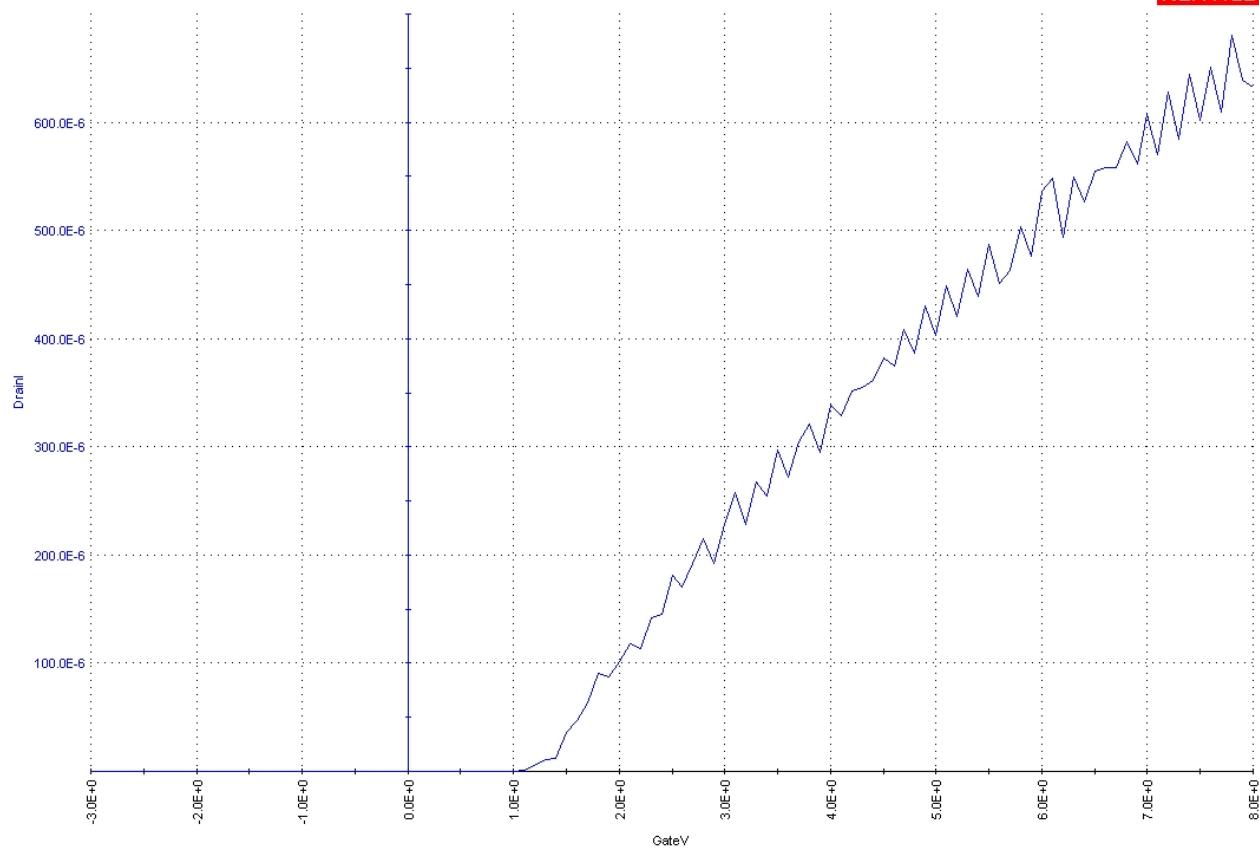
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KEITHLEY



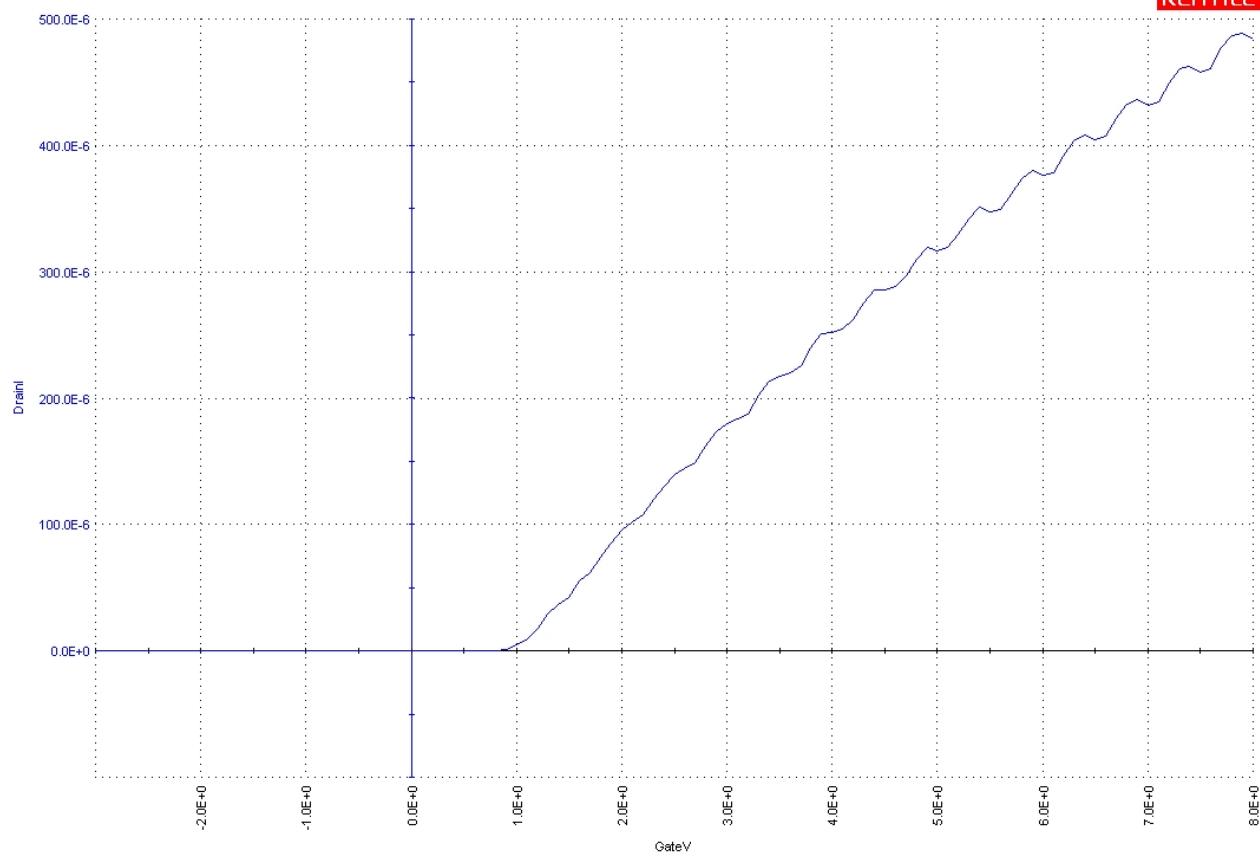
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KEITHLEY



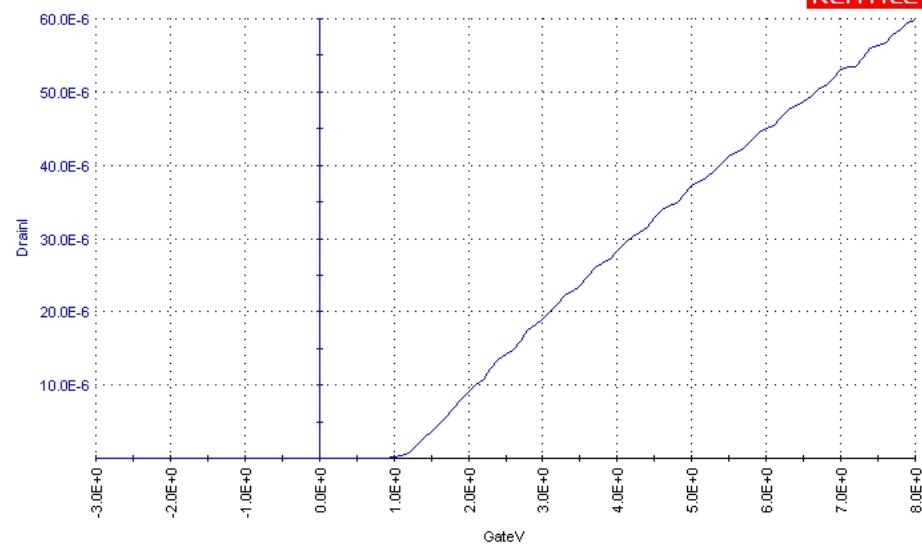
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KEITHLEY



10/17/2023 17:34:55

KEITHLEY



10/27/2023 09:46:09

KEITHLEY

