

LNF Clear Room Labs #1 to #4

Work assignments (One Lab Report)

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Abstract

In this comprehensive semiconductor fabrication lab series, key processes were explored, including thermal oxide growth, LPCVD poly-Si thin film deposition, lithography, dry etching of poly-Si, wet etching of thermal oxide, and metal deposition. The Pre-furnace clean process's significance in ensuring a pristine wafer surface was highlighted, emphasizing the selective removal of contaminants. Variances between oxide growth and polysilicon deposition processes were elucidated, encompassing sources, features, and applications. Color changes in oxidized wafers were linked to thin-film interference, demonstrating the correlation between color and oxide thickness. The ellipsometer's role in measuring oxide thickness was outlined, emphasizing its precision in quantifying critical semiconductor layer dimensions.

Photolithography's use of yellow light for photoresist sensitivity was rationalized, underscoring the necessity for wavelength-specific illumination. Lab outcomes showcased microscopic features post-development and wet etch, providing insights into feature sizes, alignment precision, and potential misalignments. The abstract concludes by emphasizing the overarching importance of these processes in semiconductor manufacturing, influencing device performance, reliability, and optimization. The series contributes to a holistic understanding of semiconductor fabrication, encompassing cleaning protocols, material deposition, lithography, and etching intricacies, crucial for advancing semiconductor device technologies.

Lab Objectives

1. This lab aims to fabricate semiconductor layers by growing a silicon dioxide insulator ("Oxide") and depositing polycrystalline silicon ("Polysilicon") through Low-Pressure Chemical Vapor Deposition (LPCVD). To ensure the success of these processes, an RCA Pre-Furnace Clean is conducted, emphasizing the importance of starting with exceptionally clean wafers.
2. Develop proficiency in photolithography for semiconductor fabrication. Acquire hands-on experience in photoresist application, precise alignment, exposure, and pattern transfer. Learn critical techniques for creating intricate microstructures, ensuring optimal device functionality and performance in advanced semiconductor manufacturing.
3. Develop proficiency in etching for semiconductor fabrication, including the controlled removal of materials in dry etching of poly-Si, wet etching of thermal oxide, and aluminum sputtering. These techniques are fundamental for shaping semiconductor structures, guaranteeing precise functionality and optimal device performance.
4. Acquire specialized skills in metal deposition, aligned lithography, and metal etching for advanced semiconductor fabrication. Learn precise metal layer deposition techniques, ensuring uniformity and adherence. Master aligned lithography methods to achieve accurate pattern transfer onto substrates. Explore controlled metal etching processes, emphasizing residue-free results. Understand the interplay of parameters for optimal resolution and feature precision. Foster expertise in equipment handling, calibration, and process integration. Apply knowledge to enhance semiconductor device manufacturing, addressing challenges in material deposition, lithographic alignment, and etching intricacies for optimal device performance.

Lab #1 Thermal Oxide Growth and LPCVD Poly-Si Thin Film Deposition

1. In the Pre-furnace clean process, why do we mix chemicals right before each cleaning step?

The purpose of mixing chemicals right before each cleaning step in the Pre-furnace clean process is **to ensure the selective removal of unwanted contaminants from the wafer surface**. By maintaining the freshness and reactivity of the cleaning solutions, you increase the likelihood of effectively targeting and removing specific types of contaminants, thus enhancing the overall cleanliness of the wafer before it undergoes high-temperature operations.

2. What are the primary differences between the oxide "growth" and the polysilicon "deposition" processes?

There are three main differences between "growth" and "deposition" processes, which are sources, features, and applications.

For sources, **the material for growth processes is typically sourced directly from the substrate or wafer itself**. For example, in thermal oxidation for oxide growth, oxygen is introduced, and the silicon substrate provides the material for the oxide layer.

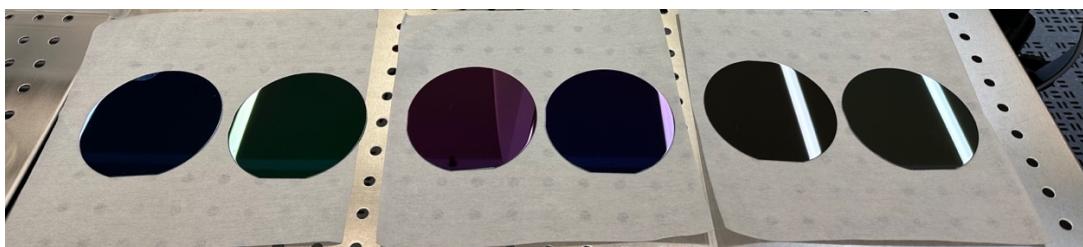
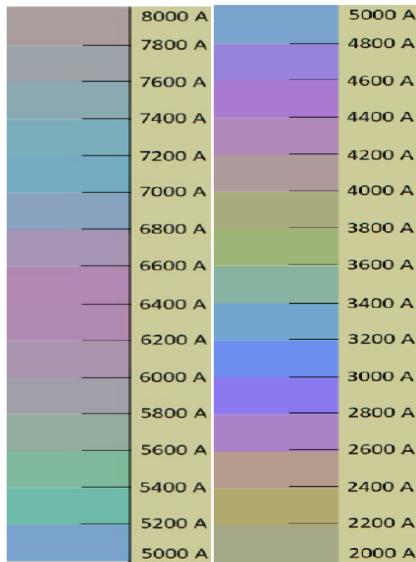
In deposition processes, the material is introduced from an external source. For instance, in polysilicon deposition, silane gas (SiH_4) or another precursor is used to deposit the polysilicon layer onto the substrate.

For features, **the thickness of the grown layer is often more difficult to control precisely compared to deposition processes.** Therefore, the uniformity of the grown layer may vary across the wafer surface.

Lastly, for applications, growth processes are often used for creating insulating layers, such as oxide layers, while deposition processes are often used for adding layers with polysilicon or dielectric materials.

3. What color was the wafer after oxidation, and what oxide thickness does this indicate?

- Figure of corresponding the thickness of wafer with different colors



	Wafer 1	Wafer 2	Wafer 3	Wafer 4	Wafer 5	Wafer 6
Color						
Average thickness (Å)	5000	5200	2600	4600	2000	3600

The color of a thin film on a wafer's surface can be influenced by the film's thickness. This phenomenon is known as thin-film interference. When light interacts with a thin film, such as an oxide layer on a wafer, some wavelengths are reinforced (constructive interference), leading to specific colors being observed.

4. Describe the equipment and mechanism for measuring the oxide thickness.

Although the color information provided for each wafer could be indicative of variations in the oxide thickness, it's important to note that accurately determining the oxide thickness typically requires precise measurement tools like **ellipsometers or spectrophotometers**.

The ellipsometer measures changes in the polarization state of light reflected from a sample. The incident light consists of electric fields vibrating both parallel (p-) and perpendicular (s-) to the plane of incidence with any amplitude and any phase difference.

For mechanism for measuring the oxide thickness, the ellipsometer directs polarized light at the sample surface. As the light interacts with the sample surface, the thin film (oxide layer) causes a differential phase shift and amplitude change between the p- and s- components. The surface properties influence the polarization state of the reflected light. Here is the equation of change in the polarization: $\rho = \tan(\Psi) e^{i\Delta}$.

Ψ (Psi): The amplitude ratio of p- to s- polarized light, often represented as $\tan\Psi$.

Δ (Delta): The phase difference between p- and s- components of the reflected light.

5. Describe what did you learn in this lab.

(a) Keeping surface of the wafer exceptional clean is extreme important before doing further processes, like growth or deposition, since contaminants would be detrimental for the device by trapping the electrons or reducing the reliability through defects. Therefore, Pre-furnace cleaning is a must.

(b) Oxide growth and polysilicon deposition have their own features, which makes themselves unique for various purposes.

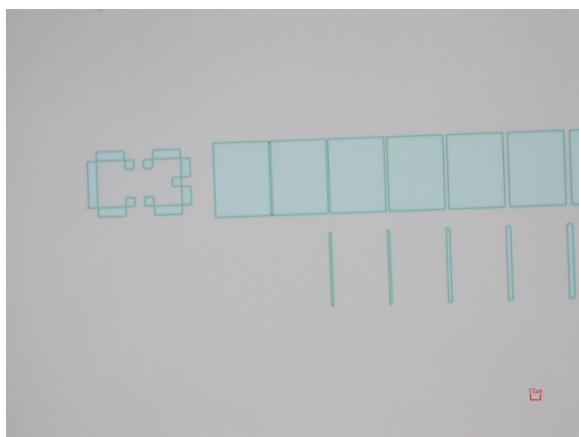
(c) Measuring the thickness of the layers we made is crucial because the different thickness leads to different performance of the devices. For instance, oxide thickness will influence the gate capacitance, threshold voltage, and breakdown voltage. As we known, thinner oxide layer can improve the power consumption and reduces the threshold voltage, but it also can lead to higher leakage current. Thus, we need to measure the thickness of the layers in order to optimize the performance of the devices.

Lab #2 Lithography to Define Poly-Si Layer

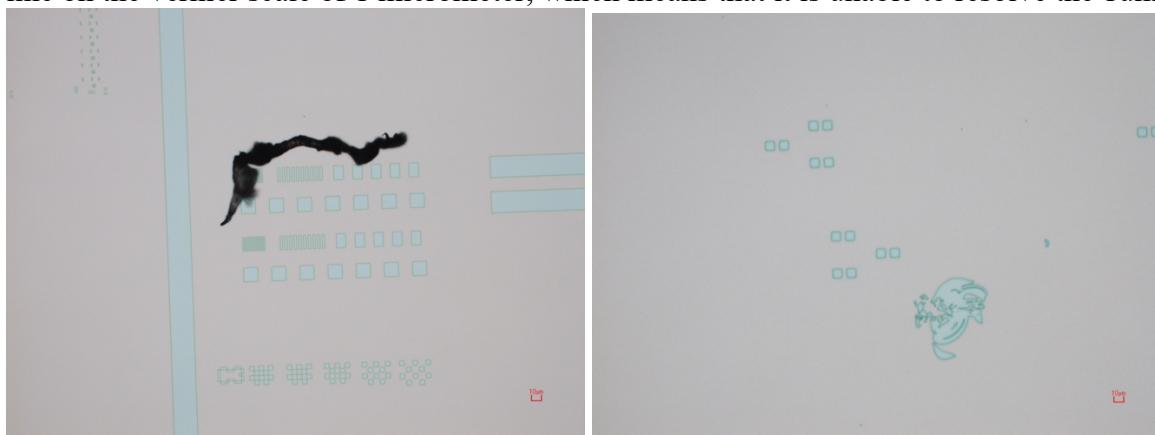
6. Why the area for photolithography has yellow light rather than white light?

Photoresists used in photolithography are typically sensitive to shorter wavelengths of light, such as ultraviolet light. Exposure to such light sources can initiate the chemical reactions in the photoresist, leading to undesired exposure before the actual photolithography process. Therefore, this is the reason why we need to use the yellow light, which is a longer wavelength of light, to be the light in the room of photolithography.

7. Take a microscope image of your sample after development. Explain what you see in the image.



The presence or absence of the marked line on the vernier scale provides information about the achieved feature sizes during the etching process. If the line is visible, it indicates a defined minimum feature size, and if it's not visible, it suggests that the minimum feature size is either smaller or less precisely determined. There is no mark line on the vernier scale of 1 micrometer, which means that it is unable to resolve the 1um.



These figures show that incomplete removal of resist material after the photolithography process can lead to residue, or any other kinds of contaminants. During wet etching, this residue may react with the etchant or interfere with the etch process, causing irregularities, black marks, or peeling.

8. Describe what did you learn in this lab.

I think the photolithography process contains the most numbers of steps among the modules of device fabrication. **The purpose of photolithography is to transfer the pattern from the mask onto the wafer.** Here is a series of brief description for each step in this module.

Substrate Preparation: The substrate is cleaned and coated with a thin layer of photoresist.

Spin-Coating: The wafer is spun at high speed to achieve a uniform and thin coating of photoresist.

Soft Bake: The coated wafer is subjected to a gentle heating process to evaporate solvent and improve the adhesion of the photoresist to the substrate.

Mask Alignment: A photomask containing the desired pattern is aligned over the coated wafer. The mask has transparent and opaque regions corresponding to the pattern to be transferred.

Exposure: The wafer is exposed to UV light through the photomask. The photoresist in the exposed areas undergoes a chemical change, making it either more soluble (positive photoresist) or less soluble (negative photoresist).

Post-Exposure Bake: Another heating step is applied to further stabilize the exposed photoresist.

Developing: The wafer is immersed in a developer solution that selectively removes either the exposed (positive) or unexposed (negative) regions of the photoresist, revealing the pattern.

Etching or Deposition: The exposed substrate is subjected to etching or deposition processes to transfer the pattern onto the substrate surface.

Resist Stripping: The remaining photoresist is removed, leaving the patterned material on the substrate.

Lab #3 Dry Etch of Poly-Si, Wet Etch of Thermal Oxide, and Al Sputtering

9. Why was an extra time (over-etch) added to the wet etch of oxide?

Determination of ending point for etching is important, and over-etching provides a margin of safety for **endpoint detection**, which ensures the desired amount of material is sufficiently removed. This can also lead the surface of wafer to achieve a **well uniformity**.

Since it is common that dry etch has higher selectivity, it can precisely target specific materials for removal without affecting others. As a result, the need for over-etching to ensure uniformity or to compensate for variations in material properties is reduced.

10. Why did we use BHF instead of HF for the wet etch?

Beside reducing the safety risk, the buffering **helps control the etch rate**, making it more predictable and enabling precise removal of material. Moreover, the addition of a buffer in BHF can **enhance etch selectivity**, allowing it to preferentially etch certain materials while being less aggressive towards others.

11. Explain why the aluminum target is not uniformly consumed during sputtering.

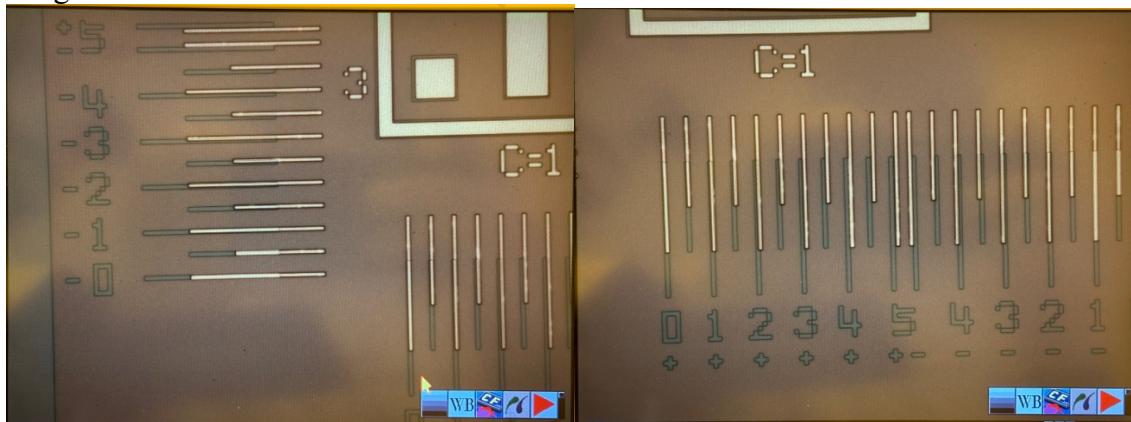
Sputtering relies on high-energy ions bombarding the target material to dislodge atoms. However, **the ion bombardment is not uniform** across the entire target surface. Certain areas experience higher ion flux, leading to uneven erosion. Areas near the center or directly facing the ion source may experience higher ion bombardment energy than regions at the edges or corners of the target.

12. Describe what did you learn in this lab.

I learned about critical processes in semiconductor fabrication, including dry etching of poly-Si, wet etching of thermal oxide, and aluminum sputtering. The importance of over-etching in wet etching was emphasized for endpoint detection and achieving uniformity. The use of buffered hydrofluoric acid (BHF) in wet etching, as opposed to hydrofluoric acid (HF), was explained for safety, controllability, and enhanced etch selectivity. Additionally, I gained insights into the non-uniform consumption of the aluminum target during sputtering, understanding factors like ion bombardment energy and target geometry that contribute to anisotropic erosion.

Lab #4 Metal Deposition, Aligned Lithography and Metal Etching

13. Take a microscope image of your sample after the wet etch. Explain what you see in the image.



According to the above figures, the feature of this device is around 0.5 um on the x-axis and 0.5 on the y-axis, because both lines are overlapped precisely when they were on the spot of 0.5 um and slightly shifted between each other after increasing the number. The higher the number of the line corresponding to the lines on vernier scale, the less precise the feature of the device would be.

14. Estimate the misalignment of your sample. Discuss the potential reason for misalignment in our process.

5M analysis

Manpower (People): Operator mistakes during wafer handling or alignment.

Method (Process): Inaccuracies in the calibration of equipment or flaws in the process integration steps.

Machine (Equipment): Tooling or chucking mechanism problems, inaccuracies in the mask alignment system, or calibration issues.

Material: Non-uniform material deposition affecting layer thickness and alignment.

Measurement (Environment): Flaws in the photolithographic masks or reticles, substrate warping due to uneven stress, or thermal expansion effects.

15. Describe what you learned in this lab

In Lab #4, microscopic analysis post-development revealed a lack of a marked line on the 1-micrometer vernier scale, indicating a potential decrease in resolution compared to Lab #2. The absence suggests an inability to resolve features at the 1-micrometer scale accurately.

Additionally, microscopic images post-wet etches displayed features around 0.5 micrometers on both the x and y axes. The precise overlap of lines at 0.5 micrometers indicates accurate alignment, while subtle shifts with increasing line numbers suggest a potential decrease in feature precision. The correlation between line numbers and feature precision is evident, emphasizing the impact of processing conditions on device features.

Conclusion

The lab series delved into crucial aspects of semiconductor fabrication, illuminating the intricate processes of thermal oxide growth, LPCVD poly-Si thin film deposition, lithography, and metal deposition. The Pre-furnace clean process's role in ensuring a contamination-free substrate was underscored, a prerequisite for subsequent high-temperature operations. Variances between oxide growth and polysilicon deposition processes were delineated, emphasizing their unique features and applications.

The impact of thin-film interference on the color of oxidized wafers provided a visual indicator of oxide thickness. The ellipsometer emerged as a precise tool for quantifying oxide thickness, essential for optimizing device performance. Photolithography's reliance on yellow light for photoresist sensitivity was rationalized, aligning with the semiconductor industry's wavelength-specific requirements.

Microscopic analyses post-development and wet etch unveiled critical insights into feature sizes, alignment precision, and potential misalignments. The series culminated in a comprehensive understanding of semiconductor fabrication, spanning cleaning protocols, material deposition, lithography, and etching intricacies. These processes, as demonstrated in the labs, play pivotal roles in influencing device performance, reliability, and overall optimization.

