SPI HDL Module Documentation

SPI module transmits a byte with the following settings:

- Most significant bit first.
- SCLK frequency = CLK frequency.
- Idle MOSI is low.
- Idle SCLK is low.

Signals

Signal	Direction	Width (bits)	Description
SPI	IN	1	Clock signal
NRST	IN	1	Synchronous reset. Active low
D	IN	8	Next byte to transmit
DS	IN	1	Data set. This signal commands the module to transmit the next byte only if the ongoing transmission has finished
SCLK	OUT	1	SPI clock output
MOSI	OUT	1	SPI data output
TI	OUT	1	Transmission indication