B SK9822 AXI4-lite Module Documentation

SK9822_AXI4 module instantiates the SK9822 module and provides a memory-mapped interface to control it using registers. More information about registers can be found in the Registers.docx file.

Parameters

Parameter	Default value	Type	Description
LED_number	30	Integer	Defines the number of LEDs in the chain
max_brightness	8	Integer	Default value and the maximum value of the global brightness
const_brightness	0	bool	If true, overrides any user global brightness value with the constant one
CLK_divider	50	Integer	Specifies the source CLK frequency division factor for SCLK signal. Can be in range of 1…65535

Signals

Signal	Direction	Width (bits)	Description
CLK	IN	1	Clock signal for SK9822. Must be connected to the same clock signal as AXI4 interfaces.
NRST	IN	1	Synchronous reset for SK9822. Active low. Must be connected to the same reset signal as AXI4 interfaces.
SCLK	OUT	1	SPI clock output. Connect it to GPIO
MOSI	OUT	1	SPI data output. Connect it to GPIO
TI	OUT	1	Transmission interrupt. Connect it to CPU interrupt input
EXT_ST_IN	IN	1	Start transmission input signal from the main instance. It is used to synchronise the transmission start between several SK9822 instances.
EXT_ST_OUT	OUT	1	Start transmission output signal to the secondary instance. It is used to synchronise the transmission start between several SK9822 instances.