**Introduction**

Frequency divider module reduces the input CLK frequency CLK\_divider times.

**Parameters**

|  |  |  |  |
| --- | --- | --- | --- |
| **Parameter** | **Default value** | **Type** | **Description** |
| CLK\_divider | 50 | Integer | Specifies the clock division factor. Can be in range of 1…65535 |

**Signals**

|  |  |  |  |
| --- | --- | --- | --- |
| **Signal** | **Direction** | **Width (bits)** | **Description** |
| CLK\_IN | IN | 1 | Source clock signal |
| CLK\_OUT | OUT | 1 | Divided clock signal |