**Introduction**

SK9822\_AXI4 module instantiates the SK9822 module and provides a memory-mapped interface to control it using registers. More information about registers can be found in the Registers.docx file.

**Parameters**

|  |  |  |  |
| --- | --- | --- | --- |
| **Parameter** | **Default value** | **Type** | **Description** |
| LED\_number | 30 | Integer | Defines the number of LEDs in the chain |
| max\_brightness | 8 | Integer | Default value and the maximum value of the global brightness |
| const\_brightness | 0 | bool | If true, overrides any user global brightness value with the constant one |
| CLK\_divider | 50 | Integer | Specifies the source CLK frequency division factor for SCLK signal. Can be in range of 1…65535 |

**Signals**

|  |  |  |  |
| --- | --- | --- | --- |
| **Signal** | **Direction** | **Width (bits)** | **Description** |
| CLK | IN | 1 | Clock signal for SK9822. Must be connected to the same clock signal as AXI4 interfaces. |
| NRST | IN | 1 | Synchronous reset for SK9822. Active low. Must be connected to the same reset signal as AXI4 interfaces. |
| SCLK | OUT | 1 | SPI clock output. Connect it to GPIO |
| MOSI | OUT | 1 | SPI data output. Connect it to GPIO |
| TI | OUT | 1 | Transmission interrupt. Connect it to CPU interrupt input |